MSE908JB8_3K45H
Rev. 1, 8/2006

Mask Set Errata for Mask 3K45H

Introduction

This mask set errata applies to the mask 3K45H for these products:

- MC68HC908JB8

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 3K45H. All standard devices are marked with a mask set number and a date code.

USB Reset

SE116-USB

Description

When the USB module is enabled, the USB reset disable bit (RSTD) in the configuration register (CONFIG) is cleared and a USB reset is detected, there is a small chance the device will fail.

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Workaround

When the USB module is enabled and a USB reset is detected, either an internal reset or an interrupt to the CPU can be generated. Which one is generated depends on the RSTD bit of CONFIG.

Configuring the USB reset to generate a USB interrupt request to the CPU by setting the RSTD bit of CONFIG fixes this problem. When a USB reset is detected in the interrupt routines, you have two choices:

- Reconfigure the USB module and other related registers
- Use software to cause a device reset, for example, illegal opcode

Example code to implement an illegal opcode:

```
USB_ISR:
     brclr b_RSTF,UIR1,No_USB_Reset ;check USB reset
     db    $32                      ;illegal opcode
No_USB_Reset
```

Power-Up from LVR

SE115-Power

Description

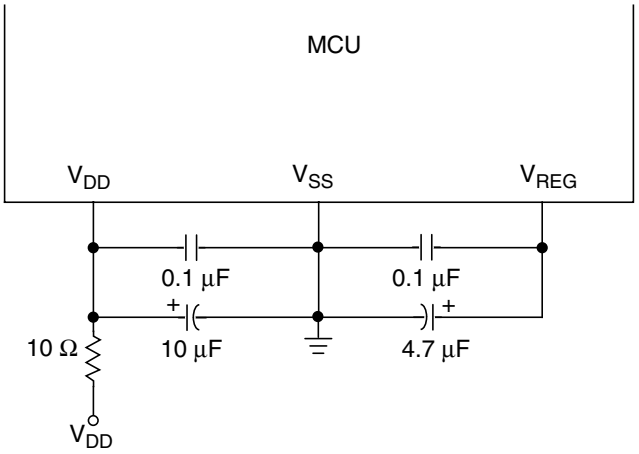
A few devices start abnormally during power-up. The issue is the release of the low voltage reset (LVR) earlier than the V_{REG} reaching the CMOS logic operating voltage (typical 0.65 V).

The LVR takes the V_{DD} but not the V_{REG} as a reference. LVR exists until the V_{DD} reaches the LVR threshold voltage (V_{LVR}). The problem happens in few devices when the V_{DD} rises quickly and the V_{REG} rises slowly. If the LVR has been released but the V_{REG} doesn't reach the CMOS logic operating voltage, the LVR does not have any effect. This might cause the internal logic to improperly initialize and the MCU might not start normally.

Therefore, the V_{DD} voltage must be lower than the VLVR minimum (2.8 V) when the V_{REG} voltage reaches the CMOS logic operating voltage.

Workaround

To fix the problem, add a 10 Ω series resistor between the power supply and the V_{DD}, and place a 10 μF capacitor at the V_{DD} pin and a 4.7 μF capacitor at the V_{REG} pin.



Glitch on Timer Buffered PWM Output

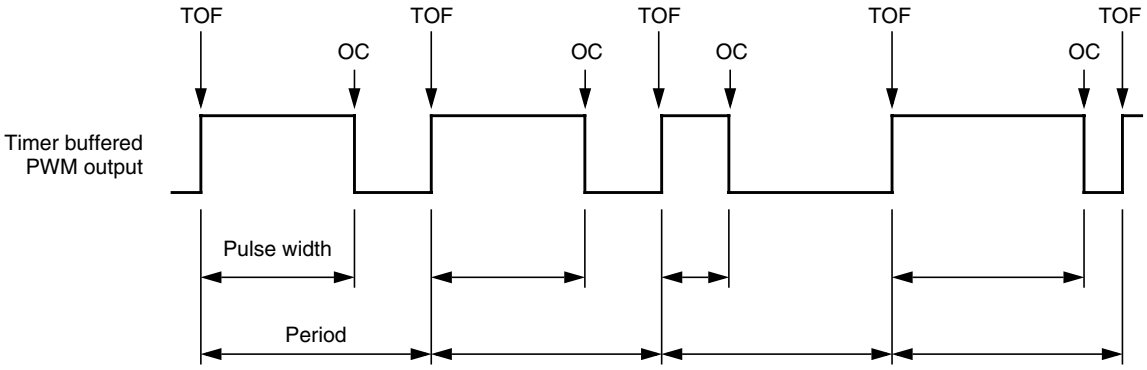
SE30-PWM

In timer buffered PWM operation, when a timer overflow (TOF) event or an output compare (OC) event coincides with a write to either pair of the timer channel registers (TCHxH/L), the duty cycle at the PWM output glitches to 0% or 100% momentarily, then returns to proper operation.

To avoid the glitches when changing the PWM duty cycle, do not write to either pair of the timer channel registers at the TOF or OC.

For example, in the TOF interrupt service routine: If the OC occurs near the last TOF, write to the timer channel registers after the OC; if the OC occurs near the next TOF, write to the timer channel registers before the OC. A write to the channel register high byte (TCHxH) should immediately followed by a write to the low byte (TCHxL) to avoid TOF or OC occurring between the writes. Instruction cycle times must be included when making timing calculations.

The figure below shows a typical timer buffered PWM output waveform, indicating the TOF and OC events.



NOTES:

Do not write to either pair of timer channel registers at:
TOF (timer overflow), or
OC (timer output compare) edges.

In buffered PWM, the pulse width is defined by the last written pair of timer channel registers.
Each pair of timer channel registers consist of a high byte register (TCHxH) and a low byte register (TCHxL).