PCA9632

4-bit Fm+ I²C-bus low power LED driver

Rev. 01 — 28 September 2007 Objective data sheet

1. General description

The PCA9632 is an I²C-bus controlled 4-bit LED driver optimized for Red/Green/Blue/Amber (RGBA) color mixing applications. The PCA9632 is a drop-in upgrade for the PCA9633 with 40× power reduction. In individual brightness control mode, each LED output has its own 8-bit resolution (256 steps) fixed frequency Individual PWM controller that operates at 1.5625 kHz with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. In group dimming mode, each LED output has its own 6-bit resolution (64 steps) fixed frequency Individual PWM controller that operates at 6.25 kHz with a duty cycle that is adjustable from 0 % to 98.4 % to allow the LED to be set to a specific brightness value. A fifth 4-bit resolution (16 steps) Group PWM controller has a fixed frequency of 190 Hz that is used to dim all the LEDs with the same value.

While operating in the Blink mode, each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 1.5625 kHz with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. Blink rate is controlled by the Group Frequency setting that has 8-bit resolution (256 steps). The blink rate is adjustable between 24 Hz to once every 10.73 seconds. For Group Frequency settings between 6 Hz and 24 Hz, the Group PWM has a 6-bit resolution (64 steps) with a duty cycle that is adjustable from 0 % to 98.4 %. For Group frequency settings between 6 Hz to 0.09 Hz (once in 10.73 seconds), the Group PWM has an 8-bit resolution (256 steps) with a duty cycle that is adjustable from 0 % to 99.6 %.

Each LED output can be off, on (no PWM control), set at its Individual PWM controller value or at both Individual and Group PWM controller values. The LED output driver is programmed to be either open-drain with a 25 mA current sink capability at 5 V or totem-pole with a 25 mA sink, 10 mA source capability at 5 V. The PCA9632 operates with a supply voltage range of 2.3 V to 5.5 V and the outputs are 5.5 V tolerant. LEDs can be directly connected to the LED output (up to 25 mA, 5.5 V) or controlled with external drivers and a minimum amount of discrete components for larger current or higher voltage LEDs.

The PCA9632 is in the new Fast-mode Plus (Fm+) family. Fm+ devices offer higher frequency (up to 1 MHz) and more densely populated bus operation (up to 4000 pF).

Software programmable LED Group and three Sub Call I²C addresses allow all or defined groups of PCA9632 devices to respond to a common I²C-bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I²C-bus commands.

The Software Reset (SWRST) Call allows the master to perform a reset of the PCA9632 through the I2C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the outputs to be set high-impedance. This allows an easy and quick way to reconfigure all device registers to the same condition.

2. Features

- 40× power reduction compared to PCA9633
- 4 LED drivers. Each output programmable at:
  - Off
  - On
  - Programmable LED brightness
  - Programmable group dimming/blinking mixed with individual LED brightness
- 1 MHz Fast-mode Plus I2C-bus interface with 30 mA high drive capability on SDA output for driving high capacitive buses
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness using a 1.5625 kHz PWM signal in individual brightness mode
- 64-step (6-bit) linear programmable brightness for each LED output varying from fully off (default) to maximum brightness using a 6.25 kHz PWM signal in Group dim mode
- In group dim mode 16-step group brightness control allows global dimming (using a 190 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness using a 1.5625 kHz PWM signal in group blink mode
- 64-step group blinking with frequency programmable from 24 Hz to 6 Hz and duty cycle from 0 % to 98.4 %
- 256-step group blinking with frequency programmable from 6 Hz to 0.09 Hz (10.73 s) and duty cycle from 0 % to 99.6 %
- Four totem-pole outputs (sink 25 mA and source 10 mA at 5 V) with software programmable open-drain LED outputs selection (default at high-impedance). No input function.
- Output state change programmable on the Acknowledge or the STOP Command to update outputs byte-by-byte or all at the same time (default to 'Change on STOP').
- Software Reset feature (SWRST Call) allows the device to be reset through the I2C-bus
- 400 kHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on SDA/SCL inputs
- Edge rate control on outputs
- No glitch on power-up
- Supports hot insertion
- Low standby current of < 1 μA
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5.5 V tolerant inputs
- –40 °C to +85 °C operation
- ESD protection exceeds 5000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101

- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP8, HVSON8

3. Applications

- RGB or RGBA LED drivers for color mixing
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9632DP1	9632	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9632TK	9632	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT908-1

5. Block diagram

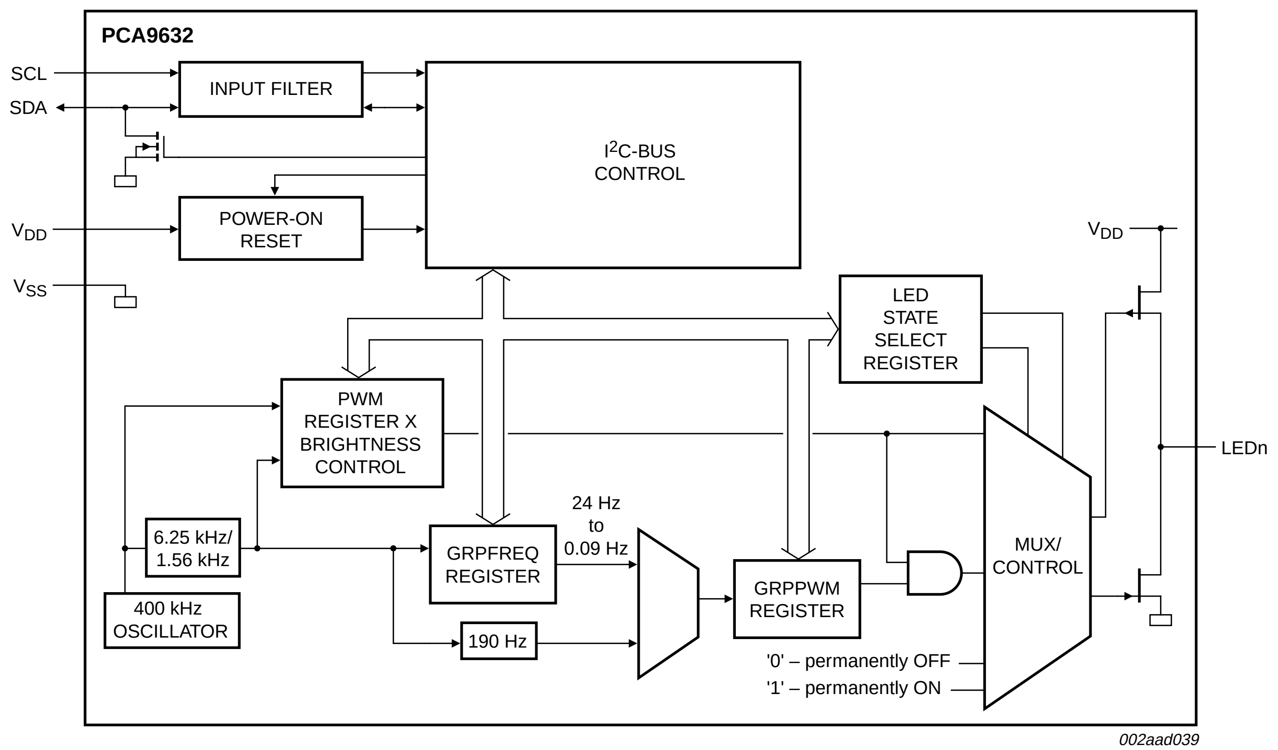


Fig 1. Block diagram of PCA9632

6. Pinning information

6.1 Pinning

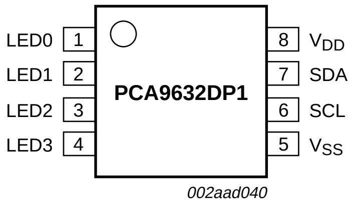


Fig 2. Pin configuration for TSSOP8

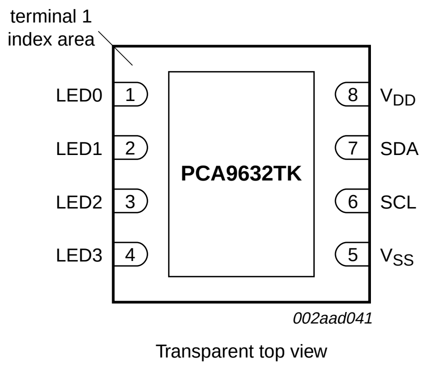


Fig 3. Pin configuration for HVSON8

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
LED0	1	O	LED driver 0
LED1	2	O	LED driver 1
LED2	3	O	LED driver 2
LED3	4	O	LED driver 3
V_{SS}	5[1]	power supply	supply ground
SCL	6	I	serial clock line
SDA	7	I/O	serial data line
V_{DD}	8	power supply	supply voltage

[1] HVSON package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

7. Functional description

Refer to Figure 1 “Block diagram of PCA9632”.

7.1 Device addresses

Following a START condition, the bus master must output the address of the slave it is accessing.

7.1.1 Regular I^{2}C-bus slave address

The I^{2}C-bus slave address of the PCA9632 is shown in Figure 4.

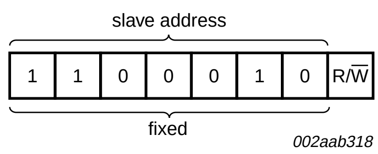


Fig 4. Slave address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

7.1.2 LED All Call I^{2}C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000
- Programmable through I^{2}C-bus (volatile programming)
- At power-up, LED All Call I^{2}C-bus address is enabled. PCA9632 sends an ACK when E0h (R/$\overline{W}$ = 0) or E1h (R/$\overline{W}$ = 1) is sent by the master.

See Section 7.3.8 “LED All Call I^{2}C-bus address, ALLCALLADR” for more detail.

Remark: The default LED All Call I^{2}C-bus address (E0h or 1110 000) must not be used as a regular I^{2}C-bus slave address since this address is enabled at power-up. All the PCA9632s on the I^{2}C-bus will acknowledge the address if sent by the I^{2}C-bus master.

7.1.3 LED Sub Call I^{2}C-bus addresses

- 3 different I^{2}C-bus addresses can be used
- Default power-up values:
  - SUBADR1 register: E2h or 1110 001
  - SUBADR2 register: E4h or 1110 010
  - SUBADR3 register: E8h or 1110 100
- Programmable through I^{2}C-bus (volatile programming)
- At power-up, Sub Call I^{2}C-bus addresses are disabled. PCA9632 does not send an ACK when E2h (R/$\overline{W}$ = 0) or E3h (R/$\overline{W}$ = 1), E4h (R/$\overline{W}$ = 0) or E5h (R/$\overline{W}$ = 1), or E8h (R/$\overline{W}$ = 0) or E9h (R/$\overline{W}$ = 1) is sent by the master.

See Section 7.3.7 “I^{2}C-bus subaddress 1 to 3, SUBADRx” for more detail.

Remark: The default LED Sub Call I²C-bus addresses may be used as regular I²C-bus slave addresses as long as they are disabled.

7.1.4 Software Reset I²C-bus address

The address shown in Figure 5 is used when a reset of the PCA9632 needs to be performed by the master. The Software Reset address (SWRST Call) must be used with R/$\overline{W}$ = 0. If R/$\overline{W}$ = 1, the PCA9632 does not acknowledge the SWRST. See Section 7.5 "Software Reset" for more detail.

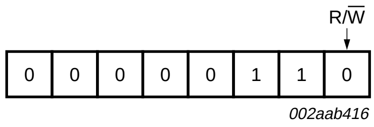


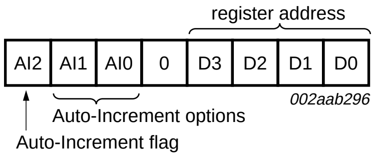
Fig 5. Software Reset address

Remark: The Software Reset I²C-bus address is a reserved address and cannot be used as a regular I²C-bus slave address or as an LED All Call or LED Sub Call address.

7.2 Control register

Following the successful acknowledgement of the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the PCA9632, which will be stored in the Control register.

The lowest 4 bits are used as a pointer to determine which register will be accessed (D[3:0]). The highest 3 bits are used as Auto-Increment flag and Auto-Increment options (AI[2:0]). Bit 4 is unused and must be programmed with zero (0) for proper device operation.



reset state = 80h

Remark: The Control register does not apply to the Software Reset I²C-bus address.

Fig 6. Control register

When the Auto-Increment flag is set (AI2 = 1), the four low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values.

Table 3. Auto-Increment options

AI2	AI1	AI0	Function
0	0	0	no Auto-Increment
1	0	0	Auto-Increment for all registers. D3, D2, D1, D0 roll over to ‘0000’ after the last register (1100) is accessed.
1	0	1	Auto-Increment for individual brightness registers only. D3, D2, D1, D0 roll over to ‘0010’ after the last register (0101) is accessed.
1	1	0	Auto-Increment for global control registers only. D3, D2, D1, D0 roll over to ‘0110’ after the last register (0111) is accessed.
1	1	1	Auto-Increment for individual and global control registers only. D3, D2, D1, D0 roll over to ‘0010’ after the last register (0111) is accessed.

Remark: Other combinations not shown in Table 3 (AI[2:0] = 001, 010, and 011) are reserved and must not be used for proper device operation.

AI[2:0] = 000 is used when the same register must be accessed several times during a single I^{2}C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AI[2:0] = 100 is used when all the registers must be sequentially accessed, for example, power-up programming.

AI[2:0] = 101 is used when the four LED drivers must be individually programmed with different values during the same I^{2}C-bus communication, for example, changing color setting to another color setting.

AI[2:0] = 110 is used when the LED drivers must be globally programmed with different settings during the same I^{2}C-bus communication, for example, global brightness or blinking change.

AI[2:0] = 111 is used when individual and global changes must be performed during the same I^{2}C-bus communication, for example, changing a color and global brightness at the same time.

Only the 4 least significant bits D[3:0] are affected by the AI[2:0] bits.

When the Control register is written, the register entry point determined by D[3:0] is the first register that will be addressed (read or write operation), and can be anywhere between 0000 and 1100 (as defined in Table 4). When AI[2] = 1, the Auto-Increment flag is set and the rollover value at which the point where the register increment stops and goes to the next one is determined by AI[2:0]. See Table 3 for rollover values. For example, if the Control register = 1110 1000 (E8h), then the register addressing sequence will be (in hex):
08 → … → 0C → 00 → … → 07 → 02 → … → 07 → 02 → … → 07 → 02 → … as long as the master keeps sending or reading data.

7.3 Register definitions

Table 4. Register summary[1][2]

Register number (hex)	D3	D2	D1	D0	Name	Type	Function
00h	0	0	0	0	MODE1	read/write	Mode register 1
01h	0	0	0	1	MODE2	read/write	Mode register 2
02h	0	0	1	0	PWM0	read/write	brightness control LED0
03h	0	0	1	1	PWM1	read/write	brightness control LED1
04h	0	1	0	0	PWM2	read/write	brightness control LED2
05h	0	1	0	1	PWM3	read/write	brightness control LED3
06h	0	1	1	0	GRPPWM	read/write	group duty cycle control
07h	0	1	1	1	GRPFREQ	read/write	group frequency
08h	1	0	0	0	LEDOUT	read/write	LED output state
09h	1	0	0	1	SUBADR1	read/write	I^2C-bus subaddress 1
0Ah	1	0	1	0	SUBADR2	read/write	I^2C-bus subaddress 2
0Bh	1	0	1	1	SUBADR3	read/write	I^2C-bus subaddress 3
0Ch	1	1	0	0	ALLCALLADR	read/write	LED All Call I^2C-bus address

[1] Only D[3:0] = 0000 to 1100 are allowed and will be acknowledged. D[3:0] = 1101, 1110, or 1111 are reserved and will not be acknowledged.

[2] When writing to the Control register, bit 4 must be programmed with logic 0 for proper device operation.

7.3.1 Mode register 1, MODE1

Table 5. MODE1 - Mode register 1 (address 00h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	AI2	read only	0	Register Auto-Increment disabled
			1*	Register Auto-Increment enabled
6	AI1	read only	0*	Auto-Increment bit 1 = 0
			1	Auto-Increment bit 1 = 1
5	AI0	read only	0*	Auto-Increment bit 0 = 0
			1	Auto-Increment bit 0 = 1
4	SLEEP	R/W	0	Normal mode[1].
			1*	Low power mode. Oscillator off[2].
3	SUB1	R/W	0*	PCA9632 does not respond to I^2C-bus subaddress 1.
			1	PCA9632 responds to I^2C-bus subaddress 1.
2	SUB2	R/W	0*	PCA9632 does not respond to I^2C-bus subaddress 2.
			1	PCA9632 responds to I^2C-bus subaddress 2.
1	SUB3	R/W	0*	PCA9632 does not respond to I^2C-bus subaddress 3.
			1	PCA9632 responds to I^2C-bus subaddress 3.
0	ALLCALL	R/W	0	PCA9632 does not respond to LED All Call I^2C-bus address.
			1*	PCA9632 responds to LED All Call I^2C-bus address.

[1] It takes 500 μs max. for the oscillator to be up and running once SLEEP bit has been set to logic 1. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 μs window.

[2] No blinking or dimming is possible when the oscillator is off.

7.3.2 Mode register 2, MODE2

Table 6. MODE2 - Mode register 2 (address 01h) bit description
*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	-	read only	0*	reserved
6	-	read only	0*	reserved
5	DMBLNK	R/W	0*	Group control = dimming
			1	Group control = blinking
4	INVRT[1]	R/W	0*	Output logic state not inverted. Value to use when no external driver used.
			1	Output logic state inverted. Value to use when external driver used.
3	OCH	R/W	0*	Outputs change on STOP command.[2]
			1	Outputs change on ACK.
2	OUTDRV[1]	R/W	0*	The 4 LED outputs are configured with an open-drain structure.
			1	The 4 LED outputs are configured with a totem-pole structure.
1 to 0	OUTNE[1:0]	R/W	01*	unused

[1] See Section 7.6 "Using the PCA9632 with and without external drivers" for more details.

[2] Change of the outputs at the STOP command allows synchronizing outputs of more than one PCA9632. Applicable to registers from 02h (PWM0) to 08h (LEDOUT) only.

7.3.3 PWM registers 0 to 3, PWMx—Individual brightness control registers

Table 7. PWM0 to PWM3 - PWM registers 0 to 3 (address 02h to 05h) bit description
*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
02h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000*	PWM0 Individual Duty Cycle
03h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000*	PWM1 Individual Duty Cycle
04h	PWM2	7:0	IDC2[7:0]	R/W	0000 0000*	PWM2 Individual Duty Cycle
05h	PWM3	7:0	IDC3[7:0]	R/W	0000 0000*	PWM3 Individual Duty Cycle

While operating in Individual brightness mode (LDRx = 10), a 1.5625 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = LED output at maximum brightness). In this mode, all the 8 bits are used.

$$duty\ cycle = \frac{IDCx[7:0]}{256} \quad (1)$$

E.g., if IDCx[7:0] = 1111 1111, then duty cycle = 255 / 256 = 99.6 %.

While operating in Group dim mode, a 6.25 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 64 linear steps from 00h (0 % duty cycle = LED output off) to 3Fh (98.4 % duty cycle = LED output at maximum brightness). In this mode only the 6 MSBs are used (IDCx[7:2]). The 2 LSBs IDCx[1:0] are ignored. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT register).

$$duty\ cycle = \frac{IDCx[7:2],00}{256} \quad (2)$$

E.g., if IDCx[7:2] = 111111, then duty cycle = 1111 1100 / 256 = 252 / 256 = 98.4 %.

While operating in blink mode, a 1.5625 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = LED output at maximum brightness). In this mode, all the 8 bits are used.

$$duty\ cycle = \frac{IDCx[7:0]}{256} \quad (3)$$

E.g., if IDCx[7:0] = 1111 1111, then duty cycle = 255 / 256 = 99.6 %.

Applicable to LED outputs programmed with LDRx = 11 (LEDOUT register).

7.3.4 Group duty cycle control, GRPPWM

Table 8. GRPPWM - Group duty cycle control register (address 06h) bit description
*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
06h	GRPPWM	7:0	GDC[7:0]	R/W	1111 1111	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with 0, a 190 Hz fixed frequency signal is superimposed with the 6.25 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a ‘Don’t care’.

In the group dim mode (DMBLNK = 0) global brightness for the 4 outputs is controlled through 16 linear steps from 00h (0 % duty cycle = LED output off) to F0h (93.75 % duty cycle = maximum brightness). In this mode only the 4 MSBs of the GRPPWM[7:4] are used. Bits GRPPWM[3:0] are unused.

$$duty\ cycle = \frac{GDC[7:4],0000}{256} \quad (4)$$

E.g., if GDC[7:4] = 1111, then duty cycle = 1111 0000 / 256 = 240 / 256 = 93.75 %.

When DMBLNK bit is programmed with 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 24 Hz to 10.73 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

In this mode, when GRPFREQ is programmed to provide a blinking with frequency programmable from 24 Hz to 6 Hz, GRPPWM[7:2] is used to provide 64-step duty cycle resolution from 0 % to 98.4 %. GRPPWM[1:0] bits are unused.

$$duty\ cycle = \frac{GDC[7:2],00}{256} \quad (5)$$

E.g., if GDC[7:2] = 111111, then duty cycle = 1111 1100 / 256 = 252 / 256 = 98.4 %.

When GRPFREQ is programmed to provide a blinking with frequency programmable from 6 Hz to 0.09 Hz (10.73 s), GRPPWM[7:0] is used to provide a 256-step duty cycle resolution from 0 % to 99.6 %. In this case, all the 8 bits of the GRPPWM register are used.

$$duty\ cycle = \frac{GDC[7:0]}{256} \quad (6)$$

E.g., If GDC[7:0] = 1111 1111, then duty cycle = 255 / 256 = 99.6 %.

Applicable to LED outputs programmed with LDRx = 11 (LEDOUT register).

7.3.5 Group frequency, GRPFREQ

Table 9. GRPFREQ - Group Frequency register (address 07h) bit description
*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
07h	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a 'Don't care' when DMBLNK = 0. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT register).

Blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 seconds).

$$global\ blinking\ period = \frac{GFRQ[7:0] + 1}{24} (in\ seconds) \quad (7)$$

7.3.6 LED driver output state, LEDOUT

Table 10. LEDOUT - LED driver output state register (address 08h) bit description
*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
08h	LEDOUT	7:6	LDR3	R/W	00*	LED3 output state control
		5:4	LDR2	R/W	00*	LED2 output state control
		3:2	LDR1	R/W	00*	LED1 output state control
		1:0	LDR0	R/W	00*	LED0 output state control

LDRx = 00 — LED driver x is off (default power-up state).

LDRx = 01 — LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10 — LED driver x individual brightness can be controlled through its PWMx register.

LDRx = 11 — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

7.3.7 I²C-bus subaddress 1 to 3, SUBADRx

Table 11. SUBADR1 to SUBADR3 - I²C-bus subaddress registers 0 to 3 (address 09h to 0Bh) bit description
*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
09h	SUBADR1	7:1	A1[7:1]	R/W	1110 001*	I²C-bus subaddress 1
		0	A1[0]	R only	0*	reserved
0Ah	SUBADR2	7:1	A2[7:1]	R/W	1110 010*	I²C-bus subaddress 2
		0	A2[0]	R only	0*	reserved
0Bh	SUBADR3	7:1	A3[7:1]	R/W	1110 100*	I²C-bus subaddress 3
		0	A3[0]	R only	0*	reserved

Subaddresses are programmable through the I^{2}C-bus. Default power-up values are E2h, E4h, E8h, and the device(s) will not acknowledge these addresses right after power-up (the corresponding SUBx bit in MODE1 register is equal to 0).

Once subaddresses have been programmed to their right values, SUBx bits need to be set to 1 in order to have the device acknowledging these addresses (MODE1 register).

Only the 7 MSBs representing the I^{2}C-bus subaddress are valid. The LSB in SUBADRx register is a read-only bit (0).

When SUBx is set to 1, the corresponding I^{2}C-bus subaddress can be used during either an I^{2}C-bus read or write sequence.

7.3.8 LED All Call I^{2}C-bus address, ALLCALLADR

Table 12. ALLCALLADR - LED All Call I^{2}C-bus address register (address 0Ch) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
0Ch	ALLCALLADR	7:1	AC[7:1]	R/W	1110 000*	ALLCALL I^{2}C-bus address register
		0	AC[0]	R only	0*	reserved

The LED All Call I^{2}C-bus address allows all the PCA9632s in the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to 1, power-up default state). This address is programmable through the I^{2}C-bus and can be used during either an I^{2}C-bus read or write sequence. The register address can be programmed as a sub call.

Only the 7 MSBs representing the All Call I^{2}C-bus address are valid. The LSB in ALLCALLADR register is a Read-only bit (0).

If ALLCALL bit = 0, the device does not acknowledge the address programmed in register ALLCALLADR.

7.4 Power-on reset

When power is applied to V_{DD}, an internal Power-on reset holds the PCA9632 in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9632 registers and I^{2}C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

7.5 Software Reset

The Software Reset Call (SWRST Call) allows all the devices in the I2C-bus to be reset to the power-up state value through a specific formatted I2C-bus command. To be performed correctly, it implies that the I2C-bus is functional and that there is no device hanging the bus.

The SWRST Call function is defined as the following:

1. A START command is sent by the I2C-bus master.
2. The reserved SWRST I2C-bus address '0000 011' with the R/$\overline{W}$ bit set to 0 (write) is sent by the I2C-bus master.
3. The PCA9632 device(s) acknowledge(s) after seeing the SWRST Call address '0000 0110' (06h) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I2C-bus master.
4. Once the SWRST Call address has been sent and acknowledged, the master sends 2 bytes with 2 specific values (SWRST data byte 1 and byte 2):
   a. Byte 1 = A5h: the PCA9632 acknowledges this value only. If byte 1 is not equal to A5h, the PCA9632 does not acknowledge it.
   b. Byte 2 = 5Ah: the PCA9632 acknowledges this value only. If byte 2 is not equal to 5Ah, then the PCA9632 does not acknowledge it.

   If more than 2 bytes of data are sent, the PCA9632 does not acknowledge any more.
5. Once the right 2 bytes (SWRST data byte 1 and byte 2 only) have been sent and correctly acknowledged, the master sends a STOP command to end the SWRST Call: the PCA9632 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

The I2C-bus master must interpret a non-acknowledge from the PCA9632 (at any time) as a 'SWRST Call Abort'. The PCA9632 does not initiate a reset of its registers. This happens only when the format of the SWRST Call sequence is not correct.

7.6 Using the PCA9632 with and without external drivers

The PCA9632 LED output drivers are 5.5 V only tolerant and can sink up to 25 mA at 5 V.

If the device needs to drive LEDs to a higher voltage and/or higher current, use of an external driver is required.

- INVRT bit (MODE2 register) can be used to keep the LED PWM control firmware the same (PWMx and GRPPWM values directly calculated from their respective formulas and the LED output state determined by LEDOUT register value) independently of the type of external driver.
- OUTDRV bit (MODE2 register) allows minimizing the amount of external components required to control the external driver (N-type or P-type device).

Table 13. Use of INVRT and OUTDRV based on connection to the LEDn outputs

INVRT	OUTDRV	Direct connection to LEDn		External N-type driver		External P-type driver	
		Firmware	External pull-up resistor	Firmware	External pull-up resistor	Firmware	External pull-up resistor
0	0	formulas and LED output state values apply[1]	LED current limiting R[1]	formulas and LED output state values inverted	required	formulas and LED output state values apply	required
0	1	formulas and LED output state values apply[1]	LED current limiting R[1]	formulas and LED output state values inverted	not required	formulas and LED output state values apply[3]	not required[3]
1	0	formulas and LED output state values inverted	LED current limiting R	formulas and LED output state values apply	required	formulas and LED output state values inverted	required
1	1	formulas and LED output state values inverted	LED current limiting R	formulas and LED output state values apply[2]	not required[2]	formulas and LED output state values inverted	not required

[1] Correct configuration when LEDs directly connected to the LEDn outputs (connection to V_{DD} through current limiting resistor).

[2] Optimum configuration when external N-type (NPN, NMOS) driver used.

[3] Optimum configuration when external P-type (PNP, PMOS) driver used.

Table 14. Output transistors based on LEDOUT registers, INVRT and OUTDRV bits

LEDOUT	INVRT	OUTDRV	Upper transistor (V_{DD} to LEDn)	Lower transistor (LEDn to V_{SS})	LEDn state
00	0	0	off	off	high-Z[1]
LED driver off	0	1	on	off	V_{DD}
	1	0	off	on	V_{SS}
	1	1	off	on	V_{SS}
01	0	0	off	on	V_{SS}
LED driver on	0	1	off	on	V_{SS}
	1	0	off	off	high-Z[1]
	1	1	on	off	V_{DD}
10	0	0	off	Individual PWM (non-inverted)	V_{SS} or high-Z[1] = PWMx value
Individual brightness control	0	1	Individual PWM (non-inverted)	Individual PWM (non-inverted)	V_{SS} or V_{DD} = PWMx value
	1	0	off	Individual PWM (inverted)	high-Z[1] or V_{SS} = 1 – PWMx value
	1	1	Individual PWM (inverted)	Individual PWM (inverted)	V_{DD} or V_{SS} = 1 – PWMx value
11	0	0	off	Individual + Group PWM (non-inverted)	V_{SS} or high-Z[1] = PWMx/GRPPWM values
Individual + Group dimming/ blinking	0	1	Individual PWM (non-inverted)	Individual PWM (non-inverted)	V_{SS} or V_{DD} = PWMx/GRPPWM values
	1	0	off	Individual + Group PWM (inverted)	high-Z[1] or V_{SS} = (1 – PWMx) or (1 – GRPPWM) values
	1	1	Individual PWM (inverted)	Individual PWM (inverted)	V_{DD} or V_{SS} = (1 – PWMx) or (1 – GRPPWM) values

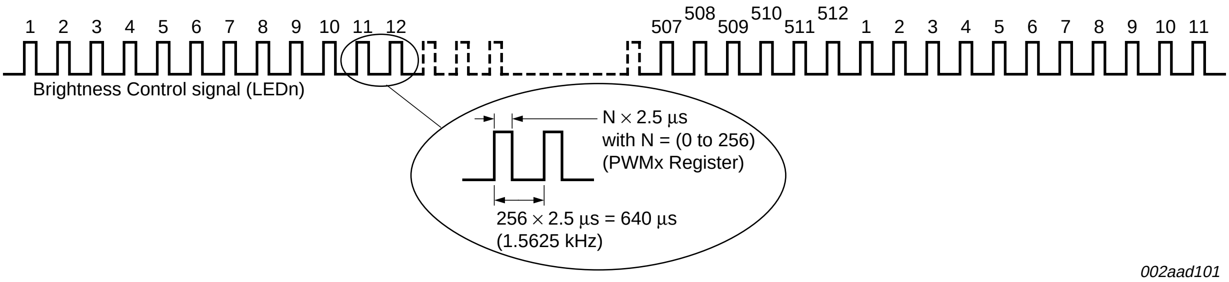
[1] External pull-up or LED current limiting resistor connects LEDn to V_{DD}.

7.7 Individual brightness control with group dimming/blinking

A 1.5625 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

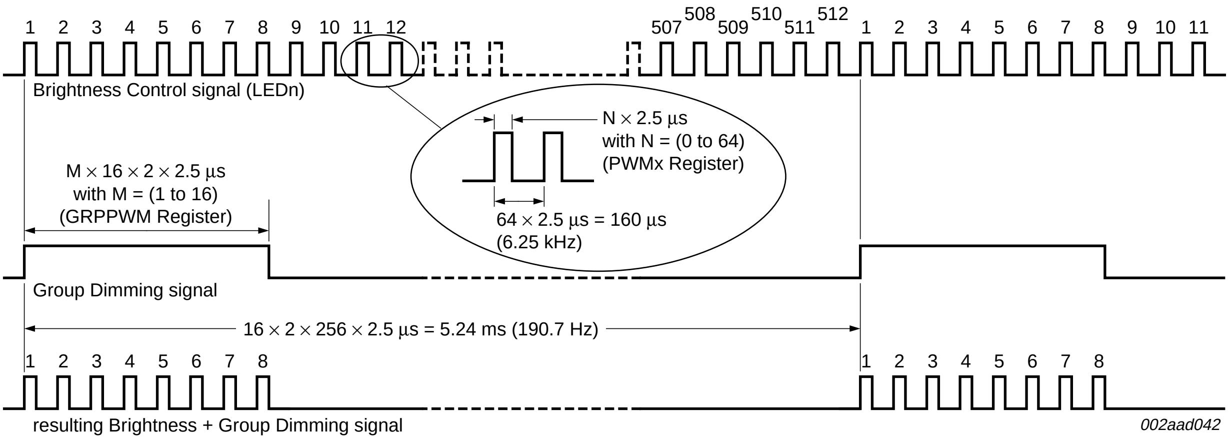
On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 4 LED outputs):

- A lower 190 Hz fixed frequency signal with programmable duty cycle (4 bits, 16 steps) is used to provide a global brightness control.
- A programmable frequency signal from 24 Hz to $^1\!/_{10.73}$ Hz (8 bits, 256 steps) with programmable duty cycle (6 bits, 64 steps) is used to provide a global blinking control for (24 Hz to 6 Hz) and (8 bits, 256 steps) for (6 Hz to $^1\!/_{10.73}$ Hz).



Minimum pulse width for LEDn Brightness Control is 2.5 µs.

Fig 7. Individual LED Brightness Control signals



Minimum pulse width for LEDn Brightness Control is 2.5 µs.

Minimum pulse width for Group Dimming is 80 µs.

When M = 1 (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal will have 2 pulses of the LED Brightness Control signal (pulse width = N × 2.5 µs, with 'N' defined in PWMx register).

Fig 8. Brightness + Group Dimming signals

Table 15. Dimming and blinking resolution

Type of control	LDRx	DMBLNK	GRPPWM	GRPFREQ	Frequency	PWMx
Individual LED brightness without dimming	10	X	X	X	1.5625 kHz	256 steps
Individual LED brightness with global dimming	11	0	16 steps	X	190 Hz with 6.25 kHz modulation	64 steps
Blinking (fast)	11	1	64 steps	256 steps	blink frequency = 6 Hz to 24 Hz PWMx frequency = 1.5625 kHz	256 steps
Blinking (slow)	11	1	256 steps	256 steps	blink frequency = 0.09 Hz to 6 Hz PWMx frequency = 1.5625 kHz	256 steps

8. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 9).

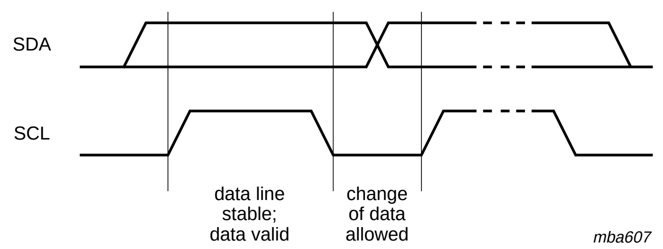


Fig 9. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 10.)

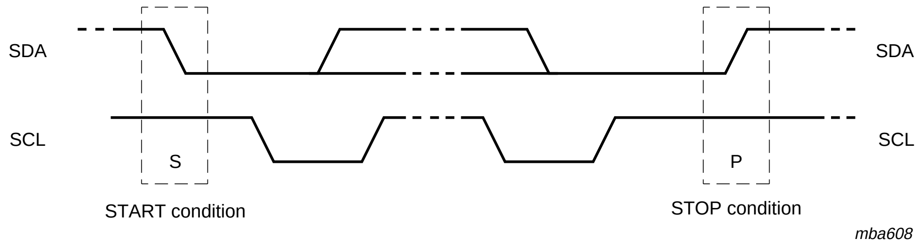


Fig 10. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 11).

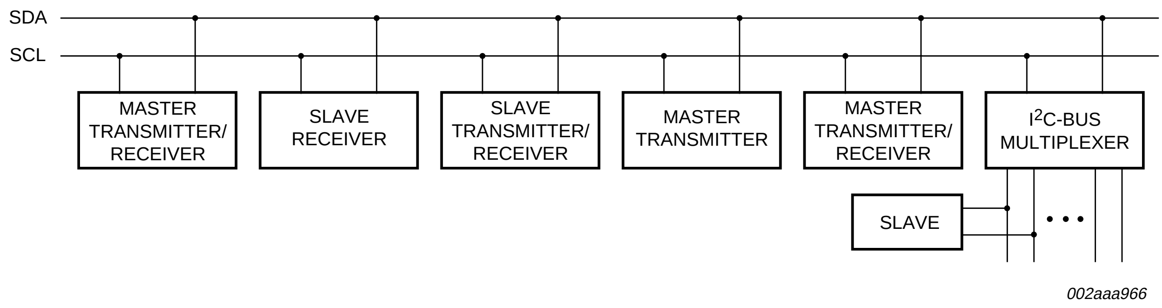


Fig 11. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

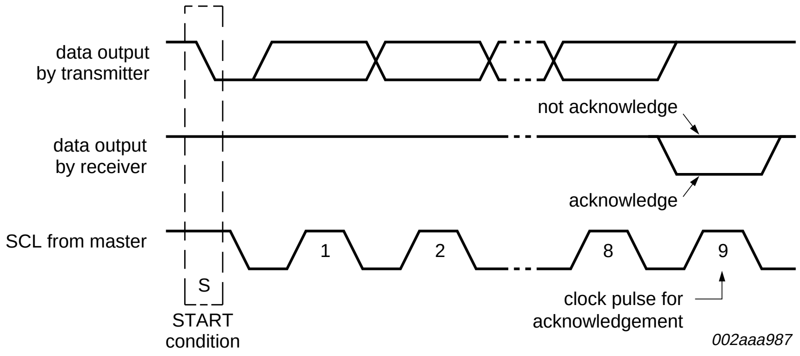
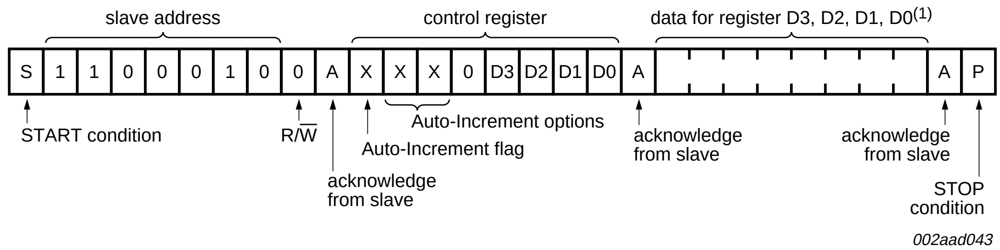


Fig 12. Acknowledgement on the I²C-bus

9. Bus transactions



(1) See Table 4 for register definition.

Fig 13. Write to a specific register

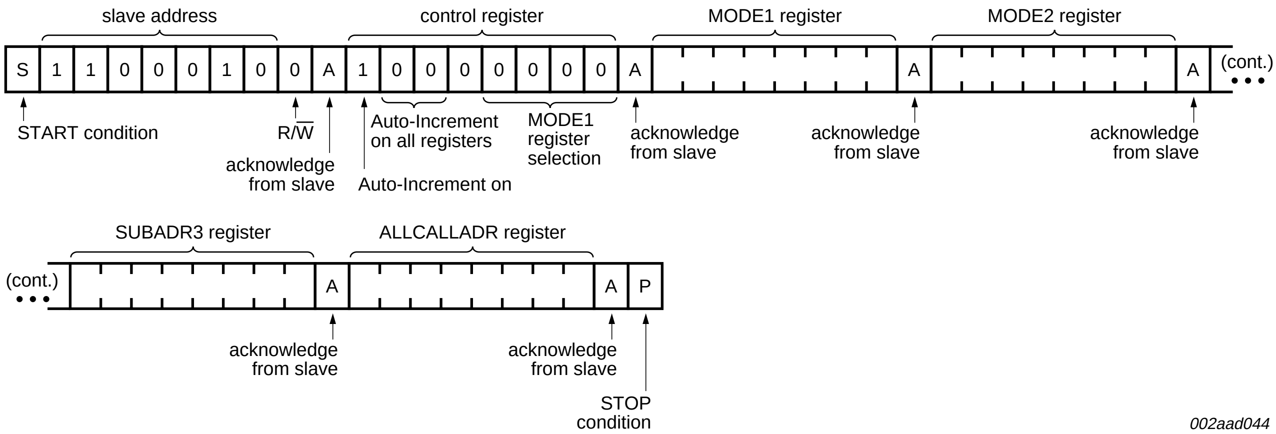


Fig 14. Write to all registers using the Auto-Increment feature

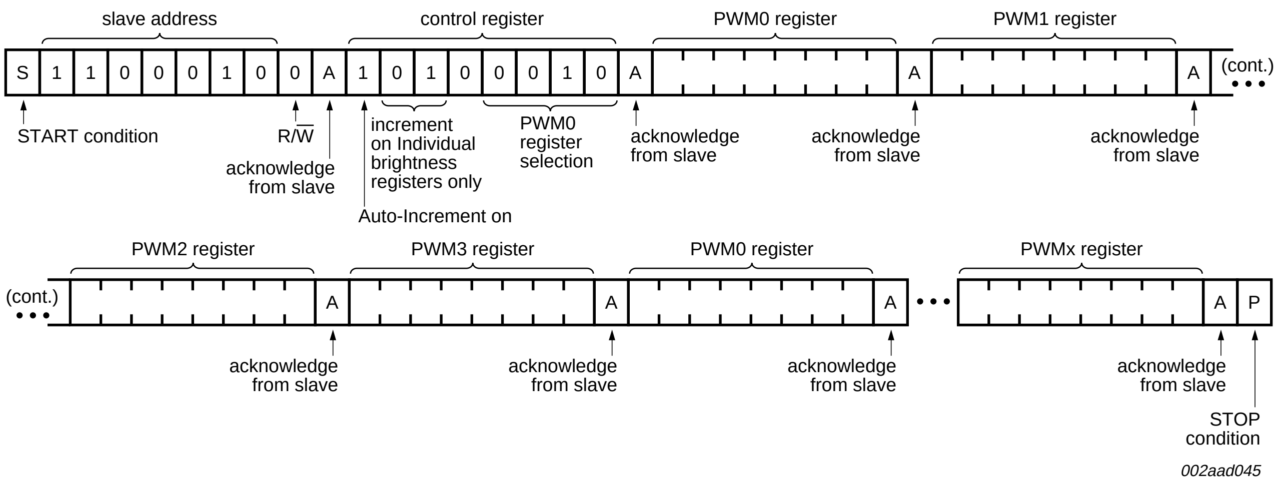


Fig 15. Multiple writes to Individual Brightness registers only using the Auto-Increment feature

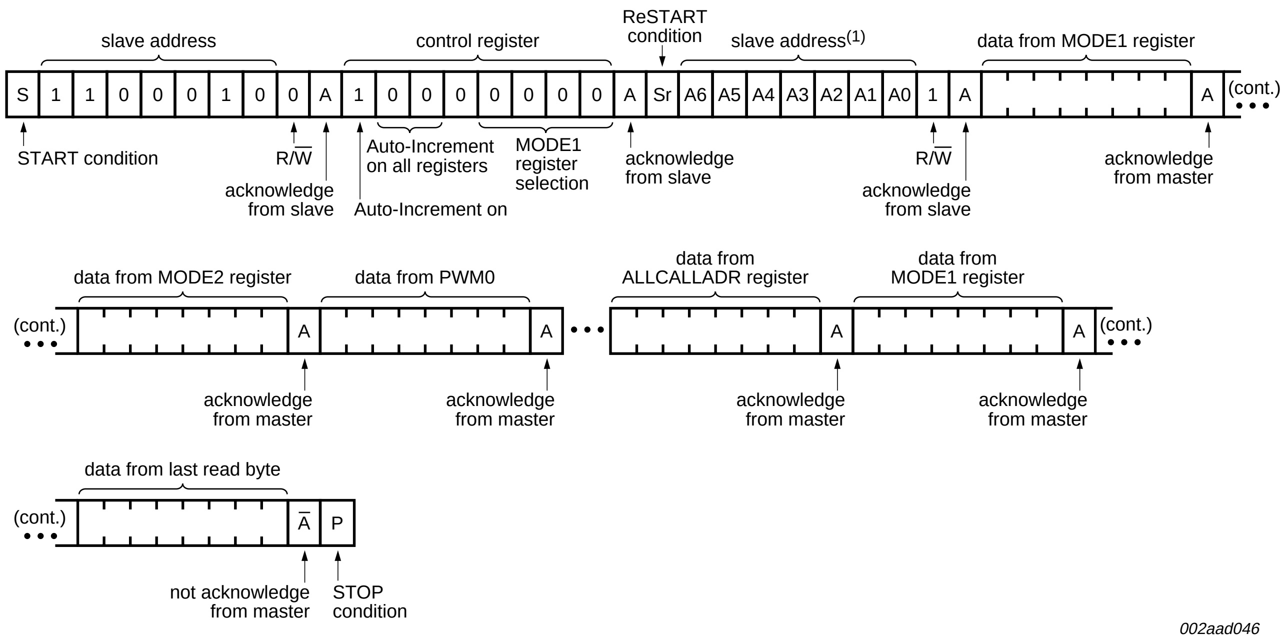
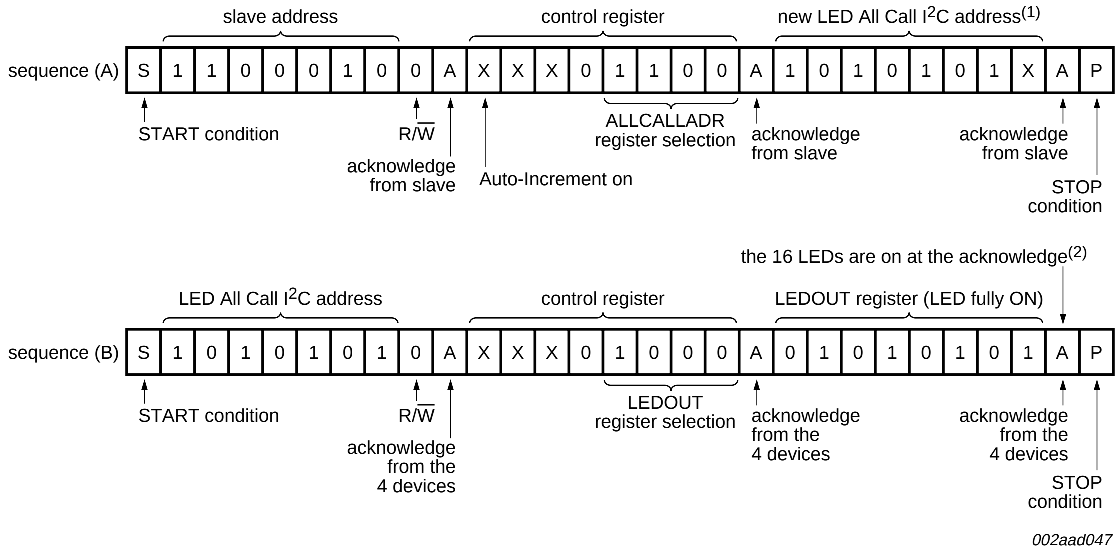


Fig 16. Read all registers using the Auto-Increment feature



(1) ALLCALL bit in MODE1 register is equal to 1 for this example.

(2) OCH bit in MODE2 register is equal to 1 for this example.

Fig 17. LED All Call I2C-bus address programming and LED All Call sequence example

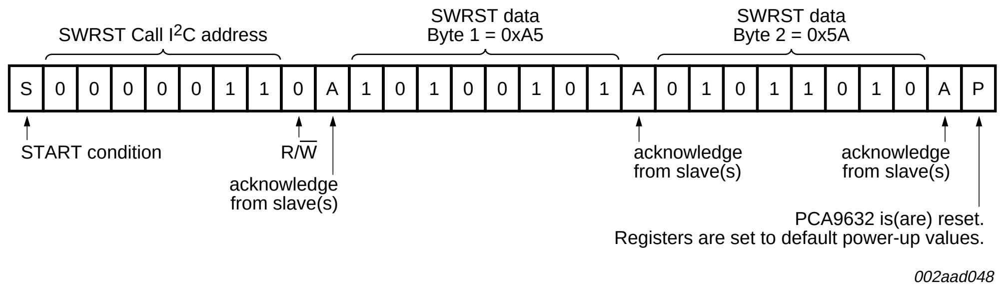
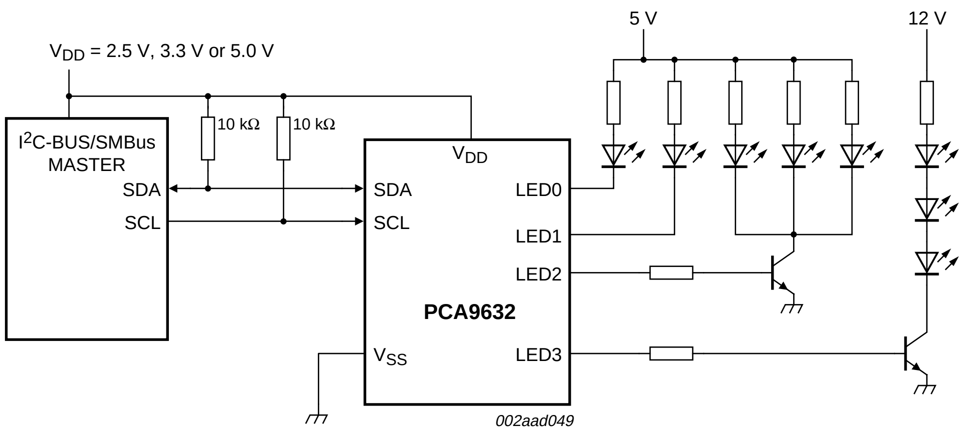


Fig 18. Software Reset (SWRST) Call sequence

10. Application design-in information



I2C-bus address = 1100 010x.

Fig 19. Typical application

11. Limiting values

Table 16. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin		V_{SS} – 0.5	5.5	V
$I_{O(LEDn)}$	output current on pin LEDn		-	25	mA
I_{SS}	ground supply current		-	100	mA
P_{tot}	total power dissipation		-	400	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

12. Static characteristics

Table 17. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage			2.3	-	5.5	V
I_{DD}	supply current	operating mode; no load; f_{SCL} = 0 MHz					
		V_{DD} = 2.3 V		-	38	150	µA
		V_{DD} = 3.3 V		-	53	150	µA
		V_{DD} = 5.5 V		-	108	150	µA
I_{stb}	standby current	no load; f_{SCL} = 0 Hz; I/O = inputs; V_I = V_{DD}					
		V_{DD} = 5.5 V		-	0.005	1	µA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS}	[1]	-	1.70	2.0	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 2.3 V		20	-	-	mA
		V_{OL} = 0.4 V; V_{DD} = 5.0 V		30	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	6	10	pF
LED driver outputs							
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 2.3 V	[2]	12	-	-	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V	[2]	17	-	-	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V	[2]	25	-	-	mA
$I_{OL(tot)}$	total LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 4.5 V	[2]	-	-	100	mA
V_{OH}	HIGH-level output voltage	I_{OH} = −10 mA; V_{DD} = 2.3 V		1.6	-	-	V
		I_{OH} = −10 mA; V_{DD} = 3.0 V		2.3	-	-	V
		I_{OH} = −10 mA; V_{DD} = 4.5 V		4.0	-	-	V
C_o	output capacitance			-	2.5	5	pF

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

[2] Each bit must be limited to a maximum of 25 mA and the total package limited to 100 mA due to internal busing limits.

13. Dynamic characteristics

Table 18. Dynamic characteristics

Symbol	Parameter	Conditions	Standard- mode I²C-bus		Fast-mode I²C-bus		Fast-mode Plus I²C-bus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	[1]	0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[2]	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{VD;DAT}$	data valid time	[3]	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
t_f	fall time of both SDA and SCL signals	[5][6]	-	300	$20 + 0.1C_b$[4]	300	-	120	ns
t_r	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$[4]	300	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[7]	-	50	-	50	-	50	ns

[1] Minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either SDA or SCL is held LOW for a minimum of 25 ms. Disable bus time-out feature for DC operation.

[2] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[3] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[4] C_b = total capacitance of one bus line in pF.

[5] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to Table 17, V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t_f) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

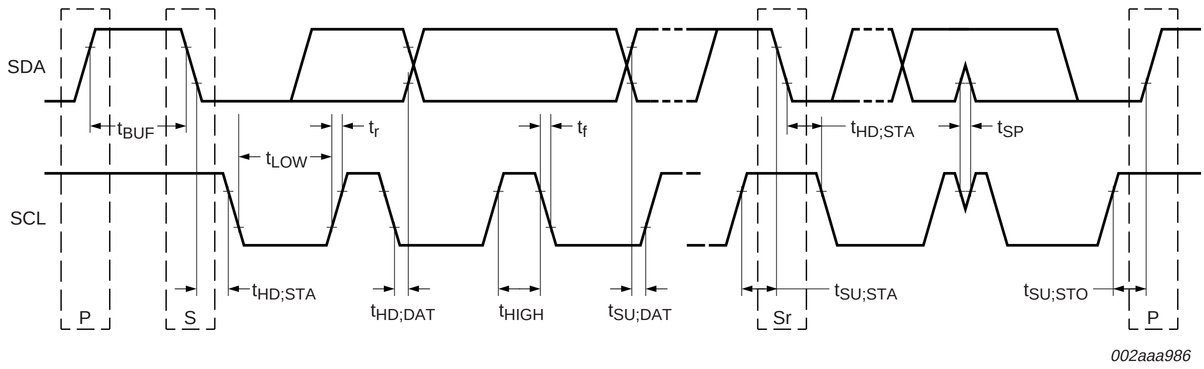
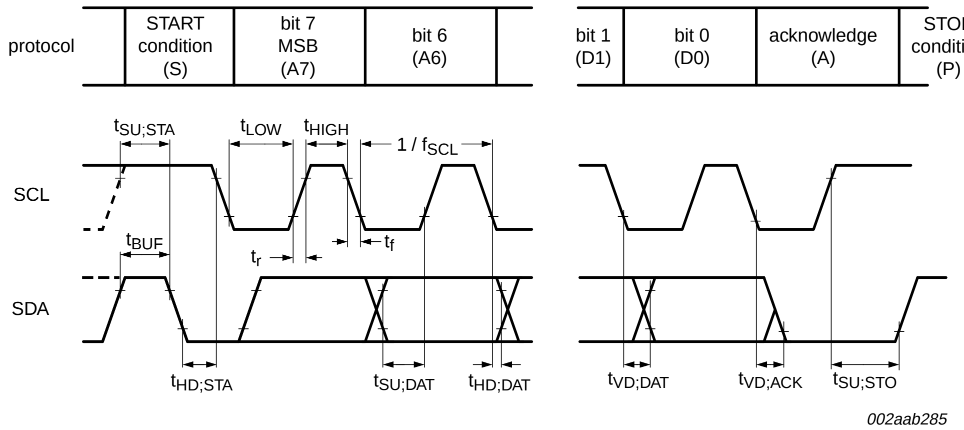


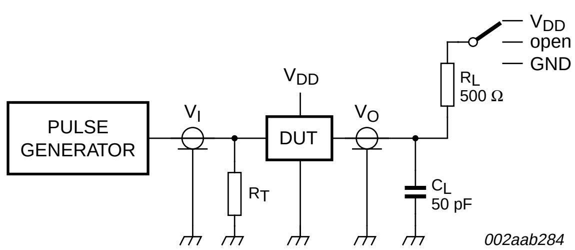
Fig 20. Definition of timing



Rise and fall times refer to V_{IL} and V_{IH}.

Fig 21. I²C-bus timing diagram

14. Test information



R_L = Load resistor for LEDn. R_L for SDA and SCL > 1 kΩ (3 mA or less current).

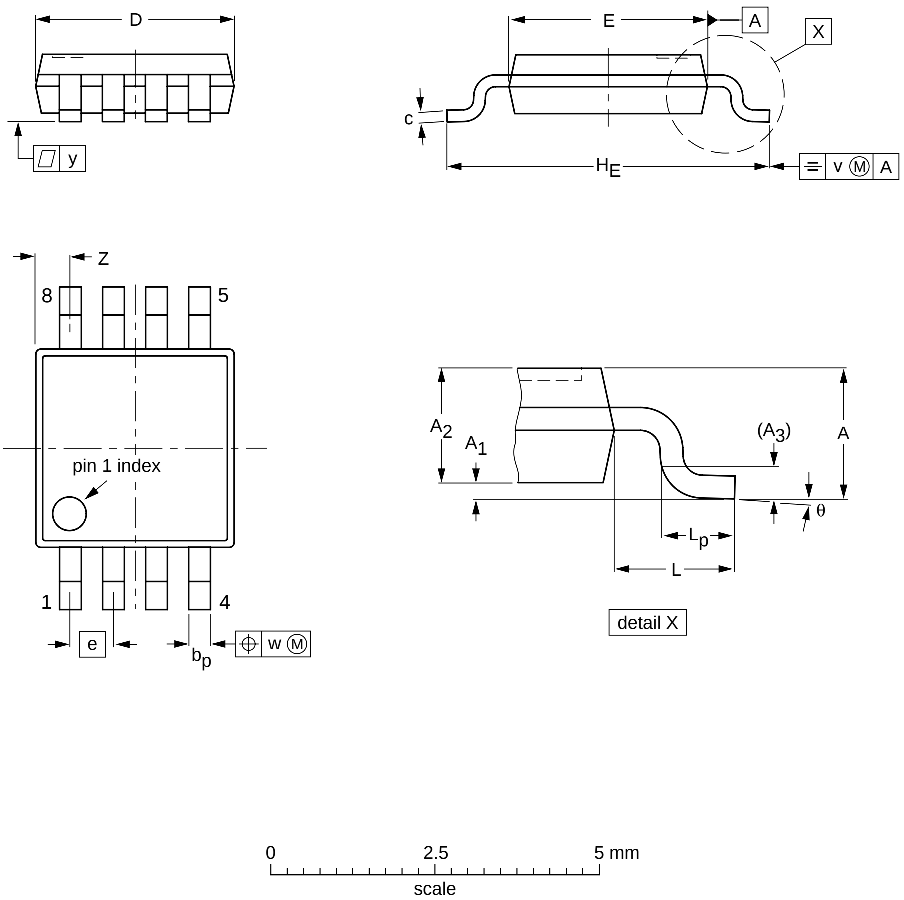
C_L = Load capacitance includes jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generators.

Fig 22. Test circuitry for switching times

15. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

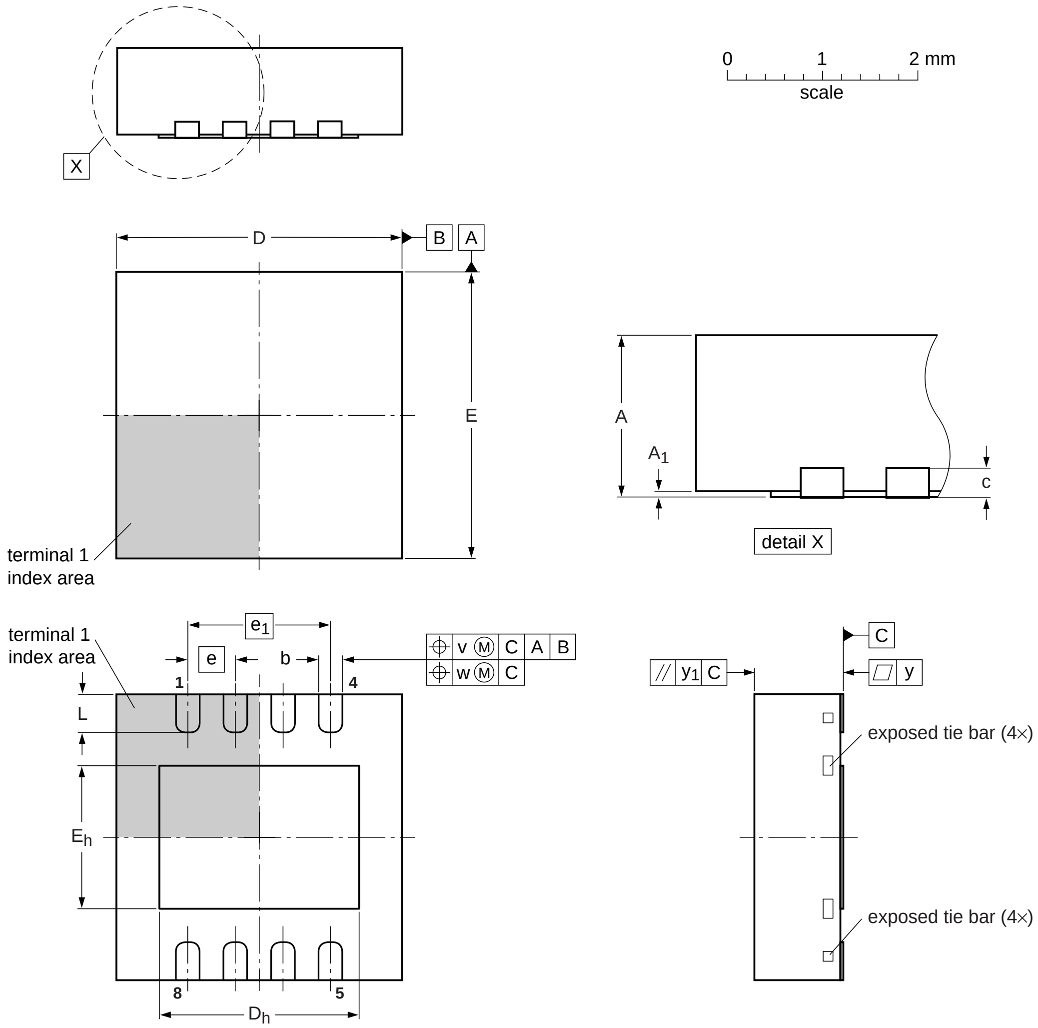
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 23. Package outline SOT505-1 (TSSOP8)

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm **SOT908-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	L	v	w	y	y1
mm	1	0.05 0.00	0.3 0.2	0.2	3.1 2.9	2.25 1.95	3.1 2.9	1.65 1.35	0.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT908-1		MO-229				~~05-09-26~~ 05-10-05

Fig 24. Package outline SOT908-1 (HVSON8)

16. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

17. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 25) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 19 and 20

Table 19. SnPb eutectic process (from J-STD-020C)

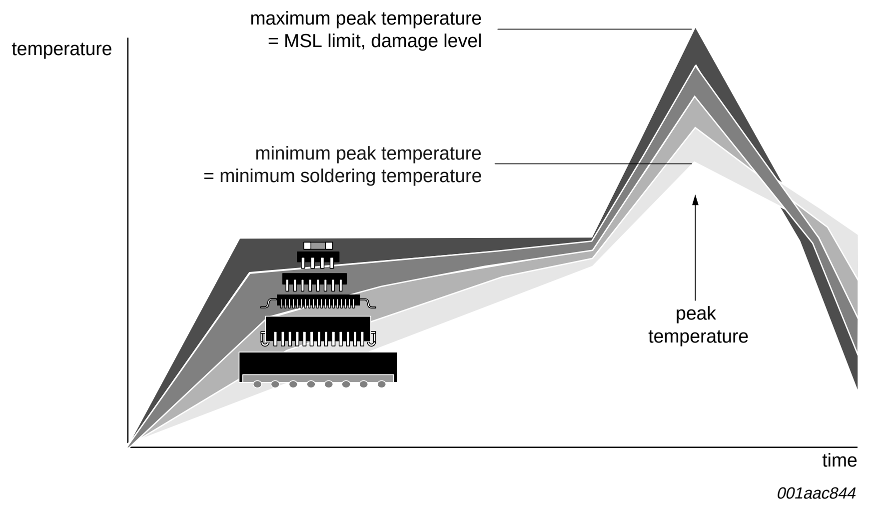
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 20. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 25.



MSL: Moisture Sensitivity Level

Fig 25. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

18. Abbreviations

Table 21. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
NMOS	Negative-channel Metal Oxide Semiconductor
PCB	Printed-Circuit Board
PMOS	Positive-channel Metal Oxide Semiconductor
PWM	Pulse Width Modulation
RGB	Red/Green/Blue
RGBA	Red/Green/Blue/Amber
SMBus	System Management Bus

19. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9632_1	20070928	Objective data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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