



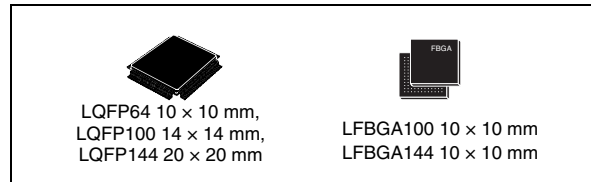
STM32F103xC STM32F103xD STM32F103xE

Performance line, ARM-based 32-bit MCU with up to 512 KB Flash,
USB, CAN, 11 timers, 3 ADCs and 13 communication interfaces

Preliminary Data

Features

- Core: ARM 32-bit Cortex™-M3 CPU
 - 72 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
 - Single-cycle multiplication and hardware division
- Memories
 - 256-to-512 Kbytes of Flash memory
 - up to 64 Kbytes of SRAM
 - Flexible static memory controller with 4 Chip Select. Supports Compact Flash, SRAM, PSRAM, NOR and NAND memories
 - LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
 - 2.0 to 3.6 V application supply and I/Os
 - POR, PDR, and programmable voltage detector (PVD)
 - 4-to-16 MHz crystal oscillator
 - Internal 8 MHz factory-trimmed RC
 - Internal 40 kHz RC with calibration
 - 32 kHz oscillator for RTC with calibration
- Low power
 - Sleep, Stop and Standby modes
 - V_{BAT} supply for RTC and backup registers
- 3 × 12-bit, 1 μ s A/D converters (up to 21 channels)
 - Conversion range: 0 to 3.6 V
 - Triple-sample and hold capability
 - Temperature sensor
- 2-channel 12-bit D/A converter
- DMA: 12-channel DMA controller
 - Supported peripherals: timers, ADCs, DAC, SDIO, I²Ss, SPIs, I²Cs and USARTs
- Debug mode
 - Serial wire debug (SWD) & JTAG interfaces
 - Cortex-M3 Embedded Trace Macrocell™



- Up to 112 fast I/O ports
 - 51/80/112 I/Os, all mappable on 16 external interrupt vectors, all 5 V-tolerant except for analog inputs
- Up to 11 timers
 - Up to four 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter
 - 2 × 16-bit, 6-channel timers with PWM output and dead-time generation
 - 2 × watchdog timers (Independent and Window)
 - SysTick timer: a 24-bit downcounter
 - 2 × 16-bit basic timers to drive the DAC
- Up to 13 communication interfaces
 - Up to 2 × I²C interfaces (SMBus/PMBus)
 - Up to 5 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
 - Up to 3 SPIs (18 Mbit/s), 2 with I²S interface multiplexed
 - CAN interface (2.0B Active)
 - USB 2.0 full speed interface
 - SDIO interface
- CRC calculation unit, 96-bit unique ID
- ECOPACK® packages

Table 1. Device summary

Reference	Part number
STM32F103xC	STM32F103RC STM32F103VC STM32F103ZC
STM32F103xD	STM32F103RD STM32F103VD STM32F103ZD
STM32F103xE	STM32F103RE STM32F103ZE STM32F103VE

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103xC, STM32F103xD and STM32F103xE High-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xx family, please refer to [Section 2.2: Full compatibility throughout the family](#).

The High-density STM32F103xx datasheet should be read in conjunction with the Medium- and High-density STM32F10xxx reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual*.

The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: <http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/>.

2 Description

The STM32F103xC, STM32F103xD and STM32F103xE performance line family incorporates the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 512 Kbytes and SRAM up to 64 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer three 12-bit ADCs, four general purpose 16-bit timers plus two PWM timer, as well as standard and advanced communication interfaces: up to two I²Cs, three SPIs, two I2Ss, one SDIO, five USARTs, an USB and a CAN.

The STM32F103xx High-density performance line family operates in the -40 to +105 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx High-density performance line family offers devices in 5 different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx High-density performance line microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical and handheld equipment
- PC peripherals gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

[Figure 1](#) shows the general block diagram of the device family.

2.1 Device overview

Table 2. STM32F103xC, STM32F103xD and STM32F103xE features and peripheral counts

Peripherals		STM32F103Rx			STM32F103Vx			STM32F103Zx		
Flash memory in Kbytes		256	384	512	256	384	512	256	384	512
SRAM in Kbytes		48	64		48	64		48	64	
FSMC		No			Yes			Yes		
Timers	General-purpose	4								
	Advanced-control	2								
	Basic	2								
Comm	SPI(I ² S) ⁽¹⁾	3(2)								
	I ² C	2								
	USART	5								
	USB	1								
	CAN	1								
	SDIO	1								
GPIOs		51			80			112		
12-bit ADC		3			3			3		
Number of channels		16			16			21		
12-bit DAC		1								
Number of channels		2								
CPU frequency		72 MHz								
Operating voltage		2.0 to 3.6 V								
Operating temperatures		Ambient temperatures: -40 to +85 °C / -40 to +105 °C (see Table 9) Junction temperature: -40 to + 125 °C (see Table 9)								
Package		LQFP64			LQFP100 ⁽²⁾ , BGA100			LQFP144, BGA144		

1. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I²S audio mode.
2. For the LQFP100 and BGA100 packages, only FSMC Bank1 and Bank2 are available. Bank1 can only support a multiplexed NOR Flash memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.



2.2 Full compatibility throughout the family

The STM32F103xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F103x6, STM32F103x8 and STM32F103xB are referred to as Medium-density devices, while the STM32F103xC, STM32F103xD and STM32F103xE are referred to as High-density devices. High-density devices are an extension of the Medium-density STM32F103x6/8/B/C devices specified in the STM32F103xx datasheet.

High-density STM32F103xx devices feature higher Flash memory and RAM capacities, and additional peripherals like SDIO, FSMC, I²S and DAC, while remaining fully compatible with the other members of the family.

The STM32F103xC, STM32F103xD and STM32F103xE are a drop-in replacement for the STM32F103x6/8/A/B/C devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Table 3. STM32F103xx family

Pinout	Memory size					
	Medium-density STM32F103xx devices			High-density STM32F103xx devices		
	32 KB Flash	64 KB Flash	128 KB Flash	256 KB Flash	384 KB Flash	512 KB Flash
	10 KB RAM	20 KB RAM	20 KB RAM	48 KB RAM	64 KB RAM	64 KB RAM
144				5 × USARTs		
100				4 × 16-bit timers, 2 × basic timers		
64	2 × USARTs 2 × 16-bit timers 1 × SPI, 1 × I ² C, USB, CAN, 1 × PWM timer	3 × USARTs 3 × 16-bit timers 2 × SPIs, 2 × I ² Cs, USB, CAN, 1 × PWM timer		3 × SPIs, 2 × I ² Ss, 2 × I ² Cs USB, CAN, 2 × PWM timers 3 × ADCs, 1 × DAC, 1 × SDIO FSMC (100- and 144-pin packages ⁽¹⁾)		
48	1 × ADC	1 × ADC				
36	1 × ADC					

1. Ports F and G are not available in devices delivered in 100-pin packages.

2.3 Overview

ARM[®] Cortex[™]-M3 core with embedded Flash and SRAM

The ARM Cortex[™]-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex[™]-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM core, STM32F103xC, STM32F103xD and STM32F103xE performance line family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

Embedded Flash memory

Up to 512 Kbytes of embedded Flash is available for storing programs and data.

CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

Embedded SRAM

Up to 64 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

FSMC (flexible static memory controller)

The FSMC is embedded in the STM32F103xC, STM32F103xD and STM32F103xE performance line family. It has four Chip Select outputs supporting the following modes: RAM, PSRAM, NOR and NAND.

Functionality overview:

- The three FSMC interrupt lines are ORed in order to be connected to the NVIC
- Write FIFO
- Code execution from external memory except for
- The targeted frequency is $\text{SYSCLK}/2$, so external access is at 36 MHz when the system is at 72 MHz and external access is at 24 MHz when the system is at 48 MHz

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

Nested vectored interrupt controller (NVIC)

The STM32F103xC, STM32F103xD and STM32F103xE performance line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See [Figure 2](#) for details on the clock tree.

Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1.

Power supply schemes

- $V_{DD} = 2.0$ to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 2.0$ to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- $V_{BAT} = 1.8$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to [Figure 11: Power supply scheme](#).

Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to [Table 11: Embedded reset and power control block characteristics](#) for the values of $V_{POR/PDR}$ and V_{PVD} .

Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

Low-power modes

The STM32F103xC, STM32F103xD and STM32F103xE performance line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**
Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.
The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, general-purpose, basic and advanced control timers TIMx, DAC, I²S, SDIO and ADC.

RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

General-purpose timers (TIMx)

There are up to 4 synchronizable standard timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F103xC, STM32F103xD and STM32F103xE performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages. They can work together with the Advanced Control timer via the Timer Link feature for synchronization or event chaining.

The counter can be frozen in debug mode.

Any of the standard timers can be used to generate PWM outputs. Each of the timers has independent DMA request generations.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Advanced control timers (TIM1 and TIM8)

The two advanced control timers (TIM1 and TIM8) can each be seen as a three-phase PWM multiplexed on 6 channels. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for

- Input Capture
- Output Compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output
- Complementary PWM outputs with programmable inserted dead-times.

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F103xC, STM32F103xD and STM32F103xE performance line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

Inter-integrated sound (I²S)

Two standard I²S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 48 kHz are supported. When either or both of the I²S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with SD Memory Card Specifications Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is also fully compliant with the CE-ATA digital protocol Rev1.1.

Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

Universal serial bus (USB)

The STM32F103xC, STM32F103xD and STM32F103xE performance line embed a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed

ADC (analog to digital converter)

Three 12-bit analog-to-digital converters are embedded into STM32F103xC, STM32F103xD and STM32F103xE performance line devices and each ADC shares up to 21 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the standard timers (TIMx) and the advanced-control timers (TIM1 and TIM8) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32F103xC, STM32F103xD and STM32F103xE performance line family. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

Temperature sensor

The temperature sensor has to generate a linear voltage with any variation in temperature. The conversion range is between $2\text{ V} < V_{DDA} < 3.6\text{ V}$. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

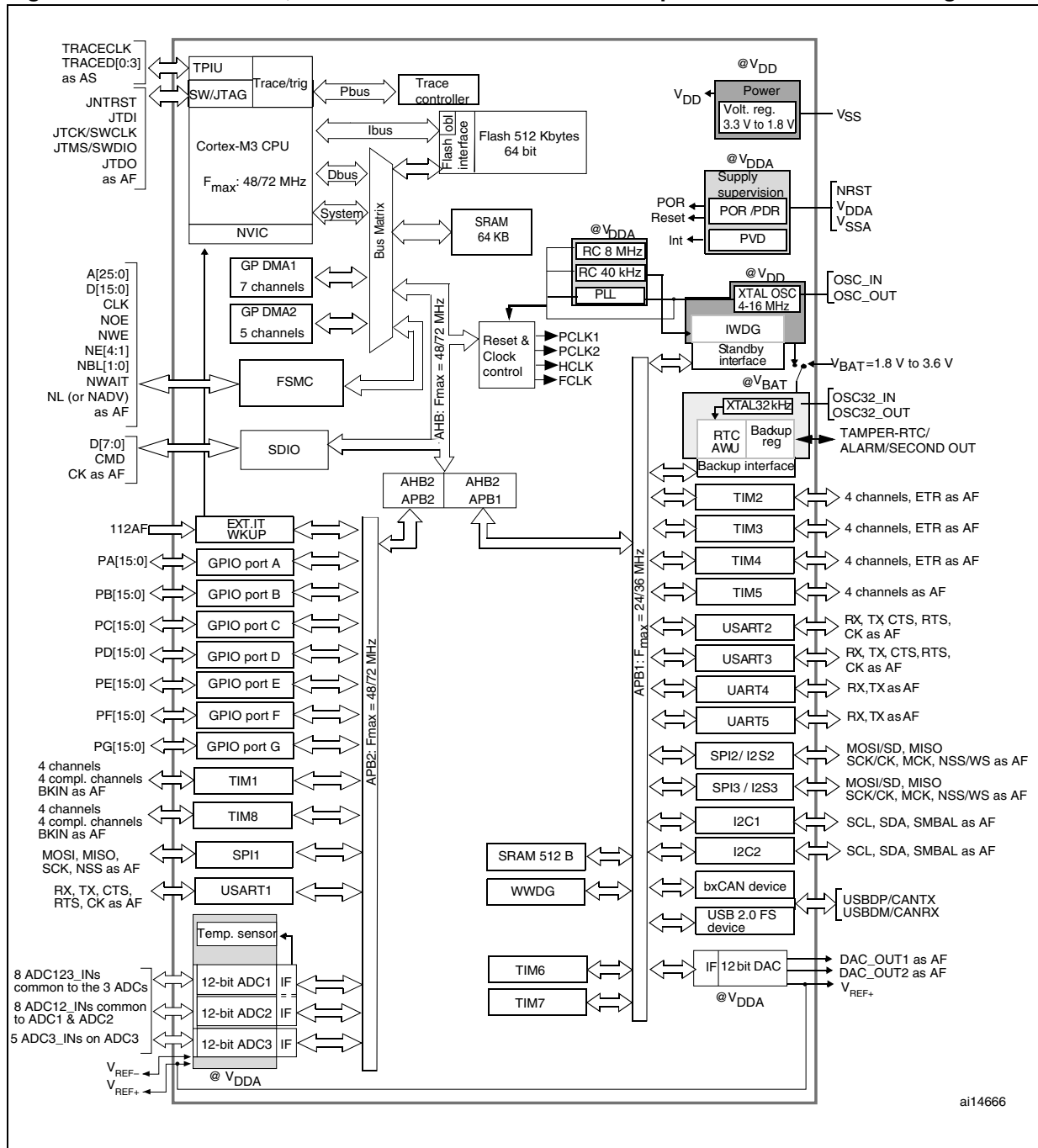
Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Embedded Trace Macrocell™

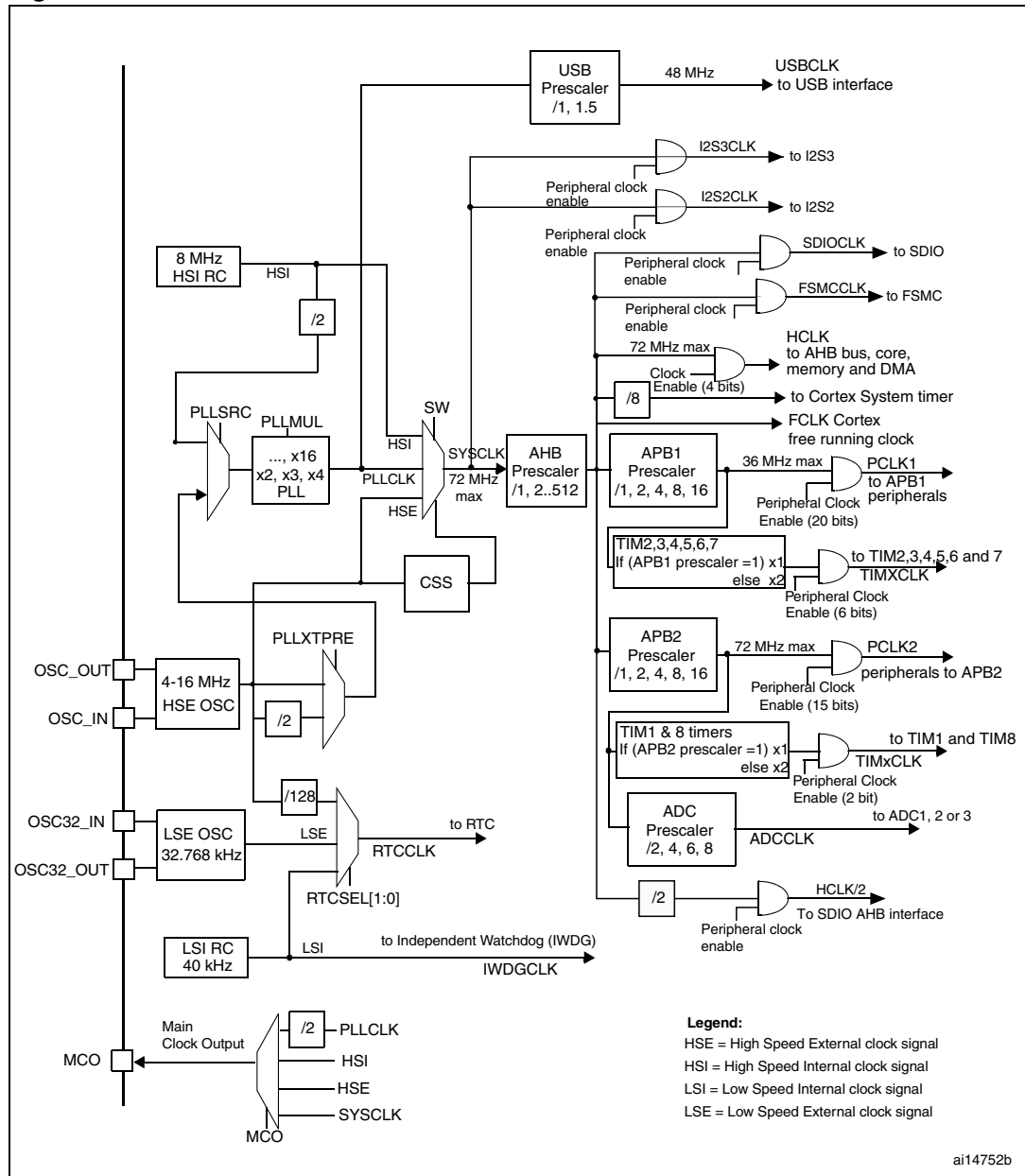
The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Figure 1. STM32F103xC, STM32F103xD and STM32F103xE performance line block diagram



1. $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ (suffix 6, see [Table 69](#)) or $-40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$ (suffix 7, see [Table 69](#)), junction temperature up to $105\text{ }^\circ\text{C}$ or $125\text{ }^\circ\text{C}$, respectively.
2. AF = alternate function on I/O port pin.

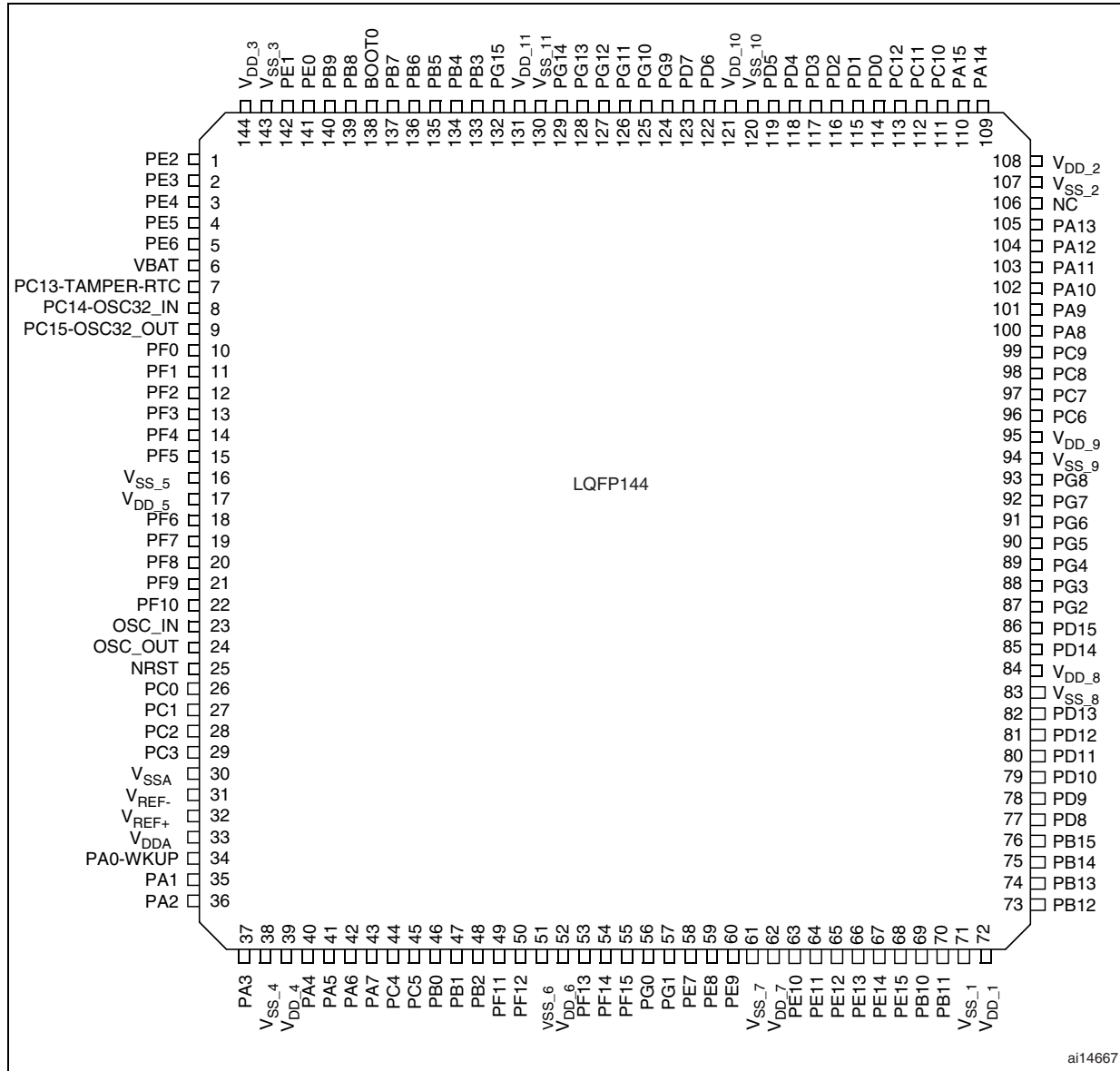
Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 48 MHz or 72 MHz.
3. To have an ADC conversion time of 1 μ s, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

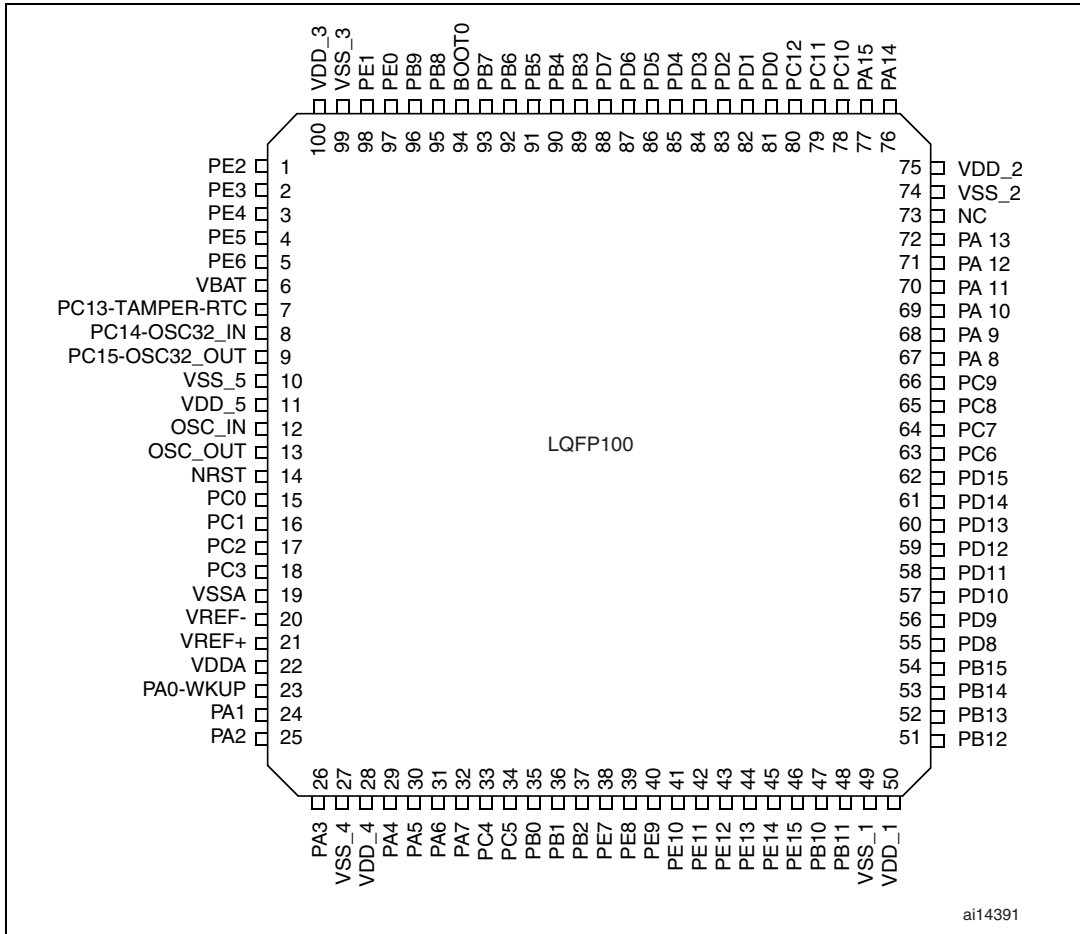
3 Pin descriptions

Figure 3. STM32F103xC, STM32F103xD and STM32F103xE performance line LQFP144 pinout



ai14667

Figure 4. STM32F103xC, STM32F103xD and STM32F103xE performance line LQFP100 pinout



ai14391

Figure 5. STM32F103xC, STM32F103xD and STM32F103xE performance line LQFP64 pinout

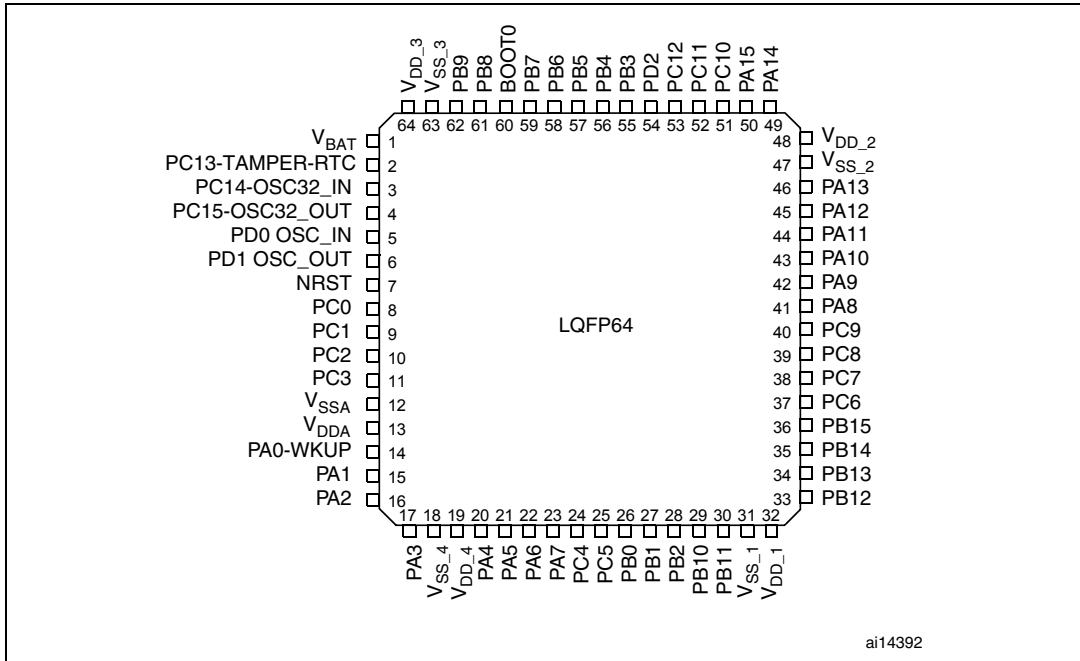
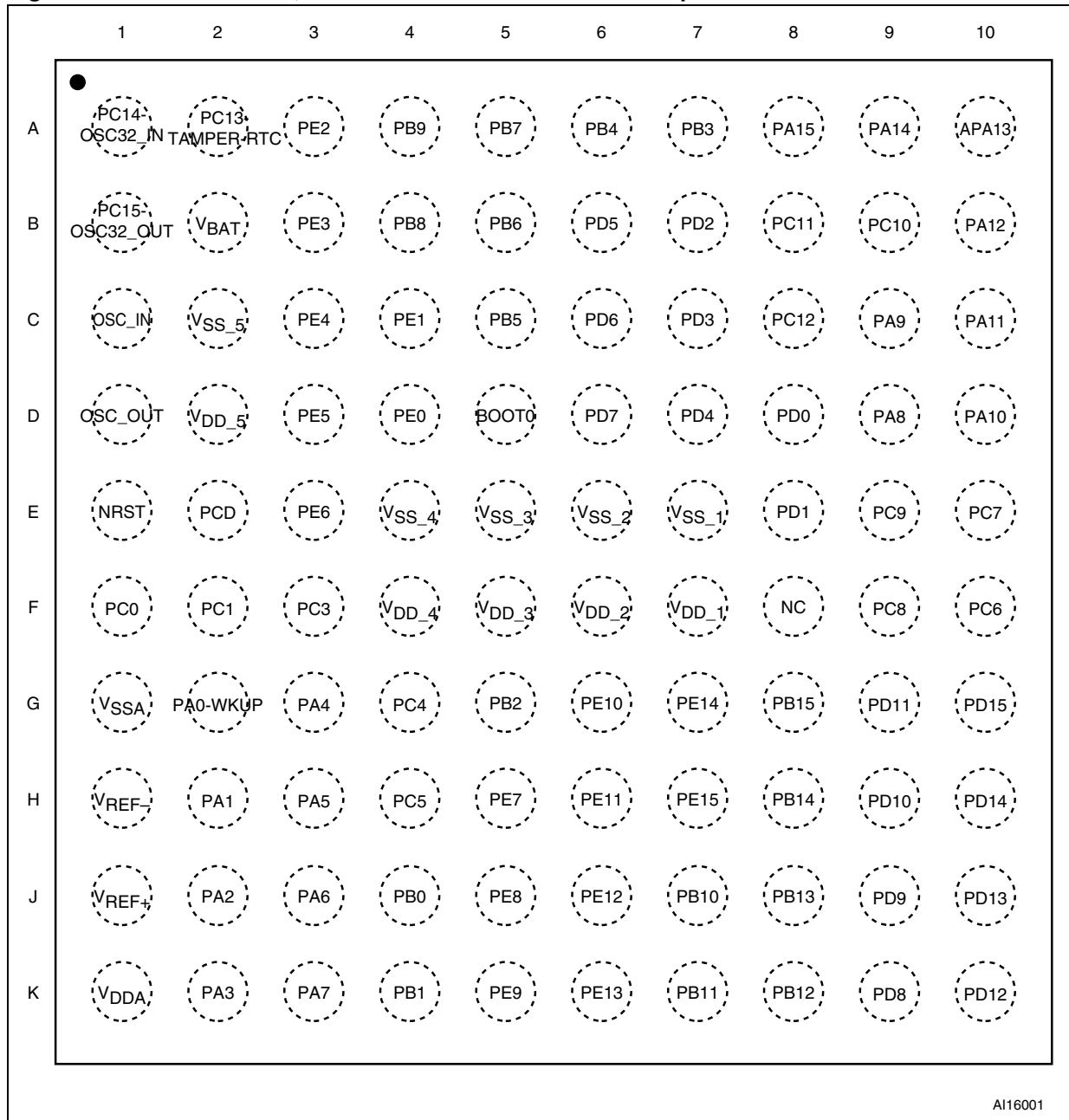
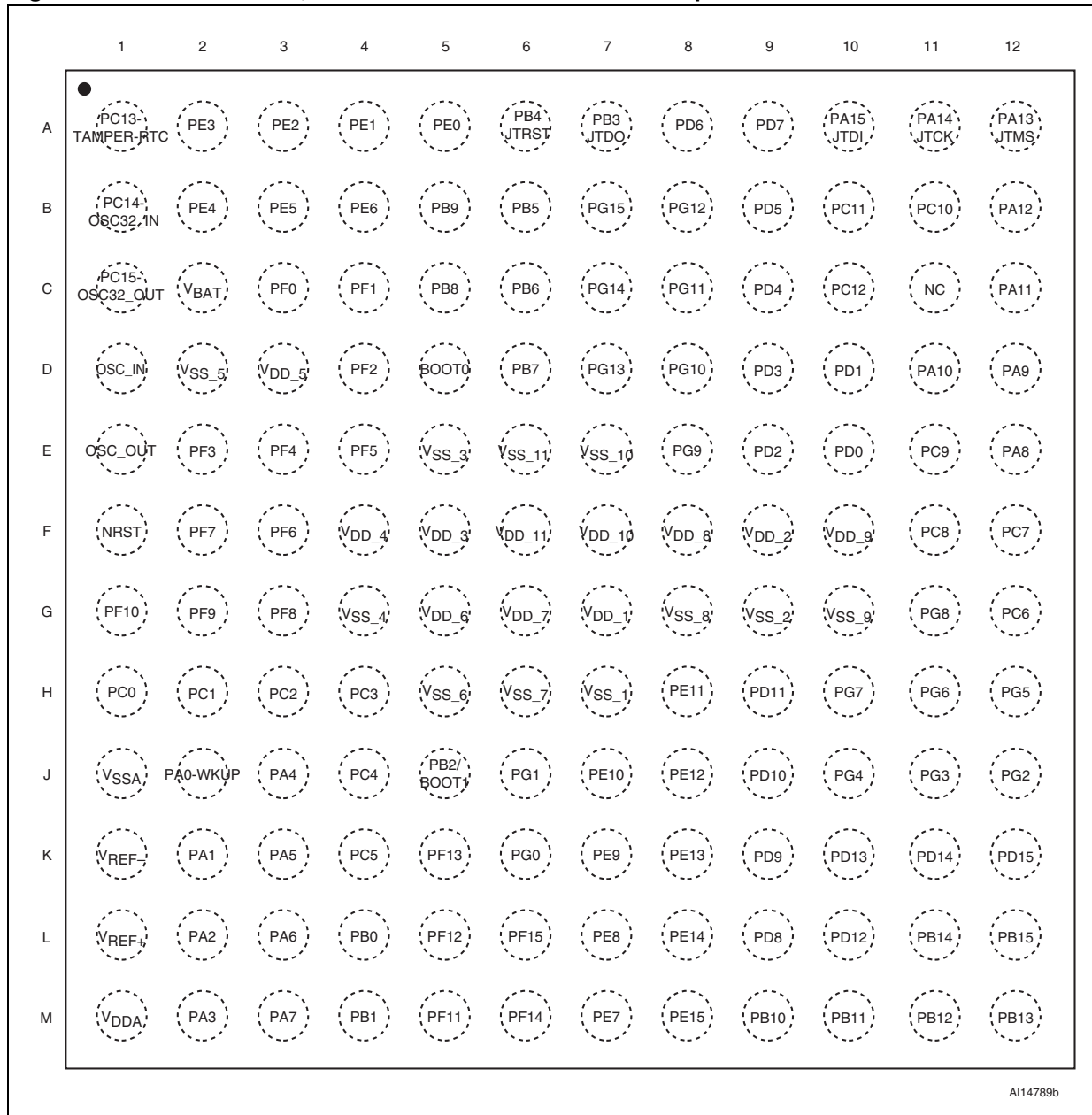


Figure 6. STM32F103xC, STM32F103xD and STM32F103xE performance line BGA100 ballout



AI16001

Figure 7. STM32F103xC, STM32F103xD and STM32F103xE performance line BGA144 ballout



A114789b

Table 4. Pin definitions

Pins					Pin name	Type ⁽¹⁾	I/O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions	
BGA144	BGA100	LQFP64	LQFP100	LQFP144					Default	Remap
A3	A3	-	1	1	PE2	I/O	FT	PE2	TRACECK/ FSMC_A23	
A2	B3	-	2	2	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	
B2	C3	-	3	3	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	
B3	D3	-	4	4	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	
B4	E3	-	5	5	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	
C2	B2	1	6	6	V _{BAT}	S		V _{BAT}		
A1	A2	2	7	7	PC13-TAMPER-RTC ⁽⁴⁾	I/O		PC13 ⁽⁵⁾	TAMPER-RTC	
B1	A1	3	8	8	PC14-OSC32_IN ⁽⁴⁾	I/O		PC14 ⁽⁵⁾	OSC32_IN	
C1	B1	4	9	9	PC15-OSC32_OUT ⁽⁴⁾	I/O		PC15 ⁽⁵⁾	OSC32_OUT	
C3	-	-	-	10	PF0	I/O	FT	PF0	FSMC_A0	
C4	-	-	-	11	PF1	I/O	FT	PF1	FSMC_A1	
D4	-	-	-	12	PF2	I/O	FT	PF2	FSMC_A2	
E2	-	-	-	13	PF3	I/O	FT	PF3	FSMC_A3	
E3	-	-	-	14	PF4	I/O	FT	PF4	FSMC_A4	
E4	-	-	-	15	PF5	I/O	FT	PF5	FSMC_A5	
D2	C2	-	10	16	V _{SS_5}	S		V _{SS_5}		
D3	D2	-	11	17	V _{DD_5}	S		V _{DD_5}		
F3	-	-	-	18	PF6	I/O		PF6	ADC3_IN4/ FSMC_NIORD	
F2	-	-	-	19	PF7	I/O		PF7	ADC3_IN5/ FSMC_NREG	
G3	-	-	-	20	PF8	I/O		PF8	ADC3_IN6/ FSMC_NIOWR	
G2	-	-	-	21	PF9	I/O		PF9	ADC3_IN7/ FSMC_CD	
G1	-	-	-	22	PF10	I/O		PF10	ADC3_IN8/ FSMC_INTR	
D1	C1	5	12	23	OSC_IN	I		OSC_IN		
E1	D1	6	13	24	OSC_OUT	O		OSC_OUT		
F1	E1	7	14	25	NRST	I/O		NRST		
H1	F1	8	15	26	PC0	I/O		PC0	ADC123_IN10	
H2	F2	9	16	27	PC1	I/O		PC1	ADC123_IN11	
H3	E2	10	17	28	PC2	I/O		PC2	ADC123_IN12	

Table 4. Pin definitions (continued)

Pins					Pin name	Type ⁽¹⁾	I/O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions	
BGA144	BGA100	LQFP64	LQFP100	LQFP144					Default	Remap
H4	F3	11	18	29	PC3	I/O		PC3	ADC123_IN13	
J1	G1	12	19	30	V _{SSA}	S		V _{SSA}		
K1	H1	-	20	31	V _{REF-}	S		V _{REF-}		
L1	J1	-	21	32	V _{REF+}	S		V _{REF+}		
M1	K1	13	22	33	V _{DDA}	S		V _{DDA}		
J2	G2	14	23	34	PA0-WKUP	I/O		PA0	WKUP/USART2_CTS ⁽⁶⁾ ADC123_IN0 TIM2_CH1_ETR TIM5_CH1/TIM8_ETR	
K2	H2	15	24	35	PA1	I/O		PA1	USART2_RTS ⁽⁶⁾ ADC123_IN1/TIM5_CH2 TIM2_CH2 ⁽⁶⁾	
L2	J2	16	25	36	PA2	I/O		PA2	USART2_TX ⁽⁶⁾ / TIM5_CH3/ADC123_IN2/ TIM2_CH3 ⁽⁶⁾	
M2	K2	17	26	37	PA3	I/O		PA3	USART2_RX ⁽⁶⁾ / TIM5_CH4/ADC123_IN3 TIM2_CH4 ⁽⁶⁾	
G4	E4	18	27	38	V _{SS_4}	S		V _{SS_4}		
F4	F4	19	28	39	V _{DD_4}	S		V _{DD_4}		
J3	G3	20	29	40	PA4	I/O		PA4	SPI1_NSS ⁽⁶⁾ /DAC_OUT1 USART2_CK ⁽⁶⁾ ADC12_IN4	
K3	H3	21	30	41	PA5	I/O		PA5	SPI1_SCK ⁽⁶⁾ DAC_OUT2 ADC12_IN5	
L3	J3	22	31	42	PA6	I/O		PA6	SPI1_MISO ⁽⁶⁾ TIM8_BKIN/ADC12_IN6 TIM3_CH1 ⁽⁶⁾	TIM1_BKIN
M3	K3	23	32	43	PA7	I/O		PA7	SPI1_MOSI ⁽⁶⁾ TIM8_CH1N/ADC12_IN7 TIM3_CH2 ⁽⁶⁾	TIM1_CH1N
J4	G4	24	33	44	PC4	I/O		PC4	ADC12_IN14	
K4	H4	25	34	45	PC5	I/O		PC5	ADC12_IN15	
L4	J4	26	35	46	PB0	I/O		PB0	ADC12_IN8/TIM3_CH3 TIM8_CH2N	TIM1_CH2N
M4	K4	27	36	47	PB1	I/O		PB1	ADC12_IN9 TIM3_CH4 ⁽⁶⁾ TIM8_CH3N	TIM1_CH3N
J5	G5	28	37	48	PB2/BOOT1	I/O	FT	PB2/BOOT1		

Table 4. Pin definitions (continued)

Pins					Pin name	Type ⁽¹⁾	I/O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions	
BGA144	BGA100	LQFP64	LQFP100	LQFP144					Default	Remap
M5	-	-	-	49	PF11	I/O			FSMC_NIOS16	
L5	-	-	-	50	PF12	I/O			FSMC_A6	
H5	-	-	-	51	V _{SS_6}	S				
G5	-	-	-	52	V _{DD_6}	S				
K5	-	-	-	53	PF13	I/O			FSMC_A7	
M6	-	-	-	54	PF14	I/O			FSMC_A8	
L6	-	-	-	55	PF15	I/O			FSMC_A9	
K6	-	-	-	56	PG0	I/O			FSMC_A10	
J6	-	-	-	57	PG1	I/O			FSMC_A11	
M7	H5	-	38	58	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
L7	J5	-	39	59	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
K7	K5	-	40	60	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
H6	-	-	-	61	V _{SS_7}	S				
G6	-	-	-	62	V _{DD_7}	S				
J7	G6	-	41	63	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
H8	H6	-	42	64	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
J8	J6	-	43	65	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
K8	K6	-	44	66	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
L8	G7	-	45	67	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
M8	H7	-	46	68	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
M9	J7	29	47	69	PB10	I/O	FT	PB10	I2C2_SCL USART3_TX ⁽⁶⁾	TIM2_CH3
M10	K7	30	48	70	PB11	I/O	FT	PB11	I2C2_SDA USART3_RX ⁽⁶⁾	TIM2_CH4
H7	E7	31	49	71	V _{SS_1}	S		V _{SS_1}		
G7	F7	32	50	72	V _{DD_1}	S		V _{DD_1}		
M11	K8	33	51	73	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/ I2C2_SMBAL/ USART3_CK ⁽⁶⁾ / TIM1_BKIN ⁽⁶⁾	
M12	J8	34	52	74	PB13	I/O	FT	PB13	SPI2_SCK/I2S2_CK USART3_CTS ⁽⁶⁾ / TIM1_CH1N	
L11	H8	35	53	75	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS ⁽⁶⁾	

Table 4. Pin definitions (continued)

Pins					Pin name	Type ⁽¹⁾	I/O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions	
BGA144	BGA100	LQFP64	LQFP100	LQFP144					Default	Remap
L12	G8	36	54	76	PB15	I/O	FT	PB15	SPI2_MOSI/I2S2_SD TIM1_CH3N ⁽⁶⁾	
L9	K9	-	55	77	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
K9	J9	-	56	78	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
J9	H9	-	57	79	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
H9	G9	-	58	80	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
L10	K10	-	59	81	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS
K10	J10	-	60	82	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
G8	-	-	-	83	V _{SS_8}	S				
F8	-	-	-	84	V _{DD_8}	S				
K11	H10	-	61	85	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
K12	G10	-	62	86	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
J12	-	-	-	87	PG2	I/O	FT		FSMC_A12	
J11	-	-	-	88	PG3	I/O	FT		FSMC_A13	
J10	-	-	-	89	PG4	I/O	FT		FSMC_A14	
H12	-	-	-	90	PG5	I/O	FT		FSMC_A15	
H11	-	-	-	91	PG6	I/O	FT		FSMC_INT2	
H10	-	-	-	92	PG7	I/O	FT		FSMC_INT3	
G11	-	-	-	93	PG8	I/O	FT			
G10	-	-	-	94	V _{SS_9}	S				
F10	-	-	-	95	V _{DD_9}	S				
G12	F10	37	63	96	PC6	I/O	FT	PC6	I2S2_MCK/ TIM8_CH1/SDIO_D6	TIM3_CH1
F12	E10	38	64	97	PC7	I/O	FT	PC7	I2S3_MCK/ TIM8_CH2/SDIO_D7	TIM3_CH2
F11	F9	39	65	98	PC8	I/O	FT	PC8	TIM8_CH3/SDIO_D0	TIM3_CH3
E11	E9	40	66	99	PC9	I/O	FT	PC9	TIM8_CH4/SDIO_D1	TIM3_CH4
E12	D9	41	67	100	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1 ⁽⁶⁾ /MCO	
D12	C9	42	68	101	PA9	I/O	FT	PA9	USART1_TX ⁽⁶⁾ / TIM1_CH2 ⁽⁶⁾	
D11	D10	43	69	102	PA10	I/O	FT	PA10	USART1_RX ⁽⁶⁾ / TIM1_CH3 ⁽⁶⁾	

Table 4. Pin definitions (continued)

Pins					Pin name	Type ⁽¹⁾	I/O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions	
BGA144	BGA100	LQFP64	LQFP100	LQFP144					Default	Remap
C12	C10	44	70	103	PA11	I/O	FT	PA11	USART1_CTS/CANRX TIM1_CH4 ⁽⁶⁾ /USBDM	
B12	B10	45	71	104	PA12	I/O	FT	PA12	USART1_RTS/USBDP/ CANTX ⁽⁶⁾ /TIM1_ETR ⁽⁶⁾	
A12	A10	46	72	105	PA13/JTMS-SWDIO	I/O	FT	JTMS-SWDIO	PA13	
C11	F8	-	73	106	Not connected					
G9	E6	47	74	107	V _{SS_2}	S		V _{SS_2}		
F9	F6	48	75	108	V _{DD_2}	S		V _{DD_2}		
A11	A9	49	76	109	PA14/JTCK-SWCLK	I/O	FT	JTCK-SWCLK	PA14	
A10	A8	50	77	110	PA15/JTDI	I/O	FT	JTDI	PA15/SPI3_NSS/ I2S3_WS	TIM2_CH1_ETR SPI1_NSS
B11	B9	51	78	111	PC10	I/O	FT	PC10	UART4_TX/SDIO_D2	USART3_TX
B10	B8	52	79	112	PC11	I/O	FT	PC11	UART4_RX/SDIO_D3	USART3_RX
C10	C8	53	80	113	PC12	I/O	FT	PC12	UART5_TX/SDIO_CK	USART3_CK
E10	D8	5	81	114	PD0	I/O	FT	OSC_IN ⁽⁷⁾	FSMC_D2	CANRX
D10	E8	6	82	115	PD1	I/O	FT	OSC_OUT ⁽⁷⁾	FSMC_D3	CANTX
E9	B7	54	83	116	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX SDIO_CMD	
D9	C7	-	84	117	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
C9	D7	-	85	118	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
B9	B6	-	86	119	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
E7	-	-	-	120	V _{SS_10}	S				
F7	-	-	-	121	V _{DD_10}	S				
A8	C6	-	87	122	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
A9	D6	-	88	123	PD7	I/O	FT	PD7	FSMC_NE1/ FSMC_NCE2	USART2_CK
E8	-	-	-	124	PG9	I/O	FT		FSMC_NE2/ FSMC_NCE3	
D8	-	-	-	125	PG10	I/O	FT		FSMC_NCE4_1/ FSMC_NE3	
C8	-	-	-	126	PG11	I/O	FT		FSMC_NCE4_2	
B8	-	-	-	127	PG12	I/O	FT		FSMC_NE4	
D7	-	-	-	128	PG13	I/O	FT		FSMC_A24	
C7	-	-	-	129	PG14	I/O	FT		FSMC_A25	
E6	-	-	-	130	V _{SS_11}	S				

Table 4. Pin definitions (continued)

Pins					Pin name	Type ⁽¹⁾	I/O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions	
BGA144	BGA100	LQFP64	LQFP100	LQFP144					Default	Remap
F6	-	-	-	131	V _{DD_11}	S				
B7	-	-	-	132	PG15	I/O				
A7	A7	55	89	133	PB3/JTDO	I/O	FT	JTDO	PB3/TRACESWO JTDO SPI3_SCK/I2S3_CK/	TIM2_CH2 / SPI1_SCK
A6	A6	56	90	134	PB4/JNTRST	I/O	FT	JNTRST	PB4/SPI3_MISO	TIM3_CH1 / SPI1_MISO
B6	C5	57	91	135	PB5	I/O		PB5	I2C1_SMBAL/ SPI3_MOSI/I2S3_SD	TIM3_CH2 / SPI1_MOSI
C6	B5	58	92	136	PB6	I/O	FT	PB6	I2C1_SCL ⁽⁶⁾ / TIM4_CH1 ⁽⁶⁾	USART1_TX
D6	A5	59	93	137	PB7	I/O	FT	PB7	I2C1_SDA ⁽⁶⁾ / FSMC_NADV/ TIM4_CH2 ⁽⁶⁾	USART1_RX
D5	D5	60	94	138	BOOT0	I		BOOT0		
C5	B4	61	95	139	PB8	I/O	FT	PB8	TIM4_CH3 ⁽⁶⁾ /SDIO_D4	I2C1_SCL/ CANRX
B5	A4	62	96	140	PB9	I/O	FT	PB9	TIM4_CH4 ⁽⁶⁾ /SDIO_D5	I2C1_SDA / CANTX
A5	D4	-	97	141	PE0	I/O	FT	PE0	TIM4_ETR FSMC_NBL0	
A4	C4	-	98	142	PE1	I/O	FT	PE1	FSMC_NBL1	
E5	E5	63	99	143	V _{SS_3}	S		V _{SS_3}		
F5	F5	64	100	144	V _{DD_3}	S		V _{DD_3}		

1. I = input, O = output, S = supply, HiZ = high impedance.

2. FT = 5 V tolerant.

3. Function availability depends on the chosen device.

4. PC13, PC14 and PC15 are supplied through the power switch, and so their use in output mode is limited: they can be used only in output 2 MHz mode with a maximum load of 30 pF and only one pin can be put in output mode at a time.

5. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

6. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

7. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100/BGA100 and LQFP144/BGA144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.

Table 5. FSMC pin definition

Pins	FSMC					LQFP100 BGA100 ⁽¹⁾
	CF	CF/IDE	NOR/PSRAM	NOR/SRAM Mux	NAND 16 bit	
PE2			A23	A23		Yes
PE3			A19	A19		Yes
PE4			A20	A20		Yes
PE5			A21	A21		Yes
PE6			A22	A22		Yes
PF0	A0	A0	A0			-
PF1	A1	A1	A1			-
PF2	A2	A2	A2			-
PF3	A3		A3			-
PF4	A4		A4			-
PF5	A5		A5			-
PF6	NIORD	NIORD				-
PF7	NREG	NREG				-
PF8	NIOWR	NIOWR				-
PF9	CD	CD				-
PF10	INTR	INTR				-
PF11	NIOS16	NIOS16				-
PF12	A6		A6			-
PF13	A7		A7			-
PF14	A8		A8			-
PF15	A9		A9			-
PG0	A10		A10			-
PG1			A11			-
PE7	D4	D4	D4	DA4	D4	Yes
PE8	D5	D5	D5	DA5	D5	Yes
PE9	D6	D6	D6	DA6	D6	Yes
PE10	D7	D7	D7	DA7	D7	Yes
PE11	D8	D8	D8	DA8	D8	Yes
PE12	D9	D9	D9	DA9	D9	Yes
PE13	D10	D10	D10	DA10	D10	Yes
PE14	D11	D11	D11	DA11	D11	Yes
PE15	D12	D12	D12	DA12	D12	Yes
PD8	D13	D13	D13	DA13	D13	Yes

Table 5. FSMC pin definition (continued)

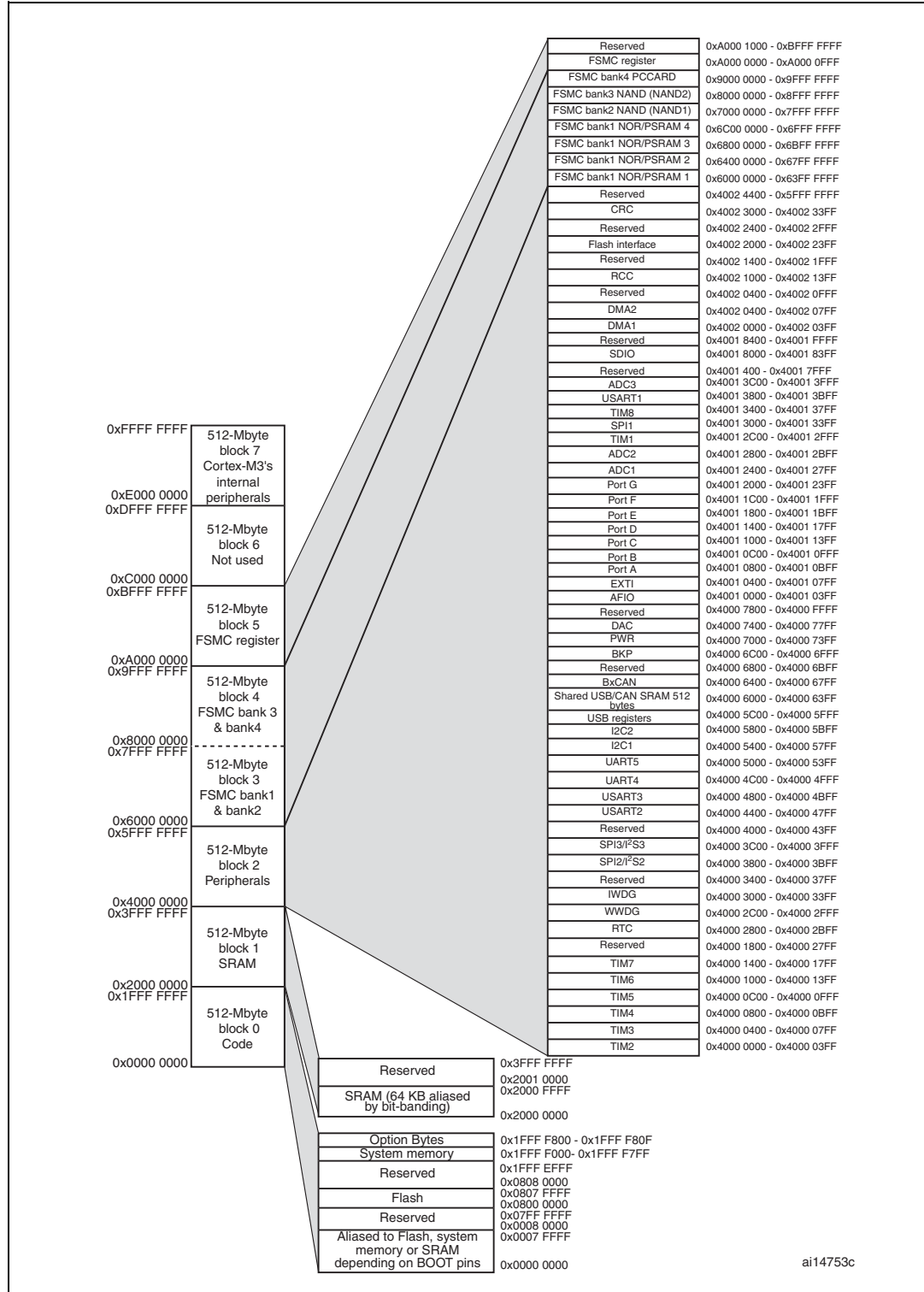
Pins	FSMC					LQFP100 BGA100 ⁽¹⁾
	CF	CF/IDE	NOR/PSRAM	NOR/SRAM Mux	NAND 16 bit	
PD9	D14	D14	D14	DA14	D14	Yes
PD10	D15	D15	D15	DA15	D15	Yes
PD11			A16	A16	CLE	Yes
PD12			A17	A17	ALE	Yes
PD13			A18	A18		Yes
PD14	D0	D0	D0	DA0	D0	Yes
PD15	D1	D1	D1	DA1	D1	Yes
PG2			A12			-
PG3			A13			-
PG4			A14			-
PG5			A15			-
PG6					INT2	-
PG7					INT3	-
PD0	D2	D2	D2	DA2	D2	Yes
PD1	D3	D3	D3	DA3	D3	Yes
PD3			CLK	CLK		Yes
PD4	NOE	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7			NE1	NE1	NCE2	Yes
PG9			NE2	NE2	NCE3	-
PG10	NCE4_1	NCE4_1	NE3	NE3		-
PG11	NCE4_2	NCE4_2				-
PG12			NE4	NE4		-
PG13			A24	A24		-
PG14			A25	A25		Yes
PB7			NADV	NADV		Yes
PE0			NBL0	NBL0		Yes
PE1			NBL1	NBL1		Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

4 Memory mapping

The memory map is shown in *Figure 8*.

Figure 8. Memory map



5 Electrical characteristics

5.1 Test conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ °C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean} \pm 3\sigma$).

5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ °C}$, $V_{DD} = 3.3\text{ V}$ (for the $2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean} \pm 2\sigma$).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 9](#).

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 10](#).

Figure 9. Pin loading conditions

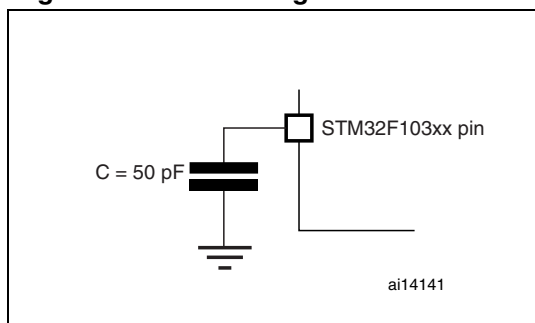
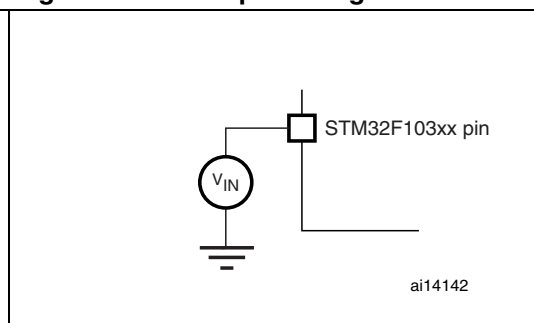
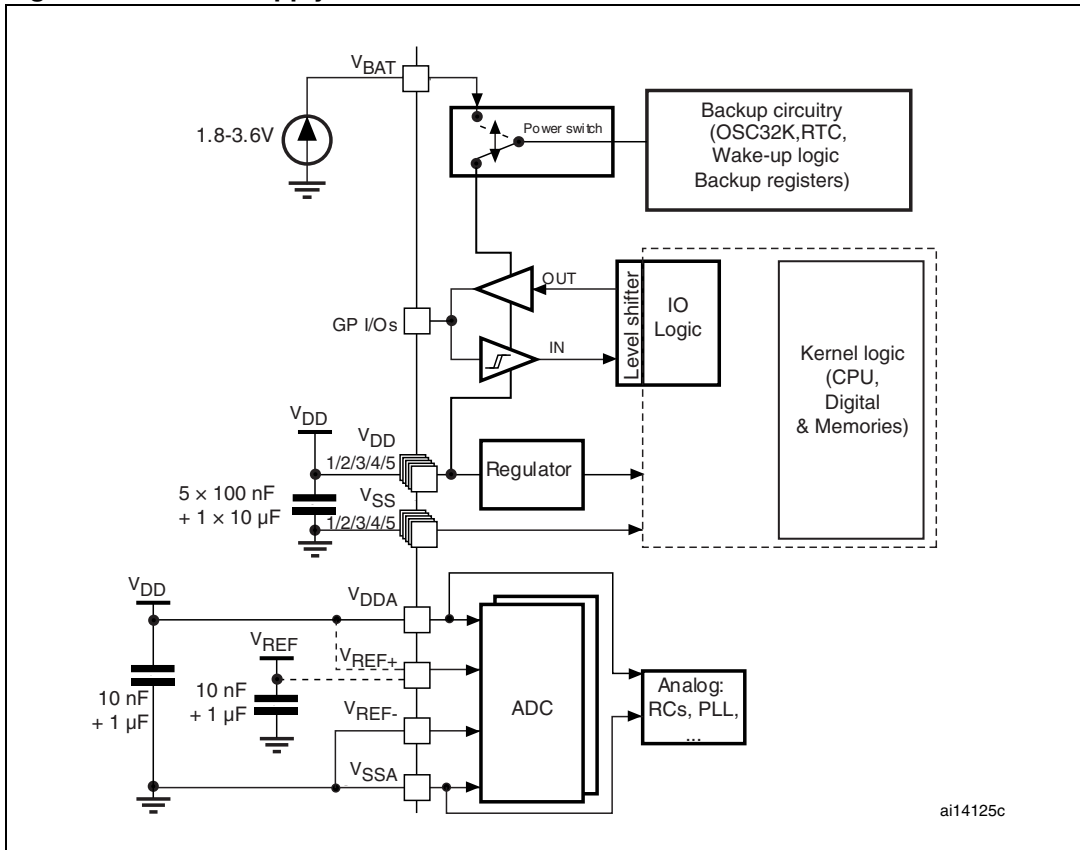


Figure 10. Pin input voltage



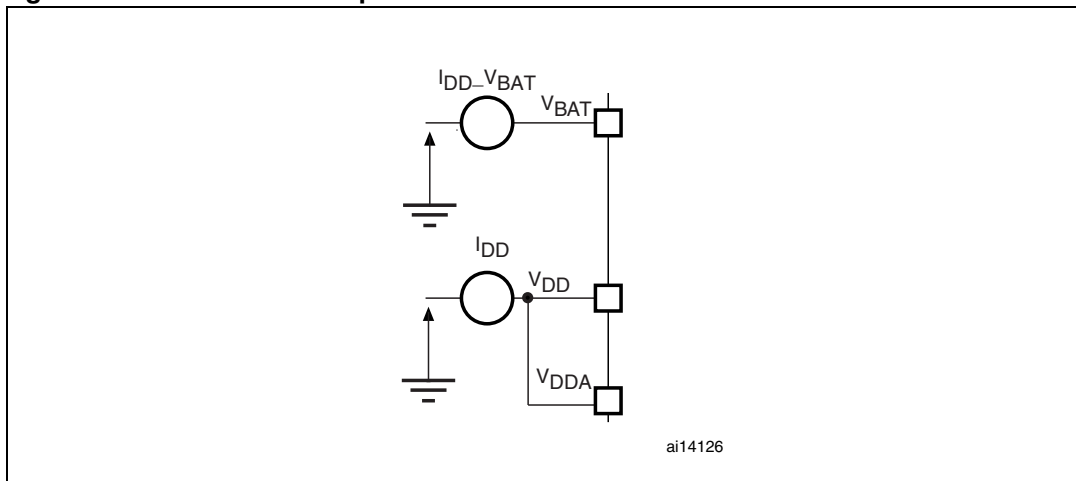
5.1.6 Power supply scheme

Figure 11. Power supply scheme



5.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 6: Voltage characteristics](#), [Table 7: Current characteristics](#), and [Table 8: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD}) ⁽¹⁾	-0.3	4.0	V
V_{IN}	Input voltage on five volt tolerant pin ⁽²⁾	$V_{SS}-0.3$	+5.5	
	Input voltage on any other pin ⁽²⁾	$V_{SS}-0.3$	$V_{DD}+0.3$	
$ \Delta V_{DDX} $	Variations between different power pins	50	50	mV
$ V_{SSX}-V_{SS} $	Variations between all the different ground pins	50	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 5.3.12: Absolute maximum ratings (electrical sensitivity)		

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded (see [Table 7: Current characteristics](#)). This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.

Table 7. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source) ⁽¹⁾	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) ⁽¹⁾	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$ ⁽²⁾⁽³⁾	Injected current on NRST pin	± 5	
	Injected current on HSE OSC_IN and LSE OSC_IN pins	± 5	
	Injected current on any other pin ⁽⁴⁾	± 5	
$\Sigma I_{INJ(PIN)}$ ⁽²⁾	Total injected current (sum of all I/O and control pins) ⁽⁴⁾	± 25	

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
3. Negative injection disturbs the analog performance of the device. See note in [Section 5.3.18: 12-bit ADC characteristics](#).
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 8. Thermal characteristics

Symbol	Ratings	Value	Unit
T _{STG}	Storage temperature range	-65 to +150	°C
T _J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 9. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f _{HCLK}	Internal AHB clock frequency		0	72	MHz
f _{PCLK1}	Internal APB1 clock frequency		0	36	
f _{PCLK2}	Internal APB2 clock frequency		0	72	
V _{DD}	Standard operating voltage		2	3.6	V
V _{BAT}	Backup operating voltage		1.8	3.6	V
P _D	Power dissipation at T _A = 85 °C for suffix 6 or T _A = 105 °C for suffix 7 ⁽¹⁾	LQFP144		TBD ⁽²⁾	mW
		LQFP100		434	
		LQFP64		444	
		LFBGA100		487	
		LFBGA144		TBD ⁽²⁾	
T _A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
		Low power dissipation ⁽³⁾	-40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	-40	105	°C
		Low power dissipation ⁽³⁾	-40	125	
T _J	Junction temperature range	6 suffix version	-40	105	°C
		7 suffix version	-40	125	

1. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{J,max} (see [Table 6.2: Thermal characteristics on page 113](#)).

2. TBD = to be determined.

3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{J,max} (see [Table 6.2: Thermal characteristics on page 113](#)).

5.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 10](#) are derived from tests performed under the ambient temperature condition summarized in [Table 9](#).

Table 10. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	$\mu\text{s/V}$
	V_{DD} fall time rate		20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 11](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 9](#).

Table 11. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}^{(2)}$	PVD hysteresis			100		mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8 ⁽¹⁾	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$	PDR hysteresis			40		mV
$T_{RSTTEMPO}^{(2)}$	Reset temporization		1	2.5	4.5	mS

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

2. Guaranteed by design, not tested in production.

5.3.4 Embedded reference voltage

The parameters given in [Table 12](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 9](#).

Table 12. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\text{ °C} < T_A < +105\text{ °C}$	1.16	1.20	1.26	V
		$-40\text{ °C} < T_A < +85\text{ °C}$	1.16	1.20	1.24	V
$T_{S_vrefint}^{(1)}$	ADC sampling time when reading the internal reference voltage			5.1	17.1	μs

1. Shortest sampling time can be determined in the application by multiple iterations.

5.3.5 Supply current characteristics

The current consumption is measured as described in [Figure 12: Current consumption measurement scheme](#).

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in [Table 13](#), [Table 14](#) and [Table 15](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 9](#).

Table 13. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f _{HCLK}	Max ⁽¹⁾		Unit
				T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in Run mode	External clock ⁽²⁾ , all peripherals enabled	72 MHz	69	70	mA
			48 MHz	50	50.5	
			36 MHz	39	39.5	
			24 MHz	27	28	
			16 MHz	20	20.5	
			8 MHz	11	11.5	
		External clock ⁽²⁾ , all peripherals disabled	72 MHz	37	37.5	
			48 MHz	28	28.5	
			36 MHz	22	22.5	
			24 MHz	16.5	17	
			16 MHz	12.5	13	
			8 MHz	8	8	

1. Data based on characterization results, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz; external clock is 9 MHz for f_{HCLK} = 36 MHz.

Table 14. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f _{HCLK}	Max		Unit
				T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in Run mode	External clock ⁽¹⁾ , all peripherals enabled	72 MHz ⁽²⁾	66	67	mA
			48 MHz ⁽³⁾	43.5	45.5	
			36 MHz ⁽³⁾	33	35	
			24 MHz ⁽³⁾	23	24.5	
			16 MHz ⁽³⁾	16	18	
			8 MHz ⁽³⁾	9	10.5	
		External clock ⁽¹⁾ , all peripherals disabled ⁽³⁾	72 MHz	33	33.5	
			48 MHz	23	23.5	
			36 MHz	18	18.5	
			24 MHz	13	13.5	
			16 MHz	10	10.5	
			8 MHz	6	6.5	

1. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz; external clock is 9 MHz for f_{HCLK} = 36 MHz.
2. Data based on characterization results, tested in production at V_{DD max}, f_{HCLK max}. and T_{A max}, and code executed from RAM.
3. Based on characterization, not tested in production.

Figure 13. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

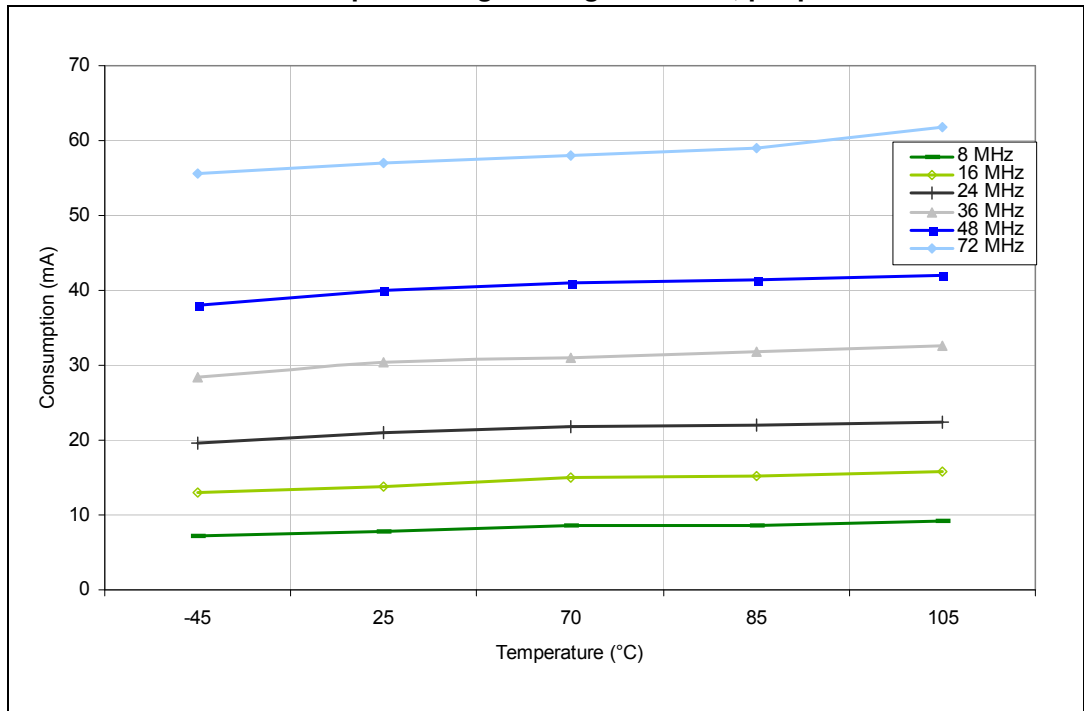


Figure 14. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled

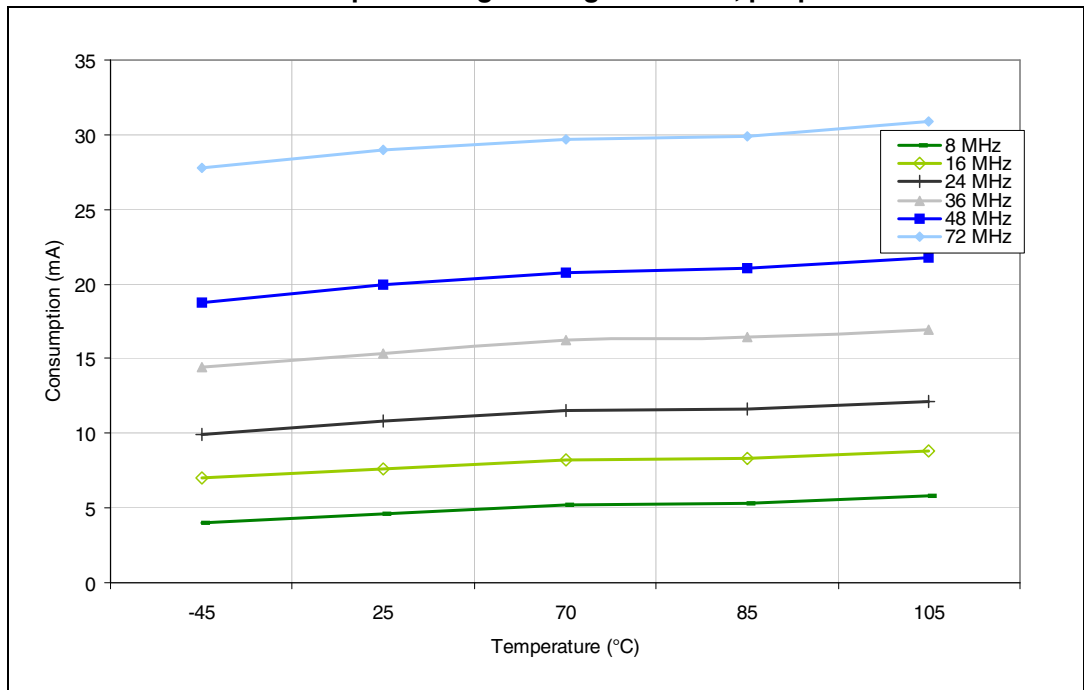


Table 15. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f _{HCLK}	Max		Unit
				T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in Sleep mode	External clock ⁽¹⁾ , all peripherals enabled	72 MHz ⁽²⁾	66	67	mA
			48 MHz ⁽³⁾	43.5	45.5	
			36 MHz ⁽³⁾	33	35	
			24 MHz ⁽³⁾	23	24.5	
			16 MHz ⁽³⁾	16	18	
			8 MHz ⁽³⁾	9	10.5	
		External clock ⁽¹⁾ , all peripherals disabled ⁽³⁾	72 MHz	33	33.5	
			48 MHz	23	23.5	
			36 MHz	18	18.5	
			24 MHz	13	13.5	
			16 MHz	10	10.5	
			8 MHz	6	6.5	

1. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz; external clock is 9 MHz for f_{HCLK} = 36 MHz.
2. Data based on characterization results, tested in production at V_{DD max}, f_{HCLK max} and T_{A max}.
3. Based on characterization, not tested in production.

Table 16. Typical and maximum current consumptions in Stop and Standby modes⁽¹⁾

Symbol	Parameter	Conditions	Typ ⁽²⁾		Max		Unit
			V _{DD} /V _{BAT} = 2.4 V	V _{DD} /V _{BAT} = 3.3 V	T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in Stop mode	Regulator in main mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	34.5	35	TBD ⁽³⁾	TBD ⁽³⁾	μA
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	24.5	25	TBD ⁽³⁾	TBD ⁽³⁾	
	Supply current in Standby mode ⁽⁴⁾	Low-speed internal RC oscillator and independent watchdog ON	3	3.8	TBD	TBD	
		Low-speed internal RC oscillator ON, independent watchdog OFF	2.8	3.6	TBD	TBD	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.9	2.1	5 ⁽⁵⁾	6.5 ⁽⁵⁾	
I _{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.1	1.4	TBD ⁽⁵⁾	TBD ⁽⁵⁾	

1. TBD stands for to be determined.
2. Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V, unless otherwise specified.
3. Data based on characterization results, tested in production at V_{DD}max and f_{HCLK} max.
4. To have the Standby consumption with RTC ON, add I_{DD_VBAT} (Low-speed oscillator and RTC ON) to I_{DD} Standby (when V_{DD} is present the Backup Domain is powered by V_{DD} supply).
5. Data based on characterization results, not tested in production.

Figure 15. Current consumption in Stop mode with regulator in main mode versus temperature at different V_{DD} values

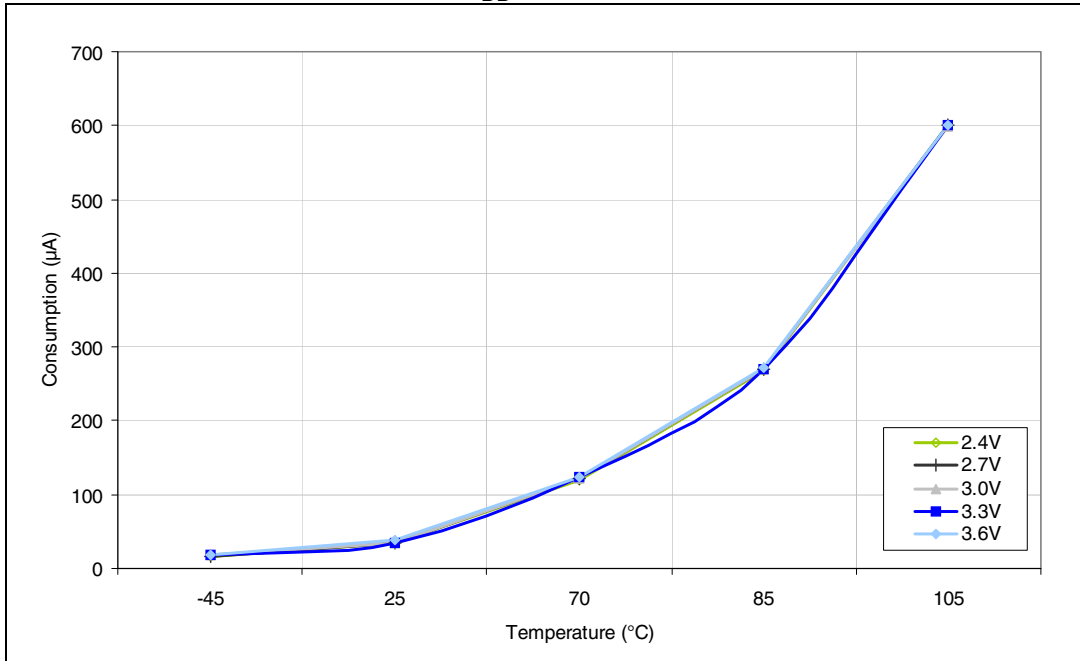


Figure 16. Current consumption in Stop mode with regulator in low-power mode versus temperature at different V_{DD} values

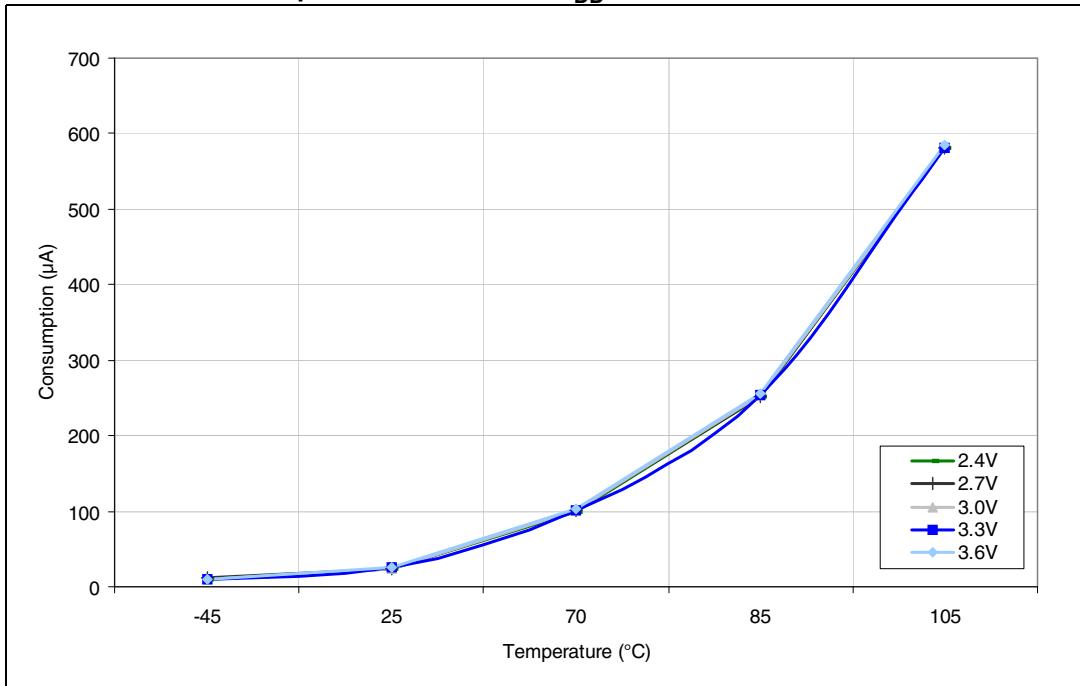
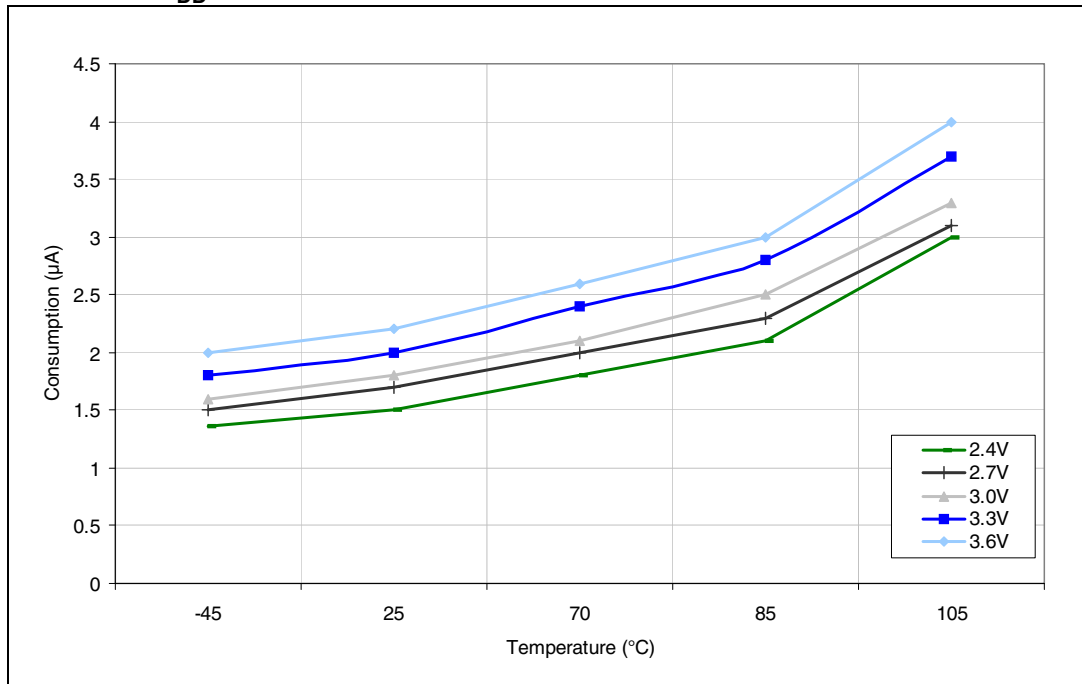


Figure 17. Current consumption in Standby mode versus temperature at different V_{DD} values



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).
- Ambient temperature and V_{DD} supply voltage conditions summarized in [Table 9](#).
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling)

When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

Table 17. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f _{HCLK}	Typ ⁽¹⁾		Unit
				All peripherals enabled ⁽²⁾	All peripherals disabled	
I _{DD}	Supply current in Run mode	External clock ⁽³⁾	72 MHz	51	30.5	mA
			48 MHz	34.6	20.7	
			36 MHz	26.6	16.2	
			24 MHz	18.5	11.4	
			16 MHz	12.8	8.2	
			8 MHz	7.2	5	
			4 MHz	4.2	3.1	
			2 MHz	2.7	2.1	
			1 MHz	2	1.7	
			500 kHz	1.6	1.4	
		125 kHz	1.3	1.2		
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	45	27	mA
			48 MHz	34	20.1	
			36 MHz	26	15.6	
			24 MHz	17.9	10.8	
			16 MHz	12.2	7.6	
			8 MHz	6.6	4.4	
			4 MHz	3.6	2.5	
			2 MHz	2.1	1.5	
			1 MHz	1.4	1.1	
500 kHz	1		0.8			
125 kHz	0.7	0.6				

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 18. Typical current consumption in Sleep mode, code with data processing code running from Flash or RAM

Symbol	Parameter	Conditions	f _{HCLK}	Typ ⁽¹⁾		Unit
				All peripherals enabled ⁽²⁾	All peripherals disabled	
I _{DD}	Supply current in Sleep mode	External clock ⁽³⁾	72 MHz	29.5	6.4	mA
			48 MHz	20	4.6	
			36 MHz	15.1	3.6	
			24 MHz	10.4	2.6	
			16 MHz	7.2	2	
			8 MHz	3.9	1.3	
			4 MHz	2.6	1.2	
			2 MHz	1.85	1.15	
			1 MHz	1.5	1.1	
			500 kHz	1.3	1.05	
		125 kHz	1.2	1.05		
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	25.6	5.1	
			48 MHz	19.4	4	
			36 MHz	14.5	3	
			24 MHz	9.8	2	
			16 MHz	6.6	1.4	
			8 MHz	3.3	0.7	
			4 MHz	2	0.6	
			2 MHz	1.25	0.55	
			1 MHz	0.9	0.5	
500 kHz	0.7		0.45			
125 kHz	0.6	0.45				

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in [Table 19](#). The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in [Table 6](#)

Table 19. Peripheral current consumption⁽¹⁾

Peripheral		Typical consumption at 25 °C	Unit
APB1	TIM2	1.2	mA
	TIM3	1.2	
	TIM4	1.2	
	TIM5	1.2	
	TIM6	0.4	
	TIM7	0.4	
	SPI2	0.2	
	SPI3	0.2	
	USART2	0.4	
	USART3	0.4	
	UART4	0.5	
	UART5	0.6	
	I2C1	0.4	
	I2C2	0.4	
	USB	0.65	
	CAN	0.72	
DAC	0.72		

Table 19. Peripheral current consumption⁽¹⁾ (continued)

Peripheral		Typical consumption at 25 °C	Unit
APB2	GPIOA	0.55	mA
	GPIOB	0.72	
	GPIOC	0.72	
	GIOD	0.55	
	GPIOE	1	
	GPIOF	0.72	
	GPIOG	1	
	ADC1 ⁽²⁾	1.9	
	ADC2	1.7	
	TIM1	1.8	
	SPI1	0.4	
	TIM8	1.7	
	USART1	0.9	
	ADC3	1.7	

- $f_{HCLK} = 72$ MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
- Specific conditions for ADC: $f_{HCLK} = 56$ MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCLK} = f_{APB2}/4$, ADON bit in the ADC_CR2 register is set to 1.

5.3.6 External clock source characteristics

High-speed external user clock

The characteristics given in [Table 20](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 9](#).

Table 20. High-speed external (HSE) user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency ⁽¹⁾			8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time ⁽¹⁾		16			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time ⁽¹⁾				5	
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			± 1	μA

- Value based on design simulation and/or technology characteristics. It is not tested in production.

Low-speed external user clock

The characteristics given in [Table 21](#) result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 9](#).

Table 21. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency ⁽¹⁾			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time ⁽¹⁾		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time ⁽¹⁾				5	
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			± 1	μA

1. Value based on design simulation and/or technology characteristics. It is not tested in production.

Figure 18. High-speed external clock source AC timing diagram

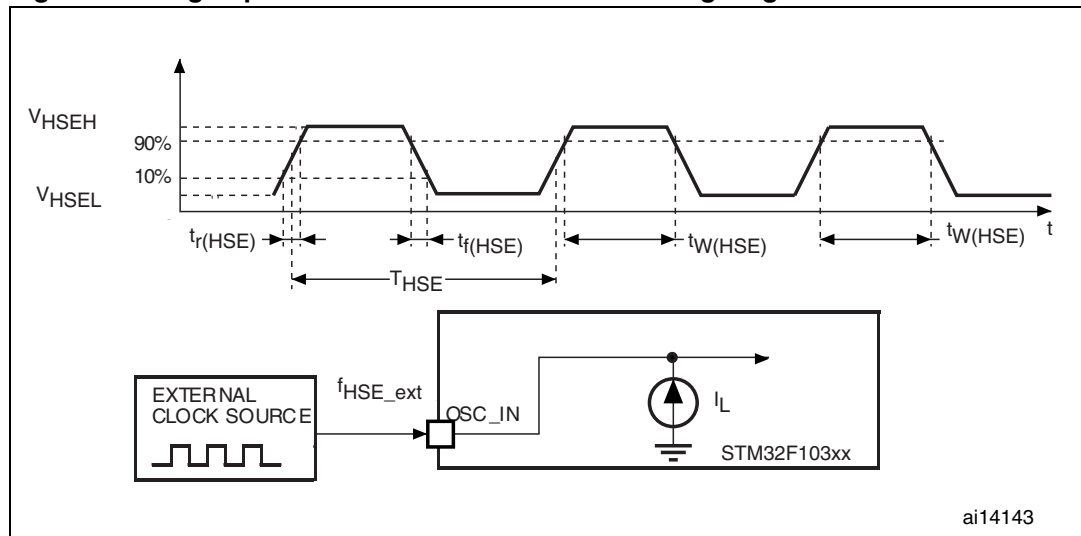
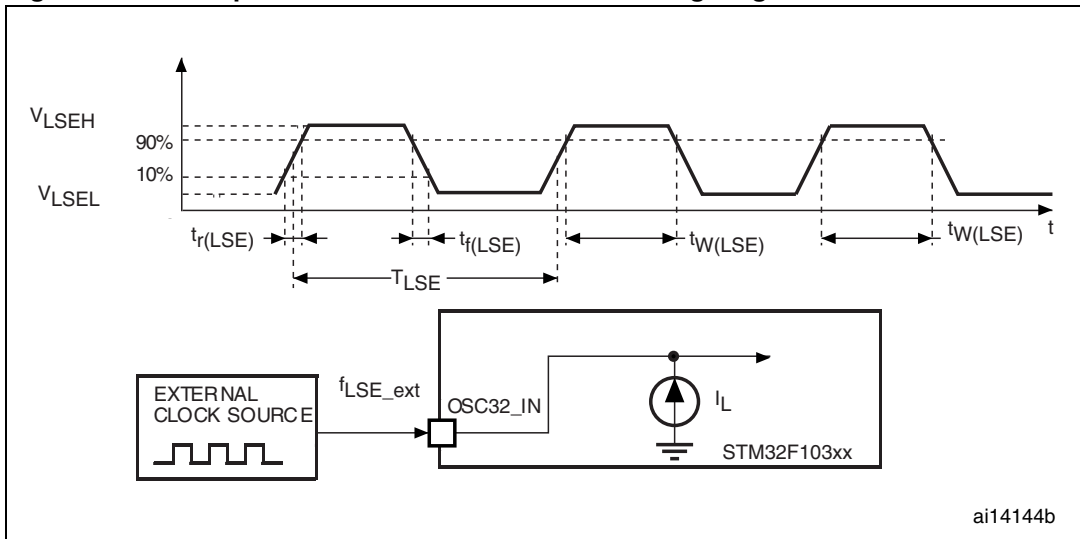


Figure 19. Low-speed external clock source AC timing diagram



High-speed external clock

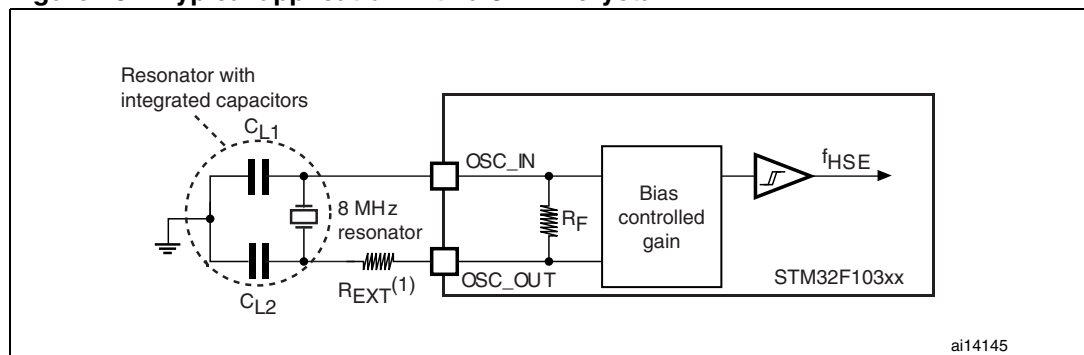
The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 22](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 22. HSE 4-16 MHz oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	16	MHz
R_F	Feedback resistor			200		k Ω
C_{L1} C_{L2} ⁽²⁾	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽³⁾	$R_S = 30 \Omega$		30		pF
i_2	HSE driving current	$V_{DD} = 3.3 V$ $V_{IN} = V_{SS}$ with 30 pF load			1	mA
g_m ⁽⁴⁾	Oscillator transconductance	Startup	25			mA/V
$t_{SU(HSE)}$ ⁽⁵⁾	startup time	V_{DD} is stabilized		2		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 25pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included when sizing C_{L1} and C_{L2} (10 pF can be used as a rough estimate of the combined pin and board capacitance).
3. The relatively low value of the R_F resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. Based on characterization results, not tested in production.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 20. Typical application with a 8-MHz crystal



1. R_{EXT} value depends on the crystal characteristics. Typical value is in the range of 5 to 6 R_S .

Low-speed external clock

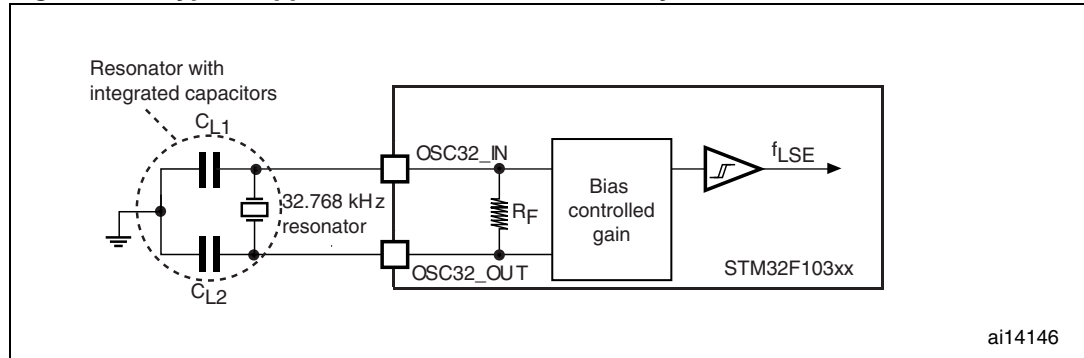
The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 23](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 23. LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor			5		$M\Omega$
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽¹⁾	$R_S = 30$ k Ω			15	pF
I_2	LSE driving current	$V_{DD} = 3.3$ V $V_{IN} = V_{SS}$			1.4	μ A
g_m	Oscillator Transconductance		5			μ A/V
$t_{SU(LSE)}$ ⁽²⁾	startup time	V_{DD} is stabilized		3		s

1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 21. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in [Table 24](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 9](#).

High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			8		MHz
ACC_{HSI}	Accuracy of HSI oscillator	$T_A = -40$ to 105 °C			$\pm 3^{(2)}$	%
		$T_A = 25$ °C		± 1	± 2	%
$t_{su(HSI)}$	HSI oscillator start up time		1		2	μs
$I_{DD(HSI)}$	HSI oscillator power consumption			80	100	μA

1. $V_{DD} = 3.3$ V, $T_A = -40$ to 105 °C unless otherwise specified.

2. Values based on device characterization, not tested in production.

LSI low speed internal RC oscillator

Table 25. LSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min ⁽²⁾	Typ	Max	Unit
f_{LSI}	Frequency		30	40	60	kHz
$t_{su(LSI)}$	LSI oscillator startup time				85	μs
$I_{DD(LSI)}$	LSI oscillator power consumption			0.65	1.2	μA

1. $V_{DD} = 3$ V, $T_A = -40$ to 105 °C unless otherwise specified.

2. Value based on device characterization, not tested in production.

Wakeup time from low-power mode

The wakeup times given in [Table 26](#) is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 9](#).

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Unit
$t_{WUSLEEP}^{(1)}$	Wakeup from Sleep mode	Wakeup on HSI RC clock	1.8	μs
$t_{WUSTOP}^{(1)}$	Wakeup from Stop mode (regulator in run mode)	HSI RC wakeup time = 2 μs	3.6	μs
	Wakeup from Stop mode (regulator in low power mode)	HSI RC wakeup time = 2 μs , Regulator wakeup from LP mode time = 5 μs	5.4	
$t_{WUSTDBY}^{(1)}$	Wakeup from Standby mode	HSI RC wakeup time = 2 μs , Regulator wakeup from power down time = 38 μs	50	μs

1. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in [Table 27](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 9](#).

Table 27. PLL characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max ⁽¹⁾	
f_{PLL_IN}	PLL input clock			8.0		MHz
	PLL input clock duty cycle		40		60	%
f_{PLL_OUT}	PLL multiplier output clock		16		72	MHz
t_{LOCK}	PLL lock time				200	μs

1. Data based on device characterization, not tested in production.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to $+105$ °C unless otherwise specified.

Table 28. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max ⁽¹⁾	Unit
t_{prog}	Word programming time	$T_A = -40$ to $+105$ °C	40	52.5	70	µs
t_{ERASE}	Page (2 KB) erase time	$T_A = -40$ to $+105$ °C	20		40	ms
t_{ME}	Mass erase time	$T_A = -40$ to $+105$ °C	20		40	ms
I_{DD}	Supply current	Read mode $f_{HCLK} = 72$ MHz with 2 wait states, $V_{DD} = 3.3$ V			28	mA
		Write mode $f_{HCLK} = 72$ MHz, $V_{DD} = 3.3$ V			7	mA
		Erase mode $f_{HCLK} = 72$ MHz, $V_{DD} = 3.3$ V			5	mA
		Power-down mode / Halt, $V_{DD} = 3.0$ to 3.6 V			50	µA
V_{prog}	Programming voltage		2		3.6	V

1. Values based on characterization and not tested in production.

Table 29. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min ⁽¹⁾	Typ	Max	
N_{END}	Endurance		TBD ⁽²⁾			kcycles
t_{RET}	Data retention	$T_A = 85$ °C, 1000 cycles	30			Years
		$T_A = 105$ °C, 1000 cycles	10			

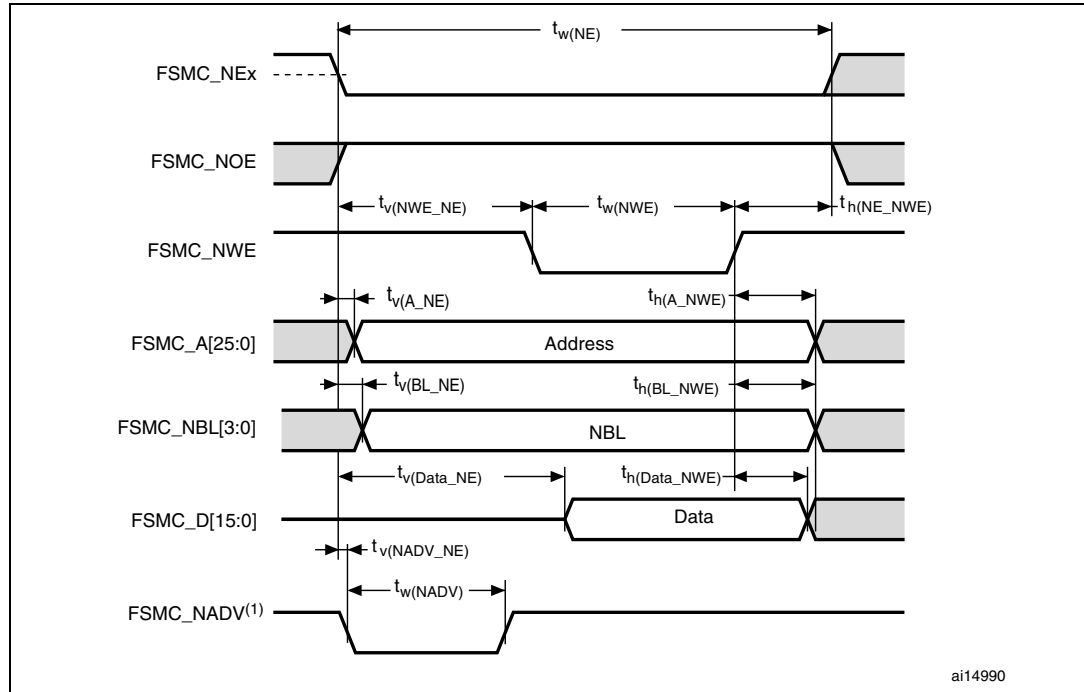
1. Values based on characterization not tested in production.

2. TBD = to be determined.

5.3.10 FSMC characteristics

All the timing characteristics are relative to the FSMC_CLK signal for synchronous SRAM/NOR Flash memory accesses.

Figure 22. Asynchronous non-multiplexed SRAM/NOR write timings



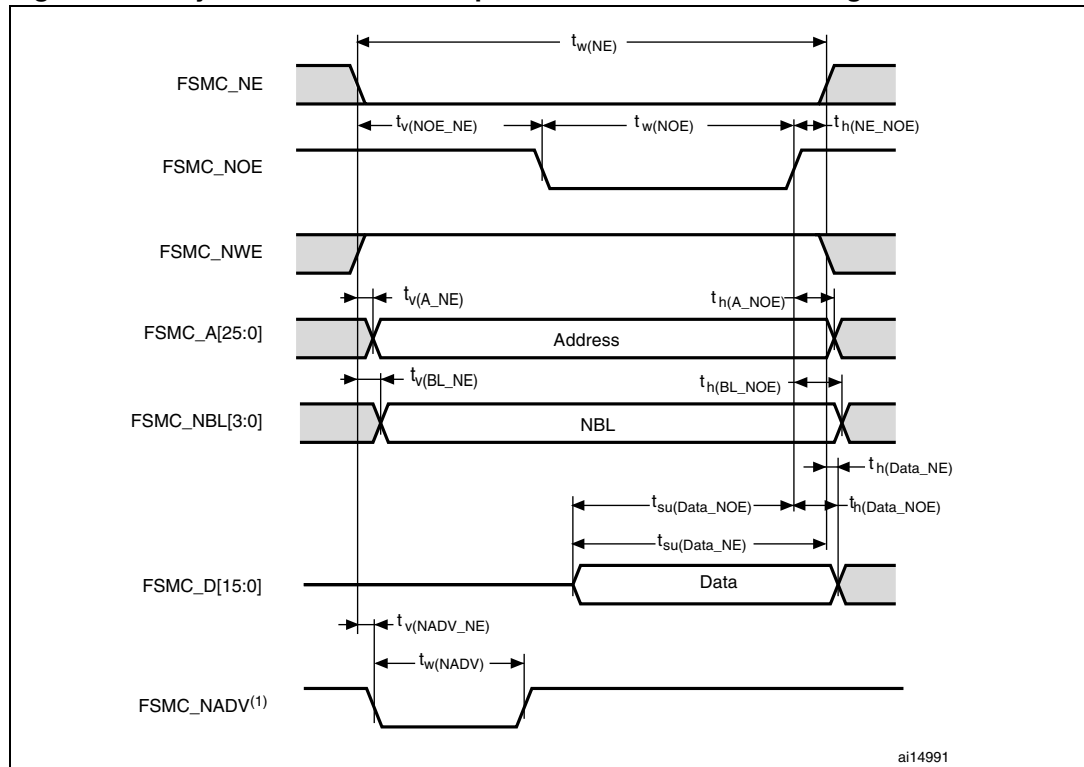
1. Mode 2/B, C and D only.

Table 30. Asynchronous non-multiplexed SRAM/NOR write timings⁽¹⁾

V _{DD_IO} = V and C _L = 15 pF				
Symbol	Parameter	Min	Max	Unit
t _{w(NE)}	FSMC_NE low time	TBD	TBD	t _{CK} /ns
t _{v(WEN_NE)}	FSMC_NEx low to FSMC_NWE low	TBD	TBD	t _{CK} /ns
t _{w(NWE)}	FSMC_NWE low time	TBD	TBD	t _{CK} /ns
t _{h(NE_NWE)}	FSMC_NWE high to FSMC_NE high hold time	TBD		t _{CK} /ns
t _{v(A_NE)}	FSMC_NEx low to FSMC_A valid		TBD	ns
t _{h(A_NWE)}	Address hold time after FSMC_NWE high	TBD		t _{CK} /ns
t _{v(BL_NE)}	FSMC_NEx low to FSMC_NBL valid		TBD	ns
t _{h(BL_NWE)}	FSMC_NBL hold time after FSMC_NWE high	TBD		t _{CK} /ns
t _{v(Data_NE)}	FSMC_NEx low to Data valid		TBD	t _{CK} /ns
t _{h(Data_NWE)}	Data hold time after FSMC_NWE high	TBD		t _{CK} /ns
t _{v(NADV_NE)}	FSMC_NEx low to FSMC_NADV low		TBD	t _{CK} /ns
t _{w(NADV)}	FSMC_NADV low time		TBD	t _{CK} /ns

1. TBD = to be determined.

Figure 23. Asynchronous non-multiplexed SRAM/NOR read timings



1. Mode 2/B, C and D only.

Table 31. Asynchronous non-multiplexed SRAM/NOR read timings⁽¹⁾

V _{DD_IO} = V and C _L = 15 pF				
Symbol	Parameter	Min	Max	Unit
t _{w(NE)}	FSMC_NE low time	TBD	TBD	t _{CK} /ns
t _{v(NOE_NE)}	FSMC_NEx low to FSMC_NOE low	TBD	TBD	t _{CK} /ns
t _{w(NOE)}	FSMC_NOE low time	TBD	TBD	t _{CK} /ns
t _{h(NE_NOE)}	FSMC_NOE high to FSMC_NE high hold time	TBD		t _{CK} /ns
t _{v(A_NE)}	FSMC_NEx low to FSMC_A valid		TBD	ns
t _{h(A_NOE)}	Address hold time after FSMC_NOE high	TBD		t _{CK} /ns
t _{v(BL_NE)}	FSMC_NEx low to FSMC_BL valid		TBD	ns
t _{h(BL_NOE)}	FSMC_BL hold time after FSMC_NOE high	TBD		t _{CK} /ns
t _{su(Data_NE)}	Data to FSMC_NEx high setup time	TBD		t _{CK} /ns
t _{su(Data_NOE)}	Data to FSMC_NOEx high setup time	TBD		t _{CK} /ns
t _{h(Data_NOE)}	Data hold time after FSMC_NOE high	TBD		t _{CK} /ns
t _{h(Data_NE)}	Data hold time after FSMC_NEx high	TBD		ns
t _{v(NADV_NE)}	FSMC_NEx low to FSMC_NADV low		TBD	t _{CK} /ns
t _{w(NADV)}	FSMC_NADV low time		TBD	t _{CK} /ns

1. TBD = to be determined.

Figure 24. Asynchronous multiplexed SRAM/NOR write timings

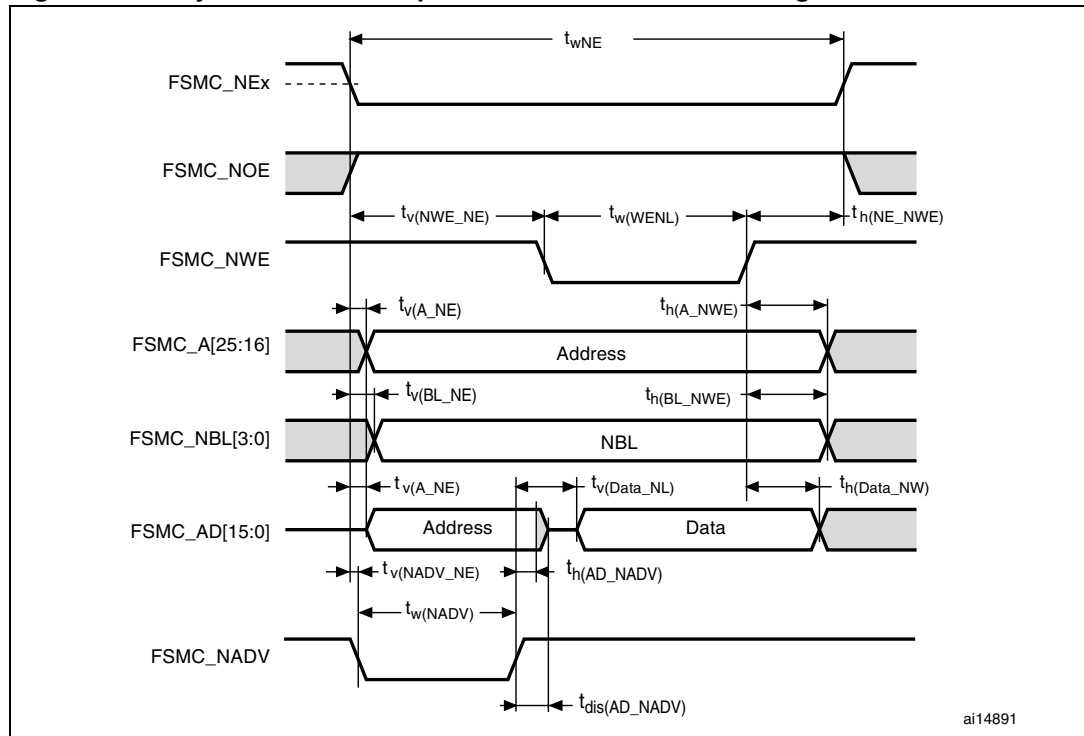


Table 32. Asynchronous multiplexed SRAM/NOR write timings⁽¹⁾

FSMC - Asynchronous multiplexed SRAM/NOR write timings V _{DD_IO} = V and C _L = 15 pF				
Symbol	Parameter	Min	Max	Unit
t _{w(NE)}	FSMC_NE low time	TBD	TBD	t _{CK} /ns
t _{v(NWE_NE)}	FSMC_NEx low to FSMC_NWE low	TBD	TBD	t _{CK} /ns
t _{w(NWE)}	FSMC_NWE low time	TBD	TBD	t _{CK} /ns
t _{h(NE_NWE)}	FSMC_NWE high to FSMC_NE high hold time	TBD		t _{CK} /ns
t _{v(A_NE)}	FSMC_NEx low to FSMC_A valid		TBD	ns
t _{v(NADV_NE)}	FSMC_NEx low to FSMC_NADV low	TBD	TBD	t _{CK} /ns
t _{w(NADV)}	FSMC_NADV low time	TBD	TBD	t _{CK} /ns
t _{h(AD_NADV)}	FSMC_AD (address) valid hold time after FSMC_NADV high	TBD		t _{CK} /ns
t _{dis(AD_NADV)}	FSMC_AD (address) disable time after FSMC_NADV high		TBD	t _{CK} /ns
t _{h(A_NWE)}	Address hold time after FSMC_NWE high	TBD		t _{CK} /ns
t _{v(BL_NE)}	FSMC_NEx low to FSMC_BL valid		TBD	ns
t _{h(BL_NWE)}	FSMC_BL hold time after FSMC_NWE high	TBD		t _{CK} /ns
t _{v(Data_NADV)}	FSMC_NADV high to Data valid	TBD		t _{CK} /ns
t _{h(Data_NWE)}	Data hold time after FSMC_NWE high	TBD		t _{CK} /ns

1. TBD = to be determined.

Figure 25. Asynchronous multiplexed SRAM/NOR read timings

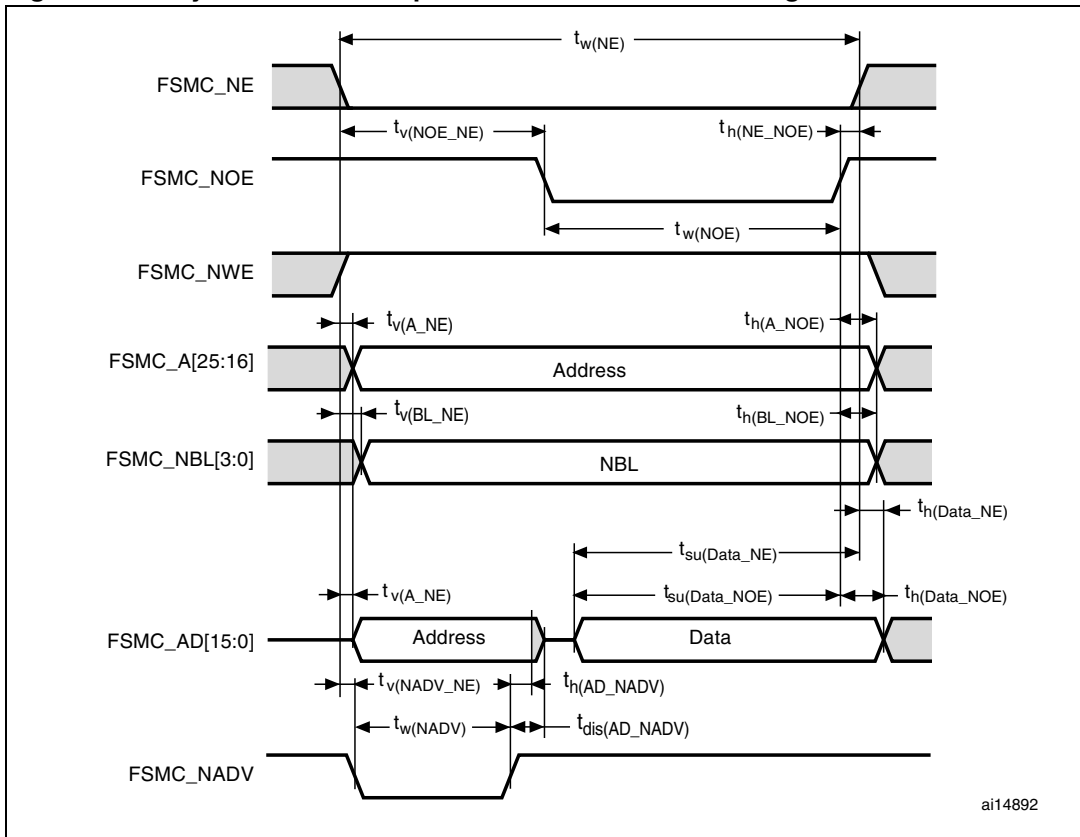


Table 33. Asynchronous multiplexed SRAM/NOR read timings

$V_{DD_IO} = V$ and $C_L = 15$ pF				
Symbol	Parameter	Min	Max	Unit
$t_{W(NE)}$	FSMC_NE low time	TBD	TBD	t_{CK}/ns
$t_{V(NOEN)}$	FSMC_NEx low to FSMC_NOE low	TBD	TBD	t_{CK}/ns
$t_{W(NOEN)}$	FSMC_NOE low time	TBD	TBD	t_{CK}/ns
$t_{h(NE_WEN)}$	FSMC_WEN high to FSMC_NE high hold time	TBD		t_{CK}/ns
$t_{h(NE_NOEN)}$	FSMC_NOE high to FSMC_NE high hold time	TBD		t_{CK}/ns
$t_{V(A_NE)}$	FSMC_NEx low to FSMC_A valid		TBD	ns
$t_{V(NADV_NE)}$	FSMC_NEx low to FSMC_NADV low	TBD	TBD	t_{CK}/ns
$t_{W(NADV)}$	FSMC_NADV low time	TBD	TBD	t_{CK}/ns
$t_{h(AD_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	TBD		t_{CK}/ns
$t_{dis(AD_NADV)}$	FSMC_AD (address) disable time after FSMC_NADV high		TBD	t_{CK}/ns
$t_{h(A_NOEN)}$	Address hold time after FSMC_NOE high	TBD		t_{CK}/ns
$t_{h(BL_NOEN)}$	FSMC_BL hold time after FSMC_NOE high	TBD		t_{CK}/ns
$t_{V(BL_NE)}$	FSMC_NEx low to FSMC_BL valid		TBD	ns
$t_{SU(Data_NE)}$	Data to FSMC_NEx high setup time	TBD		t_{CK}/ns
$t_{SU(Data_NOEN)}$	Data to FSMC_NOE high setup time	TBD		t_{CK}/ns
$t_{h(Data_NE)}$	Data hold time after FSMC_NEx high	TBD		ns
$t_{h(Data_NOEN)}$	Data hold time after FSMC_NOE high	TBD		ns

Figure 26. Synchronous multiplexed NOR/PSRAM read timings

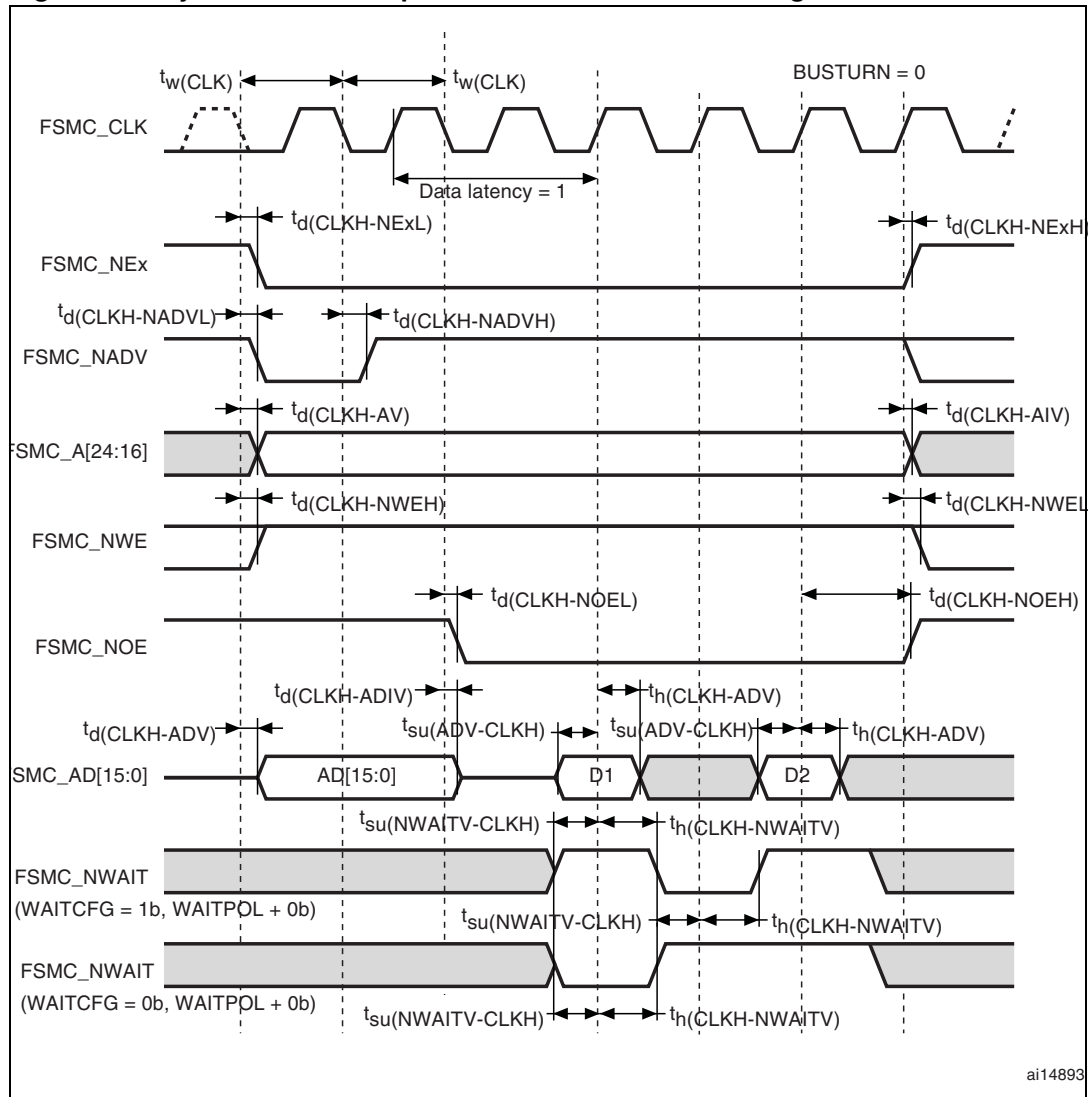


Table 34. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾

$V_{DD_IO} = V$ and $C_L = 15$ pF				
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	TBD	-	ns
$t_{d(CLKH-NExL)}$	FSMC_CLK high to FSMC_NEx low ($x = 0...2$)	-	TBD	ns
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high ($x = 0...2$)	TBD	-	ns
$t_{d(CLKH-NADVl)}$	FSMC_CLK high to FSMC_NADV low	-	TBD	ns
$t_{d(CLKH-NADVh)}$	FSMC_CLK high to FSMC_NADV high	TBD	-	ns
$t_{d(CLKH-AV)}$	FSMC_CLK high to FSMC_Ax valid ($x = 16...25$)	-	TBD	ns
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid ($x = 16...25$)	TBD	-	ns
$t_{d(CLKH-NWEL)}$	FSMC_CLK high to FSMC_NWE low	-	TBD	ns
$t_{d(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	TBD	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	TBD	ns
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	TBD	-	ns
$t_{d(CLKH-ADV)}$	FSMC_CLK high to FSMC_AD[15:0] valid	-	TBD	ns
$t_{d(CLKH-ADIV)}$	FSMC_CLK high to FSMC_AD[15:0] invalid	TBD	-	ns
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	TBD	-	ns
$t_h(CLKH-ADV)$	FSMC_A/D[15:0] valid data after FSMC_CLK high	TBD	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	TBD	-	ns
$t_h(CLKH-NWAITV)$	FSMC_NWAIT valid after FSMC_CLK high	TBD	-	ns

1. TBD = to be determined.

Figure 27. Synchronous multiplexed PSRAM write timings

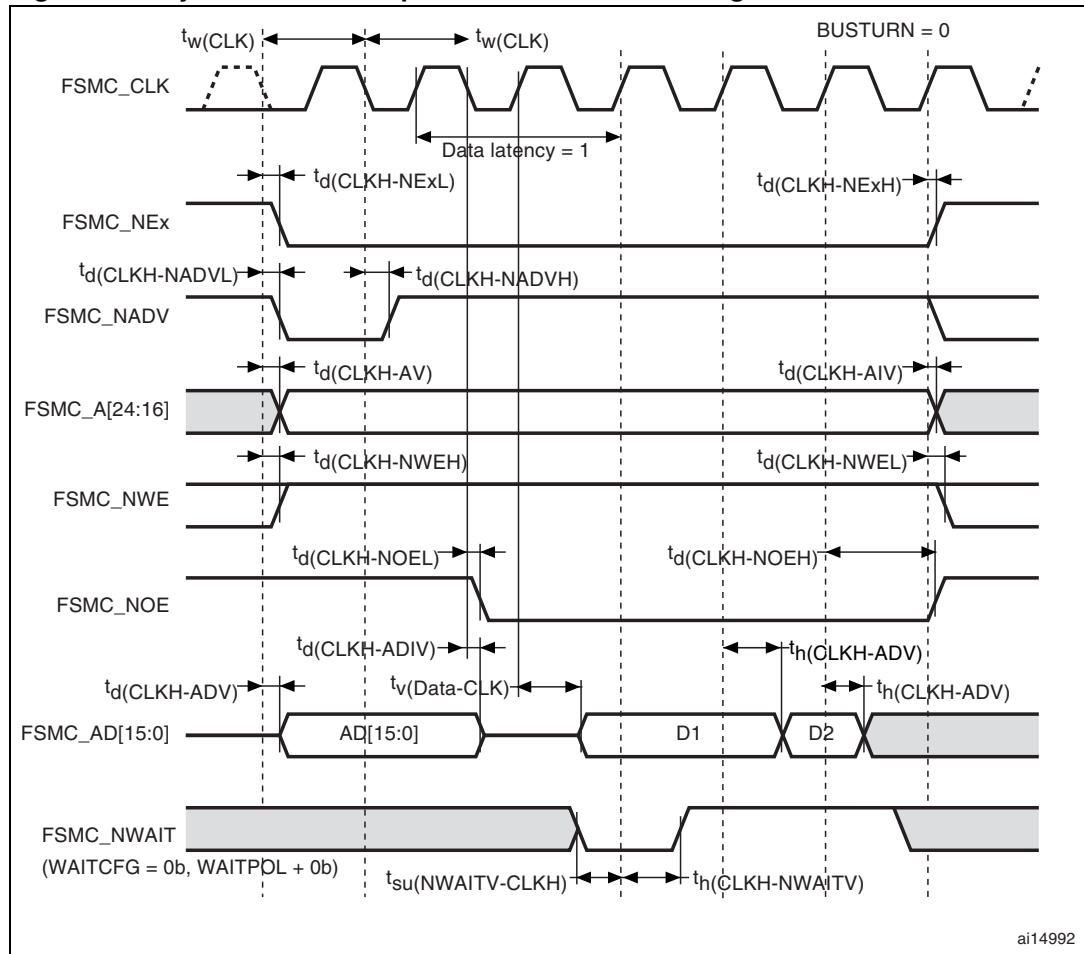


Table 35. Synchronous multiplexed PSRAM write timings⁽¹⁾

$V_{DD_IO} = V$ and $C_L = 15$ pF				
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	TBD	-	ns
$t_{d(CLKH-NExL)}$	FSMC_CLK high to FSMC_NEx low ($x = 0...2$)	-	TBD	ns
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high ($x = 0...2$)	TBD	-	ns
$t_{d(CLKH-NADVl)}$	FSMC_CLK high to FSMC_NADV low	-	TBD	ns
$t_{d(CLKH-NADVh)}$	FSMC_CLK high to FSMC_NADV high	TBD	-	ns
$t_{d(CLKH-AV)}$	FSMC_CLK high to FSMC_Ax valid ($x = 16...25$)	-	TBD	ns
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid ($x = 16...25$)	TBD	-	ns
$t_{d(CLKH-NWEL)}$	FSMC_CLK high to FSMC_NWE low	-	TBD	ns
$t_{d(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	TBD	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	TBD	ns
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	TBD	-	ns
$t_{d(CLKH-ADV)}$	FSMC_CLK high to FSMC_AD[15:0] valid	-	TBD	ns
$t_{d(CLKH-ADIV)}$	FSMC_CLK high to FSMC_AD[15:0] invalid	TBD	-	ns
$t_h(CLKH-ADV)$	FSMC_A/D[15:0] valid data after FSMC_CLK high	TBD	-	ns
$t_{su}(NWAITV-CLKH)$	FSMC_NWAIT valid before FSMC_CLK high	TBD	-	ns
$t_h(CLKH-NWAITV)$	FSMC_NWAIT valid after FSMC_CLK high	TBD	-	ns
$t_v(Data-CLK)$	FSMC_CLK high to FSMC_CLK valid	TBD	-	ns

1. TBD = to be determined.

Figure 28. Synchronous non-multiplexed NOR/PSRAM read timings

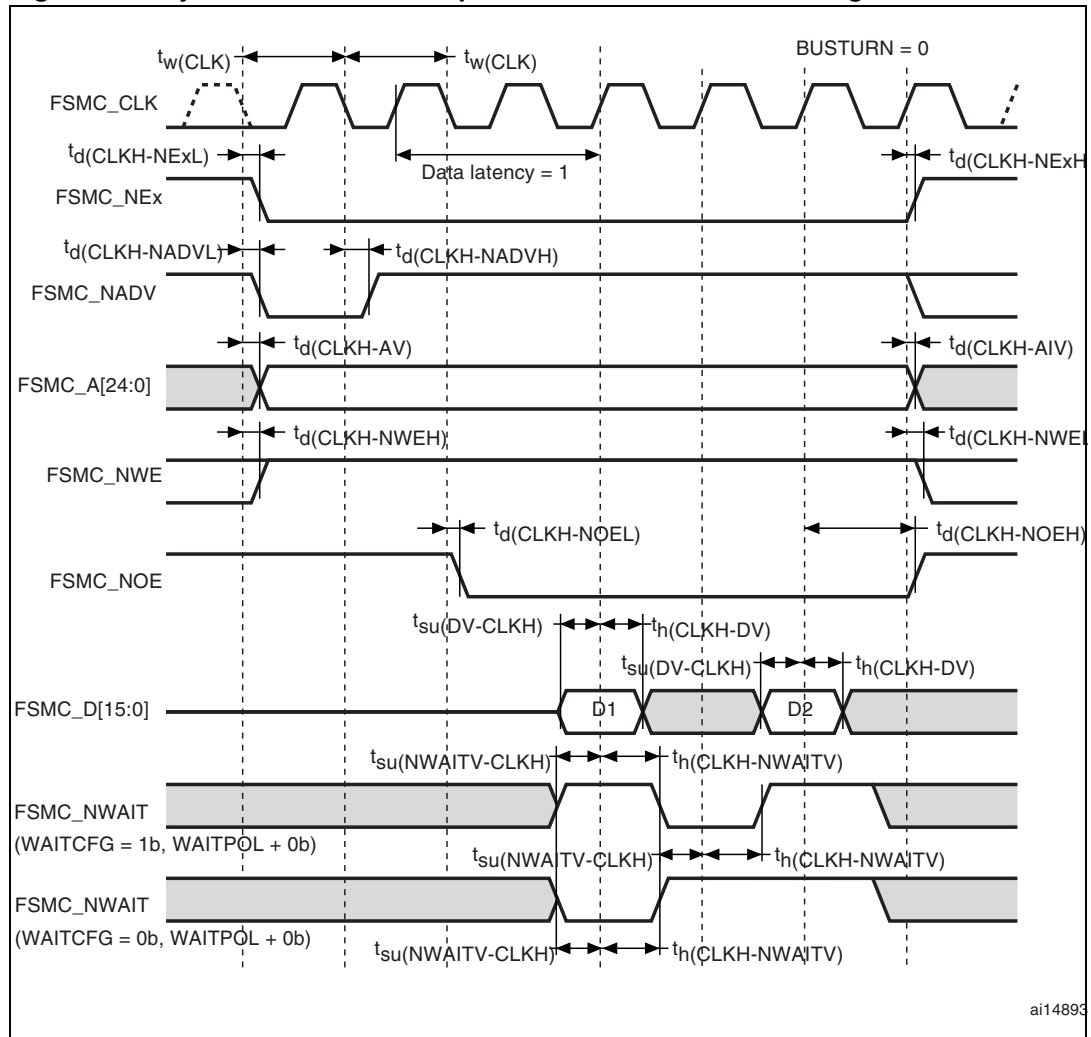


Table 36. Synchronous non-multiplexed NOR/PSRAM read timings⁽¹⁾

$V_{DD_IO} = V$ and $C_L = 15$ pF				
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	TBD	-	ns
$t_{d(CLKH-NExL)}$	FSMC_CLK high to FSMC_NEx low ($x = 0...2$)	-	TBD	ns
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high ($x = 0...2$)	TBD	-	ns
$t_{d(CLKH-NADVl)}$	FSMC_CLK high to FSMC_NADV low	-	TBD	ns
$t_{d(CLKH-NADVh)}$	FSMC_CLK high to FSMC_NADV high	TBD	-	ns
$t_{d(CLKH-AV)}$	FSMC_CLK high to FSMC_Ax valid ($x = 0...25$)	-	TBD	ns
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid ($x = 0...25$)	TBD	-	ns
$t_{d(CLKH-NWEL)}$	FSMC_CLK high to FSMC_NWE low	-	TBD	ns
$t_{d(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	TBD	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	TBD	ns
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	TBD	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	TBD	-	ns
$t_h(CLKH-DV)$	FSMC_D[15:0] valid data after FSMC_CLK high	TBD	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_SMCLK high	TBD	-	ns
$t_h(CLKH-NWAITV)$	FSMC_NWAIT valid after FSMC_CLK high	TBD	-	ns

1. TBD = to be determined.

Figure 29. Synchronous non-multiplexed PSRAM write timings

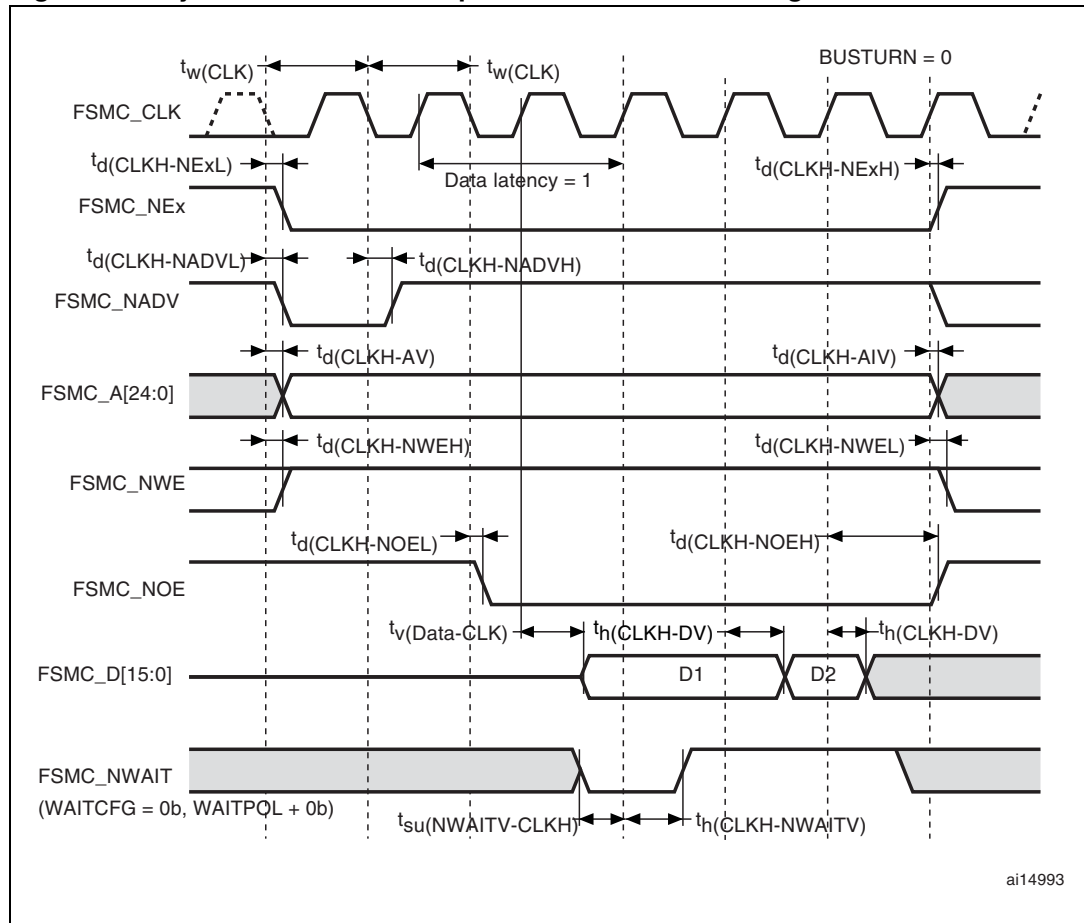
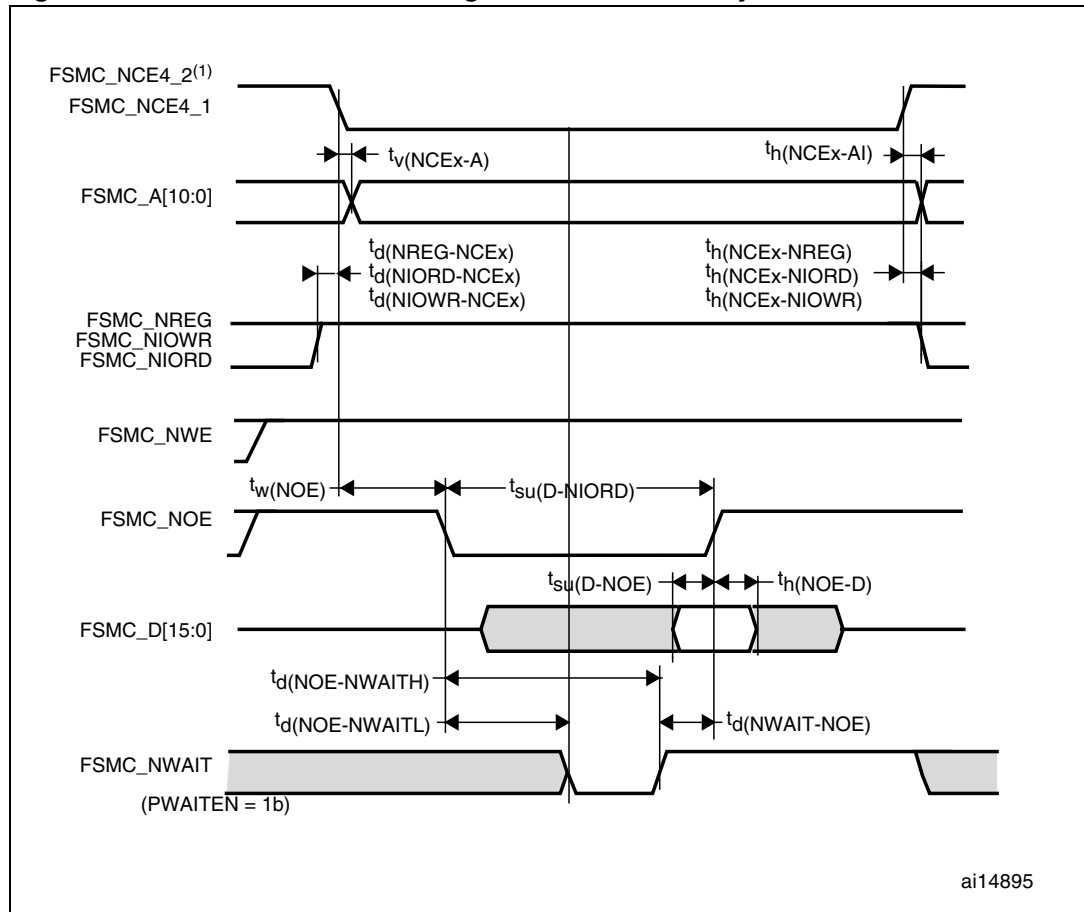


Table 37. Synchronous non-multiplexed PSRAM write timings⁽¹⁾

$V_{DD_IO} = V$ and $C_L = 15$ pF				
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	TBD	-	ns
$t_{d(CLKH-NExL)}$	FSMC_CLK high to FSMC_NEx low ($x = 0...2$)	-	TBD	ns
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high ($x = 0...2$)	x	-	ns
$t_{d(CLKH-NADVl)}$	FSMC_CLK high to FSMC_NADV low	-	TBD	ns
$t_{d(CLKH-NADVh)}$	FSMC_CLK high to FSMC_NADV high	TBD	-	ns
$t_{d(CLKH-AV)}$	FSMC_CLK high to FSMC_Ax valid ($x = 16...25$)	-	TBD	ns
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid ($x = 16...25$)	TBD	-	ns
$t_{d(CLKH-NWEL)}$	FSMC_CLK high to FSMC_NWE low	-	TBD	ns
$t_{d(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	TBD	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	TBD	ns
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	TBD	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	TBD	-	ns
$t_h(CLKH-DV)$	FSMC_D[15:0] valid data after FSMC_CLK high	TBD	-	ns
$t_v(Data-CLK)$	FSMC_CLK high to FSMC_CLK valid	TBD	-	ns
$t_h(CLKH-NWAITV)$	FSMC_NWAIT valid after FSMC_CLK high	TBD	-	ns

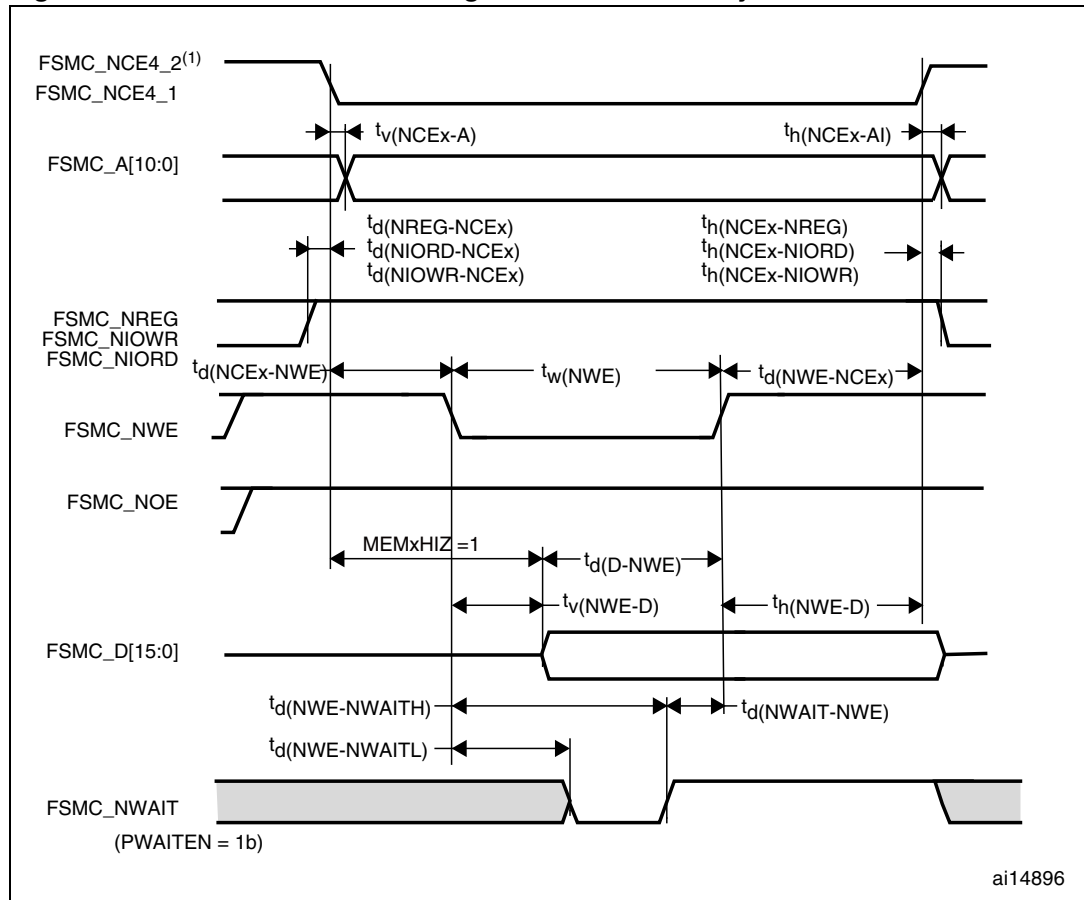
1. TBD = to be determined.

Figure 30. PC-card controller timing for common memory read access



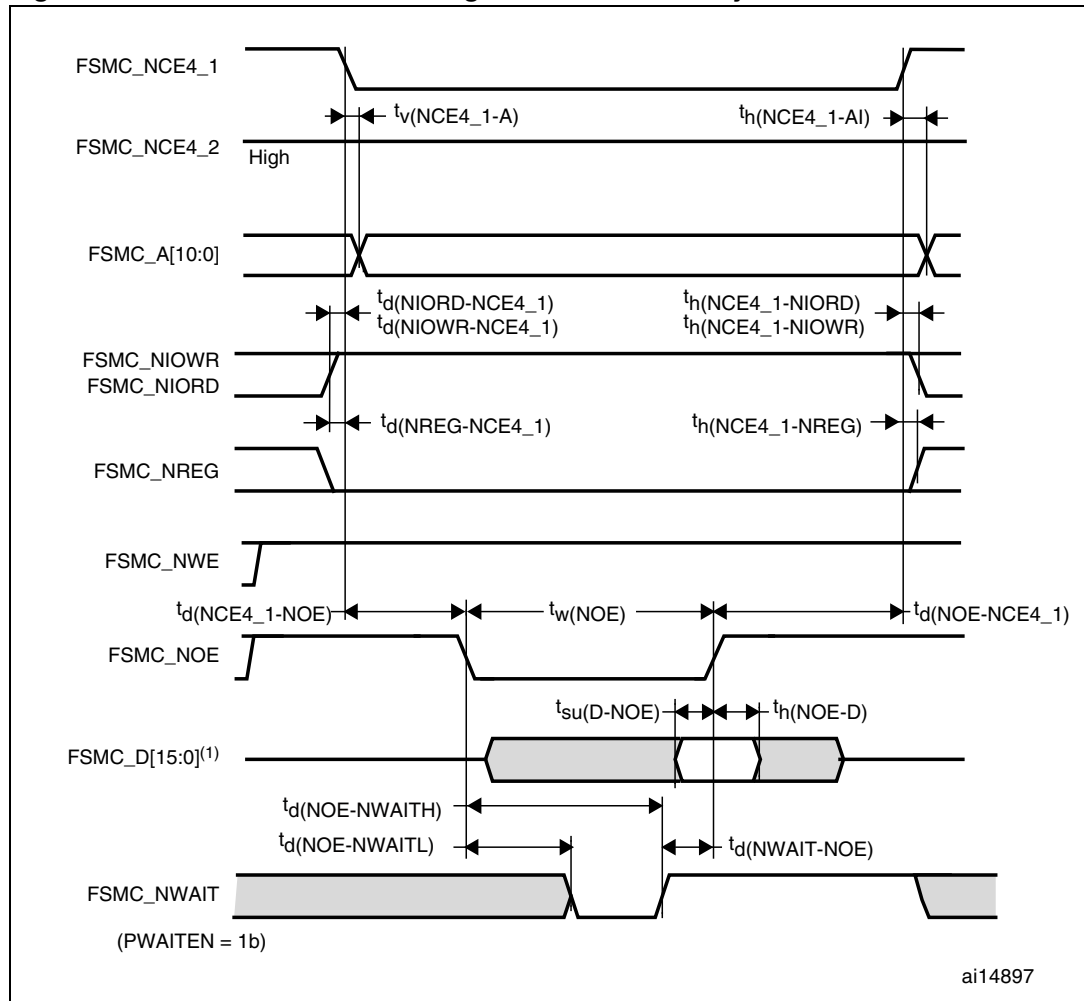
1. FSMC_NCE4_2 remains high (inactive during 8-bit access).

Figure 31. PC-card controller timing for common memory write access



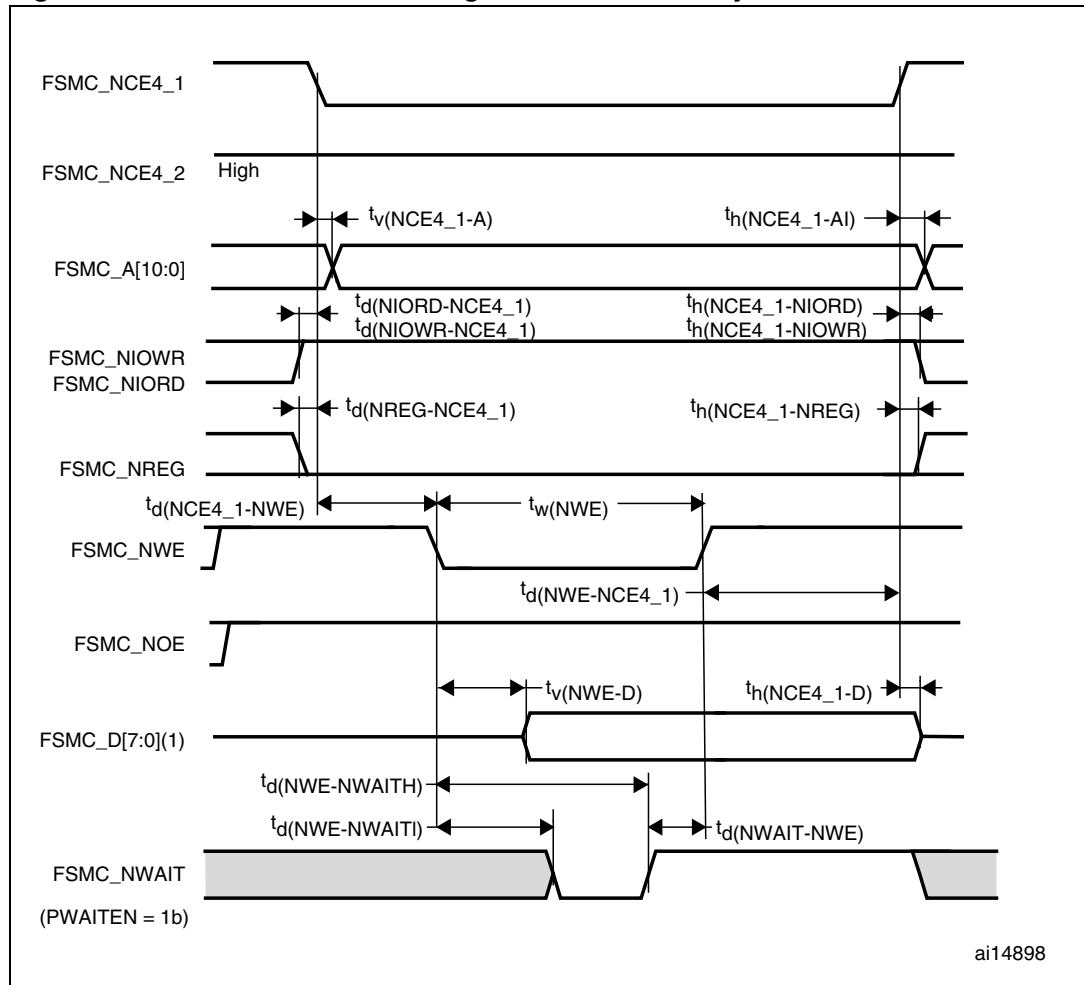
1. FSMC_NCE4_2 remains high (inactive during 8-bit access).

Figure 32. PC-card controller timing for attribute memory read access



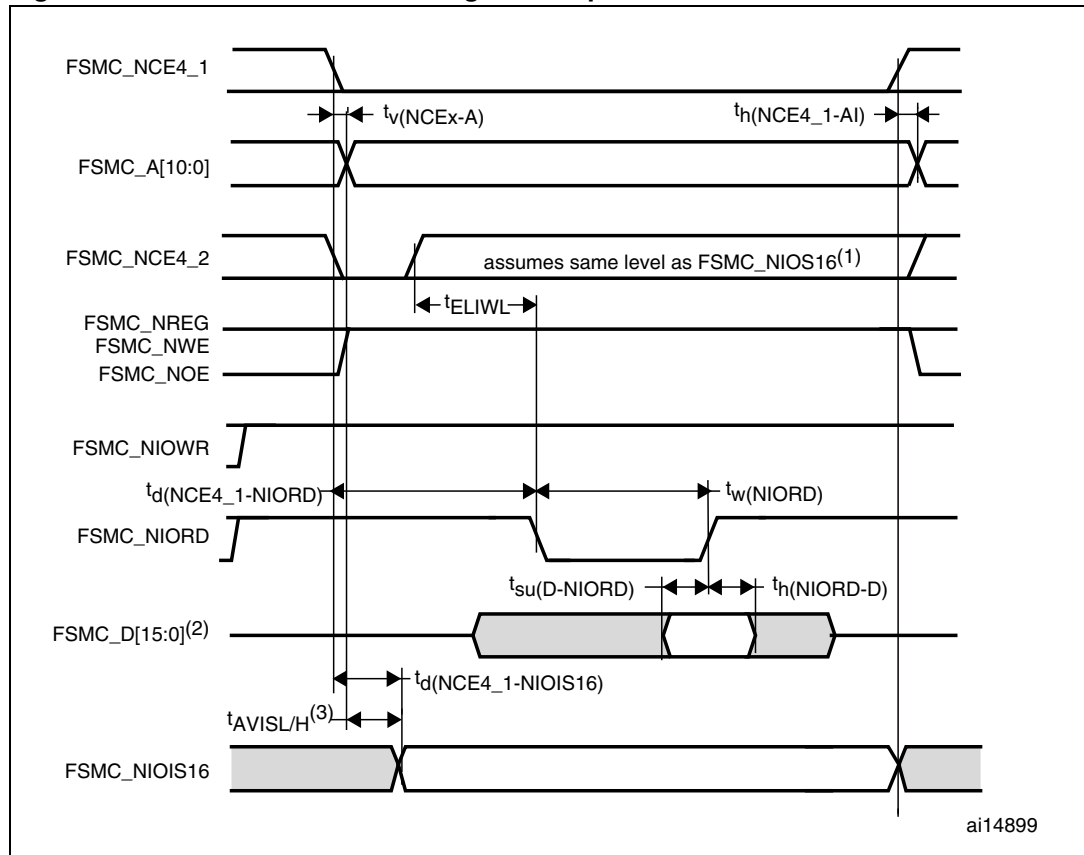
1. Only data bits 0...7 are read (bits 8...15 are disregarded).

Figure 33. PC-card controller timing for attribute memory write access



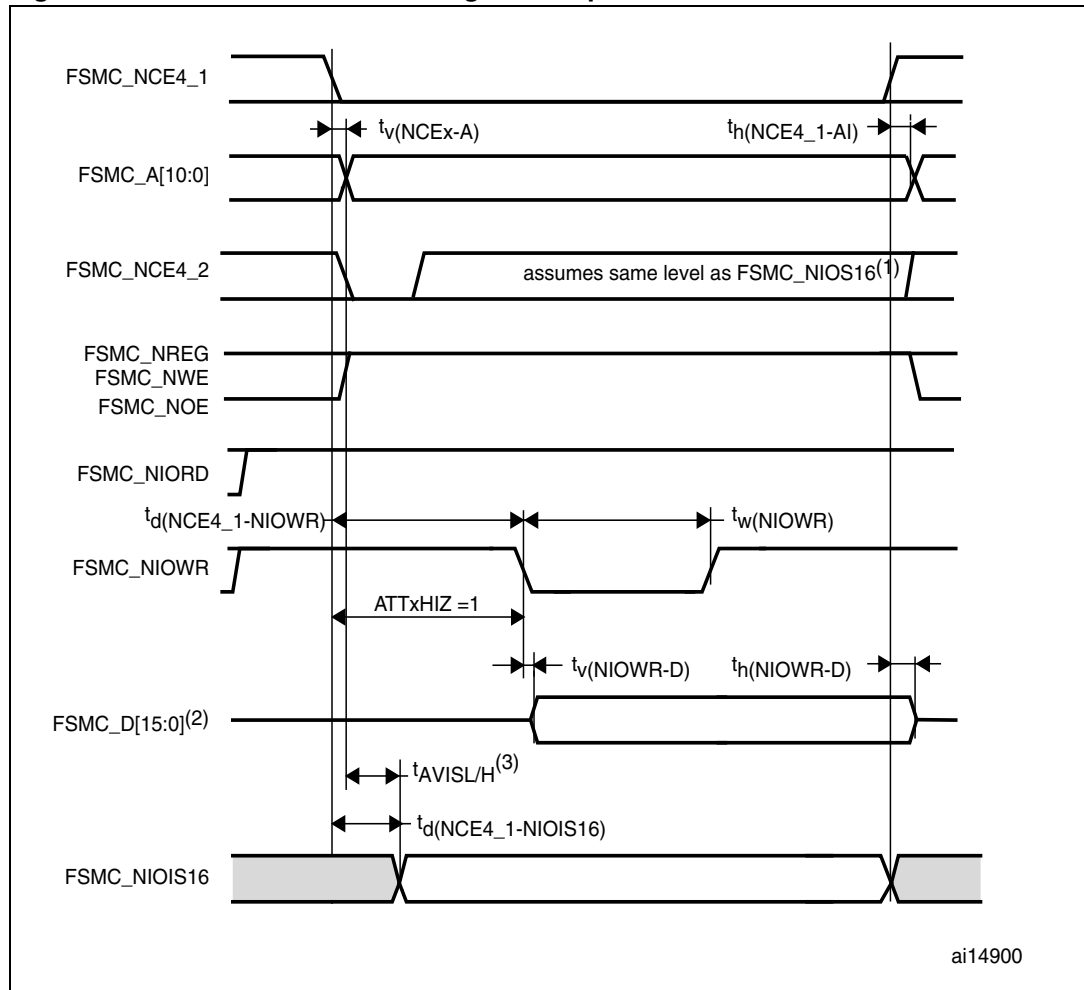
1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

Figure 34. PC-card controller timing for I/O space read access



1. FSMC_NCE4_2 is high independently of FSMC_NIOIS16 if the AHB transfer is for one byte.
2. Only data bits 0...7 are read (bits 8...15 are disregarded) if FSMC_NIOIS16 is high.
3. The CF card asserts FSMC_NIOIS16 after $t_{AVISL/H}^{(3)}$.
4. FSMC_NWAIT not shown but behaves as in the previous figures.

Figure 35. PC-card controller timing for I/O space write access



1. FSMC_NCE4_2 is high independently of FSMC_NIOIS16 if the AHB transfer is for one byte.
2. Only data bits 0...7 are driven (bits 8...15 remains HiZ) if FSMC_NIOIS16 is high.
3. The CF card asserts FSMC_NIOIS16 after $t_{AVISL/H}$.
4. FSMC_NWAIT not shown but behaves as in the previous figures.

Table 38. Switching characteristics for CF read and write cycles⁽¹⁾

Symbol	Parameter	Timing		Unit
		Min	Max	
$t_{v(NCEx-A)}$ $t_{v(NCE4_1-A)}$	FSMC_NCEx low (x = 4_1/4_2) to FSMC_Ay valid (y = 0...10) FSMC_NCE4_1 low (x = 4_1/4_2) to FSMC_Ay valid (y = 0...10)	-	TBD	ns
$t_{h(NCEx-AI)}$ $t_{h(NCE4_1-AI)}$	FSMC_NCEx high (x = 4_1/4_2) to FSMC_Ax invalid (x = 0...10) FSMC_NCE4_1 high (x = 4_1/4_2) to FSMC_Ax invalid (x = 0...10)	TBD	-	ns
$t_{d(NREG-NCEx)}$ $t_{d(NREG-NCE4_1)}$	FSMC_NCEx low to FSMC_NREG valid FSMC_NCE4_1 low to FSMC_NREG valid	-	TBD	ns
$t_{h(NCEx-NREG)}$ $t_{h(NCE4_1-NREG)}$	FSMC_NCEx high to FSMC_NREG invalid FSMC_NCE4_1 high to FSMC_NREG invalid	TBD	-	ns
$t_{d(NIORD-NCEx)}$ $t_{d(NIORD-NCE4_1)}$	FSMC_NCEx low to FSMC_NIORD valid FSMC_NCE4_1 low to FSMC_NIORD valid	-	TBD	ns
$t_{h(NCEx-NIORD)}$ $t_{h(NCE4_1-NIORD)}$	FSMC_NCEx high to FSMC_NIORD invalid FSMC_NCE4_1 high to FSMC_NIORD invalid	TBD	-	ns
$t_{d(NIOWR-NCEx)}$ $t_{d(NIOWR-NCE4_1)}$	FSMC_NIOWR valid to FSMC_NCEx low FSMC_NIOWR valid to FSMC_NCE4_1 low			
$t_{h(NCEx-NIOWR)}$ $t_{h(NCE4_1-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid FSMC_NCE4_1 high to FSMC_NIOWR invalid			
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	TBD	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	TBD	-	ns
$t_{d(D-NWE)}$	FSMC_D[15:0] valid before FSMC_NWE high	TBD	-	ns
$t_{d(NCE4_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	TBD	ns
$t_w(NIOWR)$	FSMC_NIOWR low width	TBD	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	TBD	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	TBD	-	ns
$t_{d(NCE4_1-NIOIS16)}$	FSMC_NIOS16 valid after FSMC_NCE4_1 low	-	TBD	ns
$t_{d(NCE4_1-NOE)}$	FSMC_NCE4_1 low to FSMC_NOE low	-	TBD	ns
$t_w(NOE)$	FSMC_NOE low width	TBD	TBD	cycles/ns
$t_{d(NOE-NCEx)}$ $t_{d(NOE-NCE4_1)}$	FSMC_NOE high to FSMC_NCEx high FSMC_NOE high to FSMC_NCE4_1 high	TBD		
$t_{d(NOE-NWAITL)}$	FSMC_NWAIT low after FSMC_NOE low ⁽²⁾		TBD	
$t_{d(NOE-NWAITH)}$	FSMC_NWAIT high after FSMC_NOE low ⁽²⁾	TBD		
$t_{d(NWAIT-NOE)}$	FSMC_NOE high after FSMC_NWAIT high	TBD	-	ns
$t_{su(D-NOE)}$	FSMC_D[15:0] valid data before FSMC_NOE high	TBD	-	ns
$t_{h(NOE-D)}$	FSMC_D[15:0] valid data after FSMC_NOE high	TBD	-	ns

Table 38. Switching characteristics for CF read and write cycles⁽¹⁾ (continued)

Symbol	Parameter	Timing		Unit
		Min	Max	
$t_{d(NCEx-NWE)}$	FSMC_NCE _x low to FSMC_NWE low	-	TBD	ns
$t_{w(NWE)}$	FSMC_NWE low width	TBD	TBD	cycles/ns
$t_{d(NWE-NCEx)}$ $t_{d(NWE-NCE4_1)}$	FSMC_NWE high to FSMC_NCE _x high FSMC_NWE high to FSMC_NCE4_1 high	TBD		ns
$t_{d(NCE4_1-NWE)}$	FSMC_NCE4_1 low to FSMC_NWE low			ns
$t_{d(NWE-NWAITL)}$	FSMC_NWAIT low after FSMC_NWE low ⁽²⁾		TBD	ns
$t_{d(NWE-NWAITH)}$	FSMC_NWAIT high after FSMC_NWE low ⁽²⁾	TBD		ns
$t_{d(NWAIT-NWE)}$	FSMC_NWE high after FSMC_NWAIT high	TBD	-	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	TBD	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	TBD	-	ns
$t_{h(NCE4_1-D)}$	FSMC_NCE4_1 high to FSMC_D[15:0] invalid			ns
$t_{w(NIORD)}$	FSMC_NIORD low width			ns
t_{ELIWL}	FSMC_NCE _x setup before FSMC_NWE low			ns
$t_{AVISL/H}$	Address valid to FSMC_NIOIS16 valid		35	ns

1. TBD = to be determined.

2. When one or more wait states are inserted. If no wait state needs inserted, NWAIT should be kept high or the wait feature should be disabled (WAITEN=0) in the control register.

Figure 36. NAND controller timing for read access

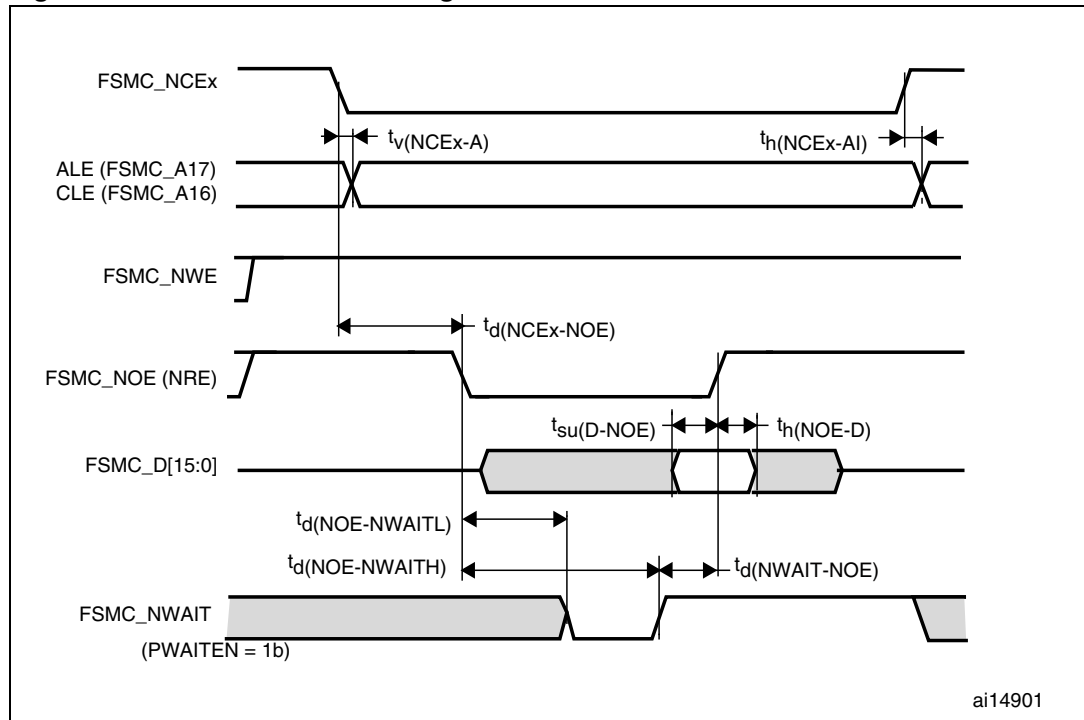


Figure 37. NAND controller timing for write access

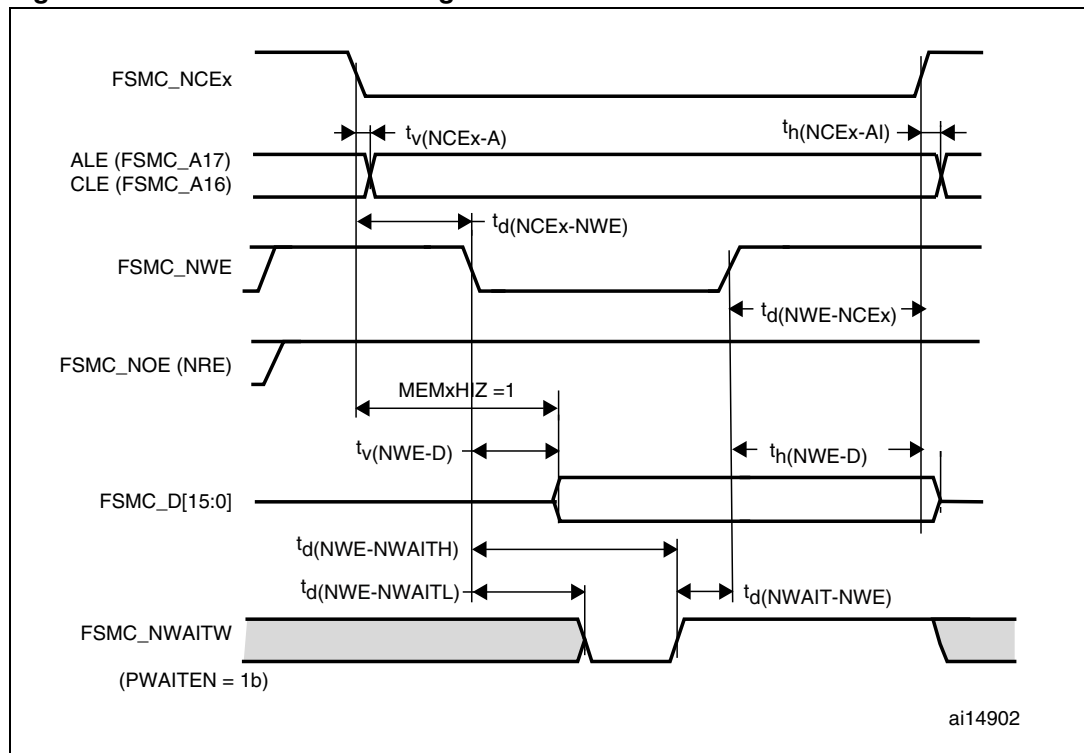


Figure 38. NAND controller timing for common memory read access

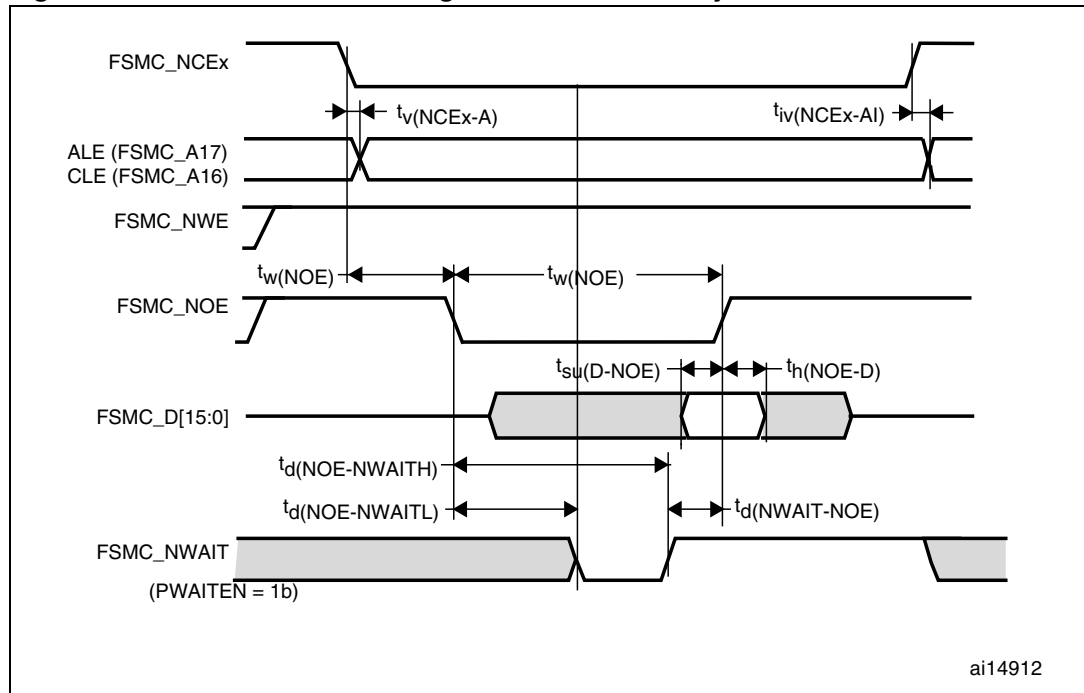


Figure 39. NAND controller timing for common memory write access

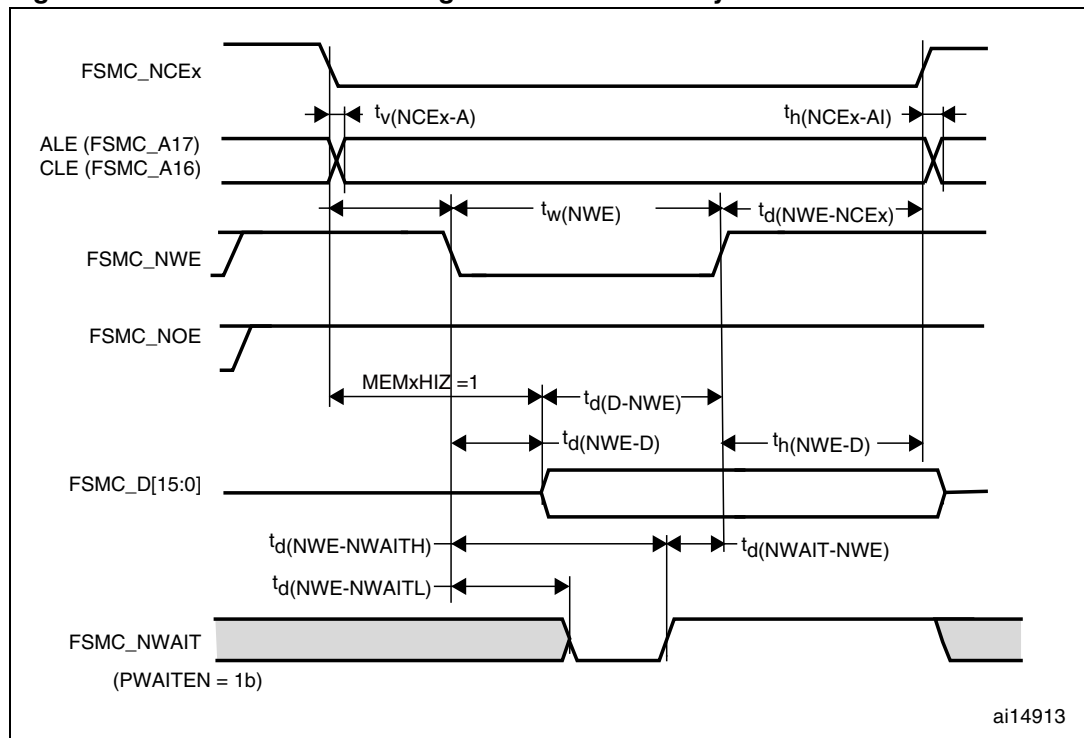


Table 39. Switching characteristics for NAND Flash read and write cycles⁽¹⁾

Symbol	Parameter	Timing		Unit
		Min	Max	
t _{v(NCEx-A)}	FSMC_NCEx low (x = 2/3) to FSMC_Ay valid (y = 16/17)	-	TBD	ns
t _{h(NCEx-AI)}	FSMC_NCEx high (x = 2/3) to FSMC_Ax invalid (x = 16/17)	TBD	-	ns
t _{d(D-NWE)}	FSMC_D[15:0] valid before FSMC_NWE high	TBD	-	ns
t _{d(NWE-D)}	FSMC_D[15:0] valid after FSMC_NWE high	TBD	-	ns
t _{d(NCEx-NOE)}	FSMC_NCEx low to FSMC_NOE low	-	TBD	ns
t _{w(NOE)}	FSMC_NOE low width	TBD	TBD	cycles/ns
t _{h(NWE-D)}	FSMC_NWE high to FSMC_D[15:0] invalid			ns
t _{d(NOE-NWAITL)}	FSMC_NWAIT low after FSMC_NOE low ⁽²⁾		TBD	
t _{d(NOE-NWAITH)}	FSMC_NWAIT high after FSMC_NOE low ⁽²⁾	TBD		
t _{d(NWAIT-NOE)}	FSMC_NOE high after FSMC_NWAIT high	TBD	-	ns
t _{su(D-NOE)}	FSMC_D[15:0] valid data before FSMC_NOE high	TBD	-	ns
t _{h(NOE-D)}	FSMC_D[15:0] valid data after FSMC_NOE high	TBD	-	ns
t _{d(NCEx-NWE)}	FSMC_NCEx low to FSMC_NWE low	-	TBD	ns
t _{w(NWE)}	FSMC_NWE low width	TBD	TBD	cycles/ns
t _{d(NWE-NCEx)}	FSMC_NWE high to FSMC_NCEx high	TBD		ns
t _{d(NWE-NWAITL)}	FSMC_NWAIT low after FSMC_NWE low ⁽²⁾		TBD	ns
t _{d(NWE-NWAITH)}	FSMC_NWAIT high after FSMC_NWE low ⁽²⁾	TBD		ns
t _{d(NWAIT-NWE)}	FSMC_NWE high after FSMC_NWAIT high	TBD	-	ns
t _{v(NWE-D)}	FSMC_NWE low to FSMC_D[15:0] valid	-	TBD	ns
t _{h(NWE-D)}	FSMC_NWE high to FSMC_D[15:0] invalid	TBD	-	ns

1. TBD = to be determined.

2. When one or more wait states are inserted. If no wait state needs inserted, NWAIT should be kept high or the wait feature should be disabled (WAITEN=0) in the control register.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 1000-4-2 standard.
- **FTB: A Burst of Fast Transient voltage** (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 40](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 40. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 48\text{ MHz}$ conforms to IEC 1000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 48\text{ MHz}$ conforms to IEC 1000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE J 1752/3 standard which specifies the test board and the pin loading.

Table 41. EMI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f _{HSE} /f _{HCLK}]		Unit
				8/48 MHz	8/72 MHz	
S _{EMI}	Peak level	V _{DD} = 3.3 V, T _A = 25 °C, LQFP100 package compliant with SAE J 1752/3	0.1 to 30 MHz	TBD	TBD	dBμV
			30 to 130 MHz	TBD	TBD	
			130 MHz to 1GHz	TBD	TBD	
			SAE EMI Level	TBD	TBD	-

1. TBD = to be determined.

5.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 42. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C conforming to JESD22-A114	2	2000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	T _A = +25 °C conforming to JESD22-C101	II	500	

1. Values based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 43. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105\text{ }^\circ\text{C}$ conforming to JESD78A	II level A

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 44](#) are derived from tests performed under the conditions summarized in [Table 9](#). All I/Os are CMOS and TTL compliant.

Table 44. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage ⁽¹⁾	TTL ports	-0.5		0.8	V
V_{IH}	Standard IO input high level voltage ⁽¹⁾		2		$V_{DD}+0.5$	
	IO FT ⁽²⁾ input high level voltage ⁽¹⁾		2		5.5V	
V_{IL}	Input low level voltage ⁽¹⁾	CMOS ports	-0.5		$0.35 V_{DD}$	V
V_{IH}	Input high level voltage ⁽¹⁾		$0.65 V_{DD}$		$V_{DD}+0.5$	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis ⁽³⁾		200			mV
	IO FT Schmitt trigger voltage hysteresis ⁽³⁾		$5\% V_{DD}$ ⁽⁴⁾			mV
I_{lkg}	Input leakage current ⁽⁵⁾	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os			± 1	μA
		$V_{IN} = 5\text{ V}$ I/O FT			3	
R_{PU}	Weak pull-up equivalent resistor ⁽⁶⁾	$V_{IN} = V_{SS}$	30	40	50	$\text{k}\Omega$
R_{PD}	Weak pull-down equivalent resistor ⁽⁶⁾	$V_{IN} = V_{DD}$	30	40	50	$\text{k}\Omega$
C_{IO}	I/O pin capacitance			5		pF

1. Values based on characterization results, and not tested in production.

2. FT = Five-volt tolerant.

3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.

4. With a minimum of 100 mV.

5. Leakage could be higher than max. if negative current is injected on adjacent pins.

6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink +20 mA (with a relaxed V_{OL}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating I_{VDD} (see [Table 7](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see [Table 7](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 45](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 9](#). All I/Os are CMOS and TTL compliant.

Table 45. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$		0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-0.4$		
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$		0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4		
$V_{OL}^{(1)(3)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$		1.3	V
$V_{OH}^{(2)(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-1.3$		
$V_{OL}^{(1)(3)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	$I_{IO} = +6 \text{ mA}$ $2 \text{ V} < V_{DD} < 2.7 \text{ V}$		0.4	V
$V_{OH}^{(2)(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		$V_{DD}-0.4$		

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 7](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 7](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
3. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 40](#) and [Table 46](#), respectively.

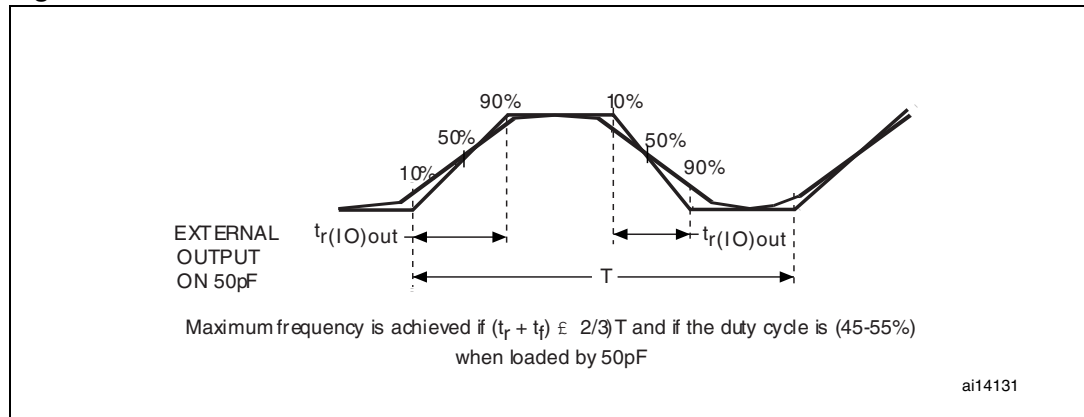
Unless otherwise specified, the parameters given in [Table 46](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 9](#).

Table 46. I/O AC characteristics⁽¹⁾

MODEx[1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$		2	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$		125 ⁽³⁾	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time			125 ⁽³⁾	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$		10	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$		25 ⁽³⁾	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time			25 ⁽³⁾	
11	$F_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		50	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		30	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$		20	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		5 ⁽³⁾	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		8 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$		12 ⁽³⁾	
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		5 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		8 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$		12 ⁽³⁾	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller		10		ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 40](#).
3. Values based on design simulation and validated on silicon, not tested in production.

Figure 40. I/O AC characteristics definition



5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 44](#)).

Unless otherwise specified, the parameters given in [Table 47](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 9](#).

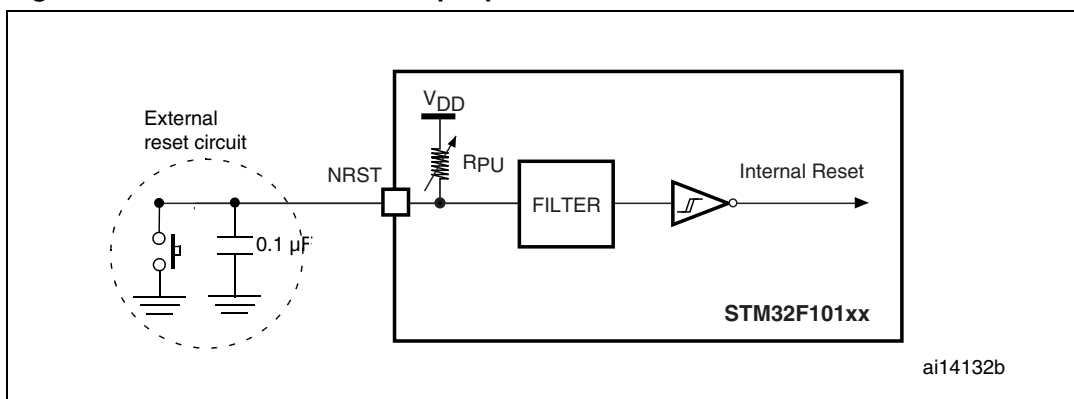
Table 47. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage		-0.5		0.8	V
$V_{IH(NRST)}$	NRST Input high level voltage		2		$V_{DD}+0.5$	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			200		
R_{PU}	Weak pull-up equivalent resistor ⁽¹⁾	$V_{IN} = V_{SS}$	30	40	50	$k\Omega$
$V_{F(NRST)}$	NRST Input filtered pulse ⁽²⁾				100	ns
$V_{NF(NRST)}$	NRST Input not filtered pulse ⁽²⁾		300			ns

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

2. Values guaranteed by design, not tested in production.

Figure 41. Recommended NRST pin protection



- 5. The reset network protects the device against parasitic resets.
- 6. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 47](#). Otherwise the reset will not be taken into account by the device.

5.3.15 TIM timer characteristics

The parameters given in [Table 48](#) are guaranteed by fabrication.

Refer to [Section 5.3.13: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 48. TIMx⁽¹⁾ characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72 \text{ MHz}$	13.9		ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 72 \text{ MHz}$	0	36	MHz
Res_{TIM}	Timer resolution			16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72 \text{ MHz}$	0.0139	910	μs
t_{MAX_COUNT}	Maximum possible count			65536×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72 \text{ MHz}$		59.6	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

5.3.16 Communications interfaces

I²C interface characteristics

Unless otherwise specified, the parameters given in [Table 49](#) are derived from tests performed under ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in [Table 9](#).

The STM32F103xC performance line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

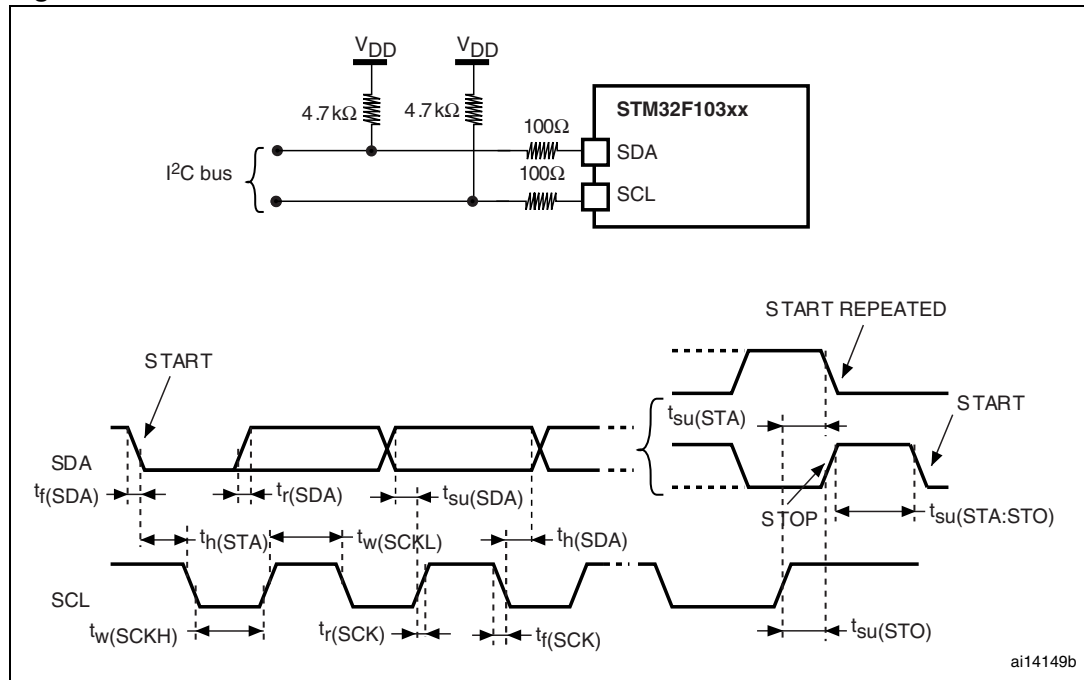
The I²C characteristics are described in [Table 49](#). Refer also to [Section 5.3.13: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

Table 49. I²C characteristics

Symbol	Parameter	Standard mode I ² C ⁽¹⁾		Fast mode I ² C ⁽¹⁾⁽²⁾		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		μ s
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0 ⁽³⁾		0 ⁽⁴⁾	900 ⁽³⁾	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$	300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		μ s
$t_{su(STA)}$	Repeated Start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		μ s
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7		1.3		μ s
C_b	Capacitive load for each bus line		400		400	pF

1. Values based on standard I²C protocol requirement, not tested in production.
2. f_{PCLK1} must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 4 MHz to achieve the maximum fast mode I²C frequency.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 42. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

Table 50. SCL frequency (f_{PCLK1} = 36 MHz, V_{DD} = 3.3 V)⁽¹⁾⁽²⁾⁽³⁾

f _{SCL} (kHz)	I2C_CCR value
	R _P = 4.7 kΩ
400	TBD
300	TBD
200	TBD
100	TBD
50	TBD
20	TBD

1. TBD = to be determined.
2. R_P = External pull-up resistance, f_{SCL} = I²C speed,
3. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

I²S - SPI characteristics

Unless otherwise specified, the parameters given in [Table 51](#) for SPI or in [Table 52](#) for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 9](#).

Refer to [Section 5.3.13: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 51. SPI characteristics^{(1) (2)}

Symbol	Parameter	Conditions	Min	Max	Unit
f _{SCK} 1/t _{c(SCK)}	SPI clock frequency	Master mode	0	18	MHz
		Slave mode	0	18	
t _{r(SCK)} t _{f(SCK)}	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
t _{su(NSS)} ⁽³⁾	NSS setup time	Slave mode	t _{c(SCK)}		
t _{h(NSS)} ⁽³⁾	NSS hold time	Slave mode	0.5t _{c(SCK)}		
t _{w(SCKH)} ⁽³⁾ t _{w(SCKL)} ⁽³⁾	SCK high and low time	Master mode, f _{PCLK} = 36 MHz, presc = 4	50	60	
t _{su(MI)} ⁽³⁾ t _{su(SI)} ⁽³⁾	Data input setup time	Master mode	10		
		Slave mode	5		
t _{h(MI)} ⁽³⁾ t _{h(SI)} ⁽³⁾	Data input hold time	Master mode, f _{PCLK} = 36 MHz, presc = 4	15		
		Slave mode, f _{PCLK} = 36 MHz, presc = 4	5		
		Master mode, f _{PCLK} = TBD	TBD ⁽⁴⁾		
		Slave mode, f _{PCLK} = TBD	TBD ⁽⁴⁾		
t _{a(SO)} ⁽³⁾⁽⁵⁾	Data output access time	Slave mode, f _{PCLK} = 36 MHz, presc = 4	0	60	
		Slave mode, f _{PCLK} = TBD	0	TBD	
t _{dis(SO)} ⁽³⁾⁽⁶⁾	Data output disable time	Slave mode	5	TBD	
t _{v(SO)} ⁽³⁾⁽¹⁾	Data output valid time	Slave mode (after enable edge), f _{PCLK} = 36 MHz, presc = 4		30	
		f _{PCLK} = TBD		TBD	
t _{v(MO)} ⁽³⁾⁽¹⁾	Data output valid time	Master mode (after enable edge), f _{PCLK} = 36 MHz, presc = 4		10	
		f _{PCLK} = TBD	TBD	TBD	
t _{h(SO)} ⁽³⁾	Data output hold time	Slave mode (after enable edge)	30		
t _{h(MO)} ⁽³⁾		Master mode (after enable edge)	10		

1. TBD = to be determined.
2. Remapped SPI1 characteristics to be determined.
3. Values based on design simulation and/or characterization results, and not tested in production.
4. Depends on f_{PCLK}. For example, if f_{PCLK} = 8MHz, then t_{PCLK} = 1/f_{PCLK} = 125 ns and t_{v(MO)} = 255 ns.
5. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
6. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 43. SPI timing diagram - slave mode and CPHA = 0

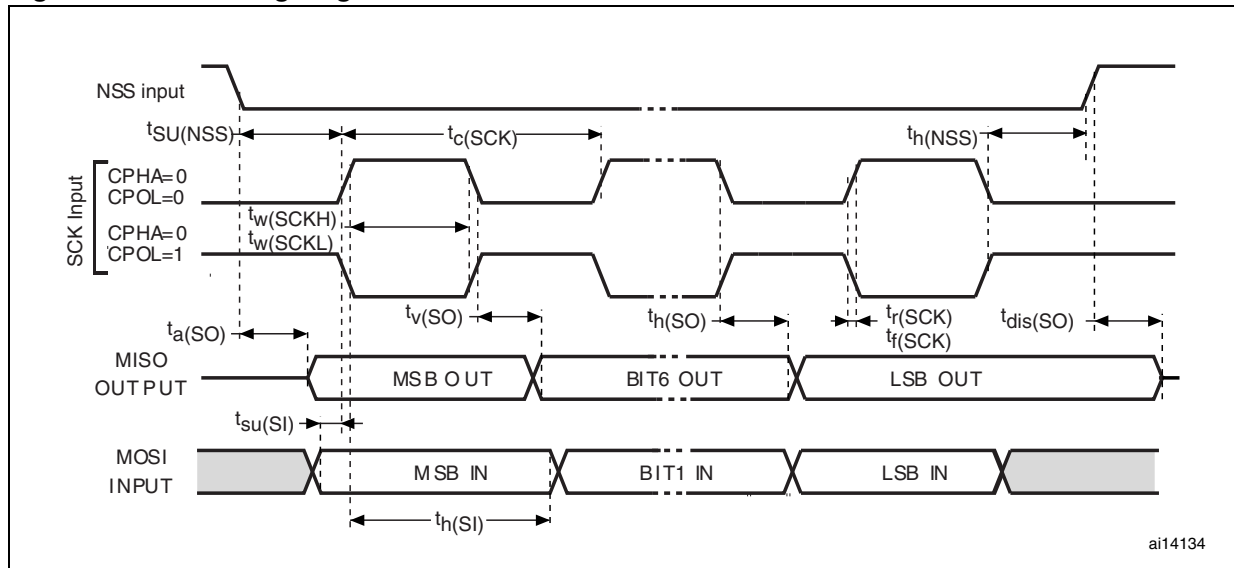
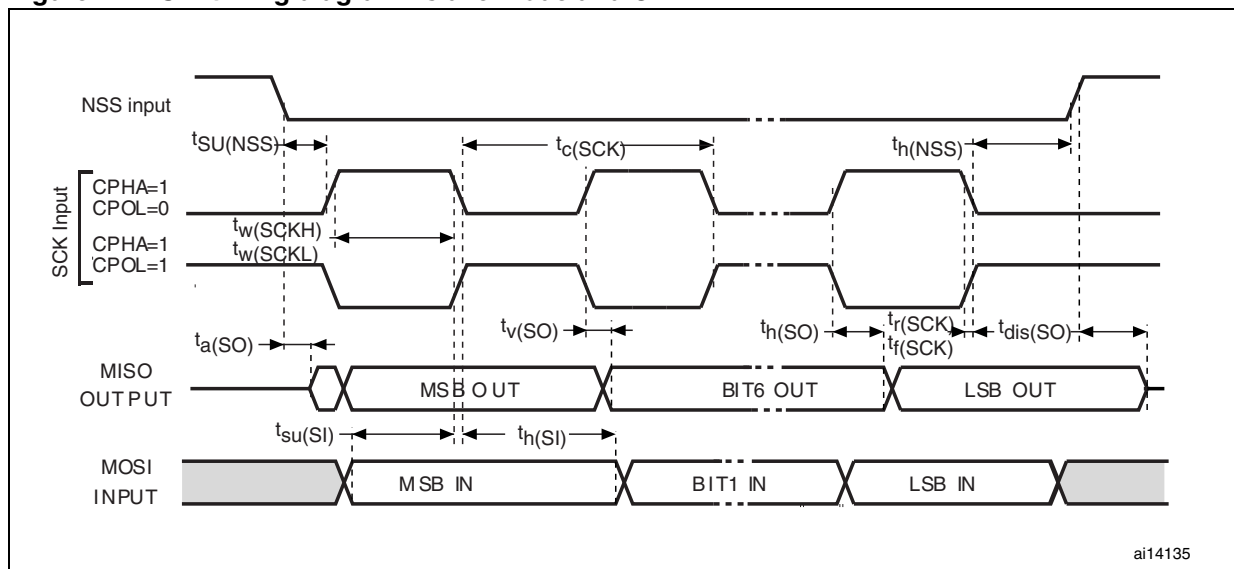
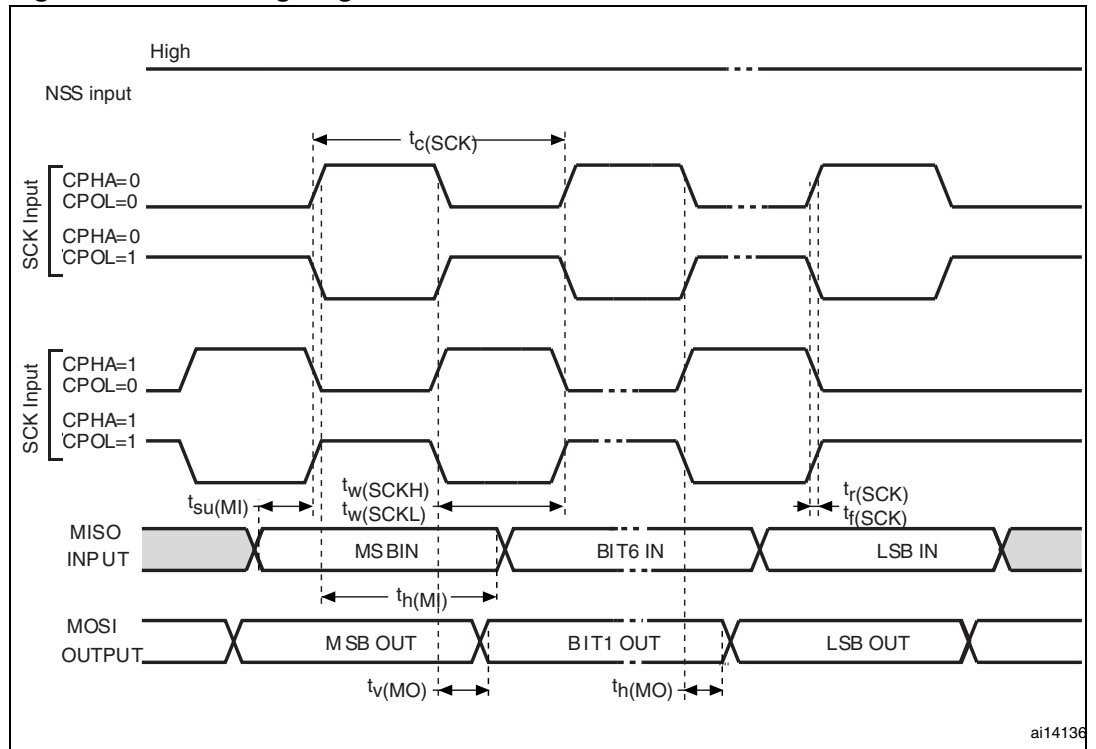


Figure 44. SPI timing diagram - slave mode and CPHA = 1⁽¹⁾



1. Measurement points are done at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

Figure 45. SPI timing diagram - master mode⁽¹⁾



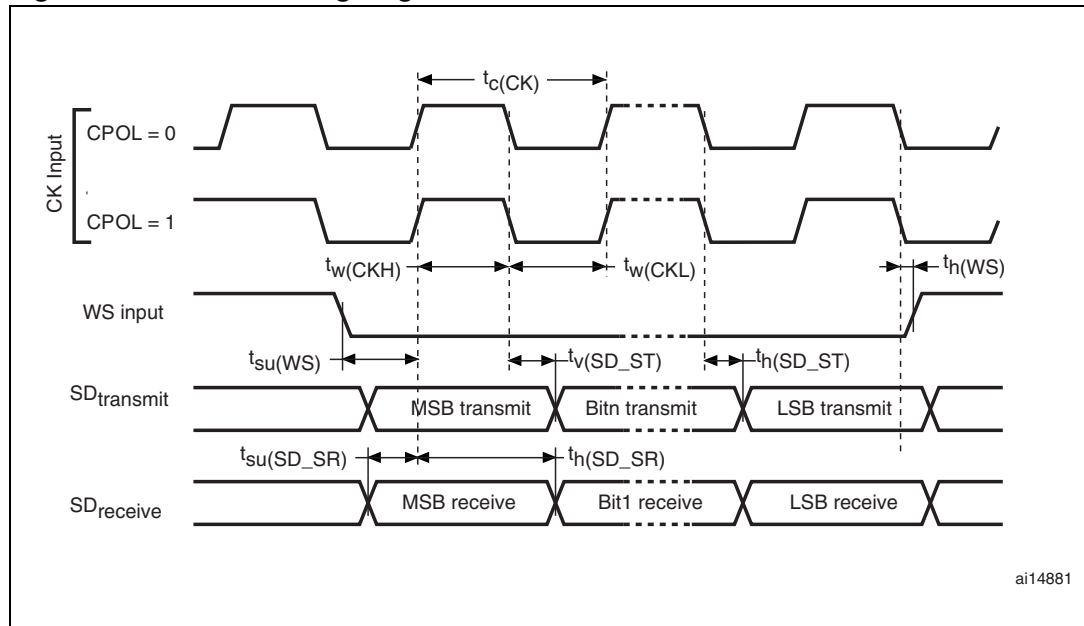
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 52. I²S characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
f _{CK} 1/t _{c(CK)}	I ² S clock frequency	Master	TBD	TBD	MHz
		Slave	0	TBD	
t _{r(CK)} t _{f(CK)}	I ² S clock rise and fall time	capacitive load C _L = 50 pF		TBD	ns
t _{v(WS)} ⁽²⁾	WS valid time	Master	TBD		
t _{h(WS)} ⁽²⁾	WS hold time	Master	TBD		
t _{su(WS)} ⁽²⁾	WS setup time	Slave	TBD		
t _{h(WS)} ⁽²⁾	WS hold time	Slave	TBD		
t _{w(CKH)} ⁽²⁾ t _{w(CKL)} ⁽²⁾	CK high and low time	Master f _{PCLK} = TBD, presc = TBD	TBD		
t _{su(SD_MR)} ⁽²⁾ t _{su(SD_SR)} ⁽²⁾	Data input setup time	Master receiver Slave receiver	TBD TBD		
t _{h(SD_MR)} ⁽²⁾⁽³⁾ t _{h(SD_SR)} ⁽²⁾⁽³⁾	Data input hold time	Master receiver Slave receiver	TBD TBD		
t _{h(SD_MR)} ⁽²⁾ t _{h(SD_SR)} ⁽²⁾	Data input hold time	Master f _{PCLK} = TBD Slave f _{PCLK} = TBD	TBD TBD		
t _{v(SD_ST)} ⁽²⁾⁽³⁾	Data output valid time	Slave transmitter (after enable edge)		TBD	
		f _{PCLK} = TBD		TBD	
t _{h(SD_ST)} ⁽²⁾	Data output hold time	Slave transmitter (after enable edge)	TBD		
t _{v(SD_MT)} ⁽²⁾⁽³⁾	Data output valid time	Master transmitter (after enable edge)		TBD	
		f _{PCLK} = TBD	TBD	TBD	
t _{h(SD_MT)} ⁽²⁾	Data output hold time	Master transmitter (after enable edge)	TBD		

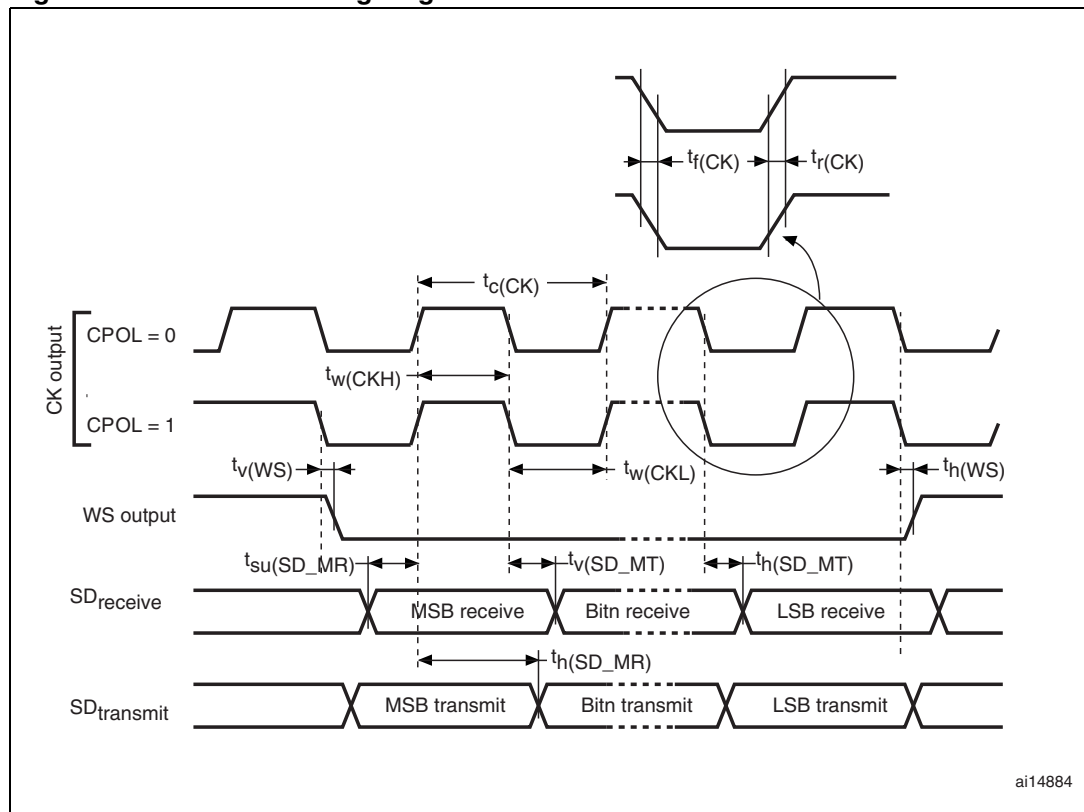
1. TBD = to be determined.
2. Data based on design simulation and/or characterization results, not tested in production.
3. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PCLK} =125 ns.

Figure 46. I²S slave timing diagram⁽¹⁾



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.

Figure 47. I²S master timing diagram⁽¹⁾



1. Data based on design simulation and/or characterization results, not tested in production.

SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in [Table 53](#) are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 9](#).

Refer to [Section 5.3.13: I/O port characteristics](#) for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 48. SDIO high-speed mode

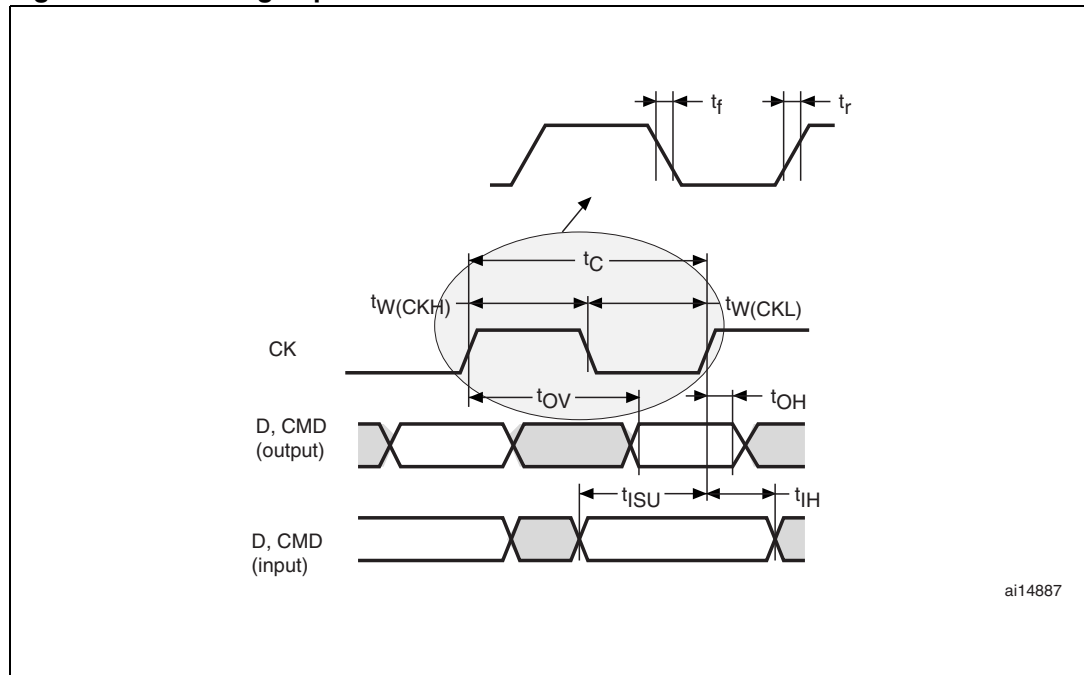


Figure 49. SD default mode

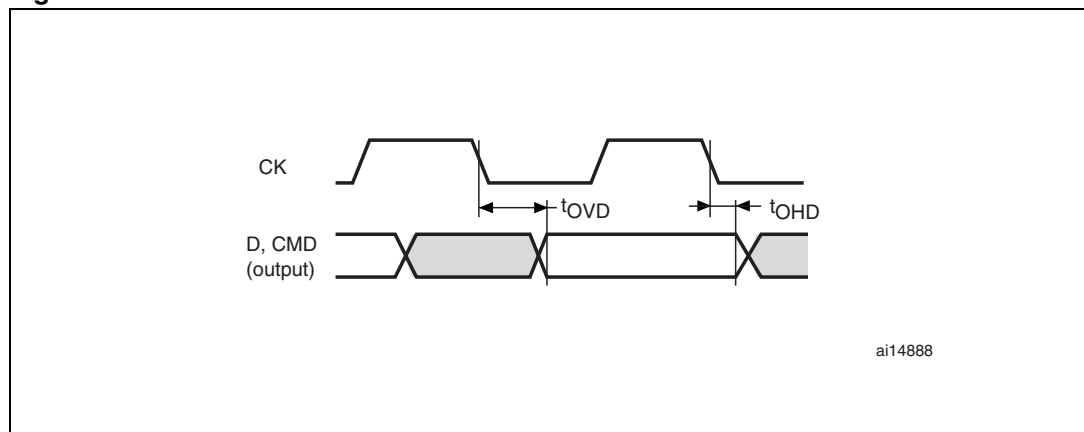


Table 53. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f _{PP}	Clock frequency in data transfer mode	C _L ≤ 30 pF	0	TBD	MHz
t _{W(CKL)}	Clock low time	C _L ≤ 30 pF	TBD		ns
t _{W(CKH)}	Clock high time	C _L ≤ 30 pF	TBD		
t _r	Clock rise time	C _L ≤ 30 pF		TBD	
t _f	Clock fall time	C _L ≤ 30 pF		TBD	
t _C					
CMD, D inputs (referenced to CK)					
t _{ISU}	Input setup time	C _L ≤ 30 pF	TBD		ns
t _{IH}	Input hold time	C _L ≤ 30 pF	TBD		
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t _{OV}	Output valid time	C _L ≤ 30 pF		TBD	ns
t _{OH}	Output hold time	C _L ≤ 30 pF	TBD		
CMD, D outputs (referenced to CK) in SD default mode⁽¹⁾					
t _{OVD}	Output valid default time	C _L ≤ 30 pF		TBD	ns
t _{OHD}	Output hold default time	C _L ≤ 30 pF	TBD		

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 54. USB startup time

Symbol	Parameter	Max	Unit
t _{STARTUP}	USB transceiver startup time	1	μs

Table 55. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
Input levels					
V _{USB}	USB voltage ⁽²⁾	Within V _{DD} voltage range	3.0 ⁽³⁾	3.6	V
V _{DI} ⁽⁴⁾	Differential input sensitivity	I(USBDP, USBDM)	0.2		V
V _{CM} ⁽⁴⁾	Differential common mode range	Includes V _{DI} range	0.8	2.5	
V _{SE} ⁽⁴⁾	Single ended receiver threshold		1.3	2.0	
Output levels					
V _{OL}	Static output level low	R _L of 1.5 kΩ to 3.6 V ⁽⁵⁾		0.3	V
V _{OH}	Static output level high	R _L of 15 kΩ to V _{SS} ⁽⁵⁾	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F103xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by characterization, not tested in production.
5. R_L is the load connected on the USB drivers

Figure 50. USB timings: definition of data signal rise and fall time

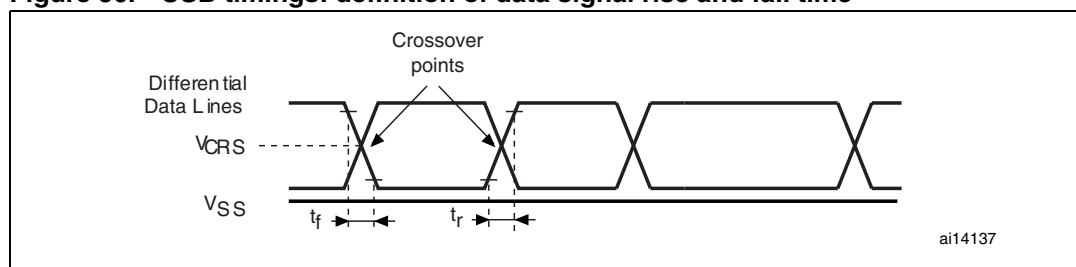


Table 56. USB: full-speed electrical characteristics

Driver characteristics ⁽¹⁾					
Symbol	Parameter	Conditions	Min	Max	Unit
t _r	Rise time ⁽²⁾	C _L = 50 pF	4	20	ns
t _f	Fall Time ⁽²⁾	C _L = 50 pF	4	20	ns
t _{rfm}	Rise/ fall time matching	t _r /t _f	90	110	%
V _{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by characterization, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

5.3.17 CAN (controller area network) interface

Refer to [Section 5.3.13: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CANTX and CANRX).

5.3.18 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 57](#) are derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 9](#).

Note: It is recommended to perform a calibration after each power-up.

Table 57. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	ADC power supply		2.4		3.6	V
V_{REF+}	Positive reference voltage		2.4		V_{DDA}	V
f_{ADC}	ADC clock frequency		0.6		14	MHz
$f_S^{(1)}$	Sampling rate		0.05		1	MHz
$f_{TRIG}^{(1)}$	External trigger frequency	$f_{ADC} = 14$ MHz			823	kHz
					17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range ⁽²⁾		0 (V_{SSA} or V_{REF-} tied to ground)		V_{REF+}	V
$R_{AIN}^{(1)}$	External input impedance		See Equation 1 and Table 58			k Ω
$R_{ADC}^{(1)}$	Sampling switch resistance				1	k Ω
$C_{ADC}^{(1)}$	Internal sample and hold capacitor				5	pF
$t_{CAL}^{(1)}$	Calibration time	$f_{ADC} = 14$ MHz	5.9			μ s
			83			$1/f_{ADC}$
$t_{lat}^{(1)}$	Injection trigger conversion latency	$f_{ADC} = 14$ MHz			0.214	μ s
					$3^{(3)}$	$1/f_{ADC}$
$t_{latr}^{(1)}$	Regular trigger conversion latency	$f_{ADC} = 14$ MHz			0.143	μ s
					$2^{(3)}$	$1/f_{ADC}$
$t_S^{(1)}$	Sampling time	$f_{ADC} = 14$ MHz	0.107		17.1	μ s
			1.5		239.5	$1/f_{ADC}$
$t_{STAB}^{(1)}$	Power-up time		0	0	1	μ s
$t_{CONV}^{(1)}$	Total conversion time (including sampling time)	$f_{ADC} = 14$ MHz	1		18	μ s
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Guaranteed by design, not tested in production.
2. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA} , depending on the package. Refer to [Section 3: Pin descriptions](#) for further details.
3. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in [Table 57](#).

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_s}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 58. R_{AIN} max for f_{ADC} = 14 MHz⁽¹⁾

T _s (cycles)	t _s (μs)	R _{AIN} max (kΩ)
1.5	0.11	1.2
7.5	0.54	10
13.5	0.96	19
28.5	2.04	41
41.5	2.96	60
55.5	3.96	80
71.5	5.11	104
239.5	17.1	350

1. Data guaranteed by design, not tested in production.

Table 59. ADC accuracy - limited test conditions⁽¹⁾

Symbol	Parameter	Test conditions	Typ	Max ⁽²⁾	Unit
ET	Total unadjusted error ⁽³⁾	f _{PCLK2} = 56 MHz, f _{ADC} = 14 MHz, R _{AIN} < 10 kΩ, V _{DDA} = 3 V to 3.6 V T _A = 25 °C Measurements made after ADC calibration V _{REF+} = V _{DDA}	±1.3	±2	LSB
EO	Offset error ⁽³⁾		±1	±1.5	
EG	Gain error ⁽³⁾		±0.5	±1.5	
ED	Differential linearity error ⁽³⁾		±0.7	±1	
EL	Integral linearity error ⁽³⁾		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. Data based on characterization, not tested in production.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I_{INJ(PIN)} and ΣI_{INJ(PIN)} in [Section 5.3.13](#) does not affect the ADC accuracy.

Table 60. ADC accuracy^{(1) (2)}

Symbol	Parameter	Test conditions	Typ	Max ⁽³⁾	Unit
ET	Total unadjusted error ⁽⁴⁾	$f_{PCLK2} = 56 \text{ MHz}$, $f_{ADC} = 14 \text{ MHz}$, $R_{AIN} < 10 \text{ k}\Omega$ $V_{DDA} = 2.4 \text{ V to } 3.6 \text{ V}$ Measurements made after ADC calibration	± 2	± 5	LSB
EO	Offset error ⁽³⁾		± 1.5	± 25	
EG	Gain error ⁽³⁾		± 1.5	± 3	
ED	Differential linearity error ⁽³⁾		± 1	± 2	
EL	Integral linearity error ⁽³⁾		± 1.5	± 3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD} , frequency, V_{REF} and temperature ranges.
3. Data based on characterization, not tested in production.
4. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 5.3.13](#) does not affect the ADC accuracy.

Figure 51. ADC accuracy characteristics

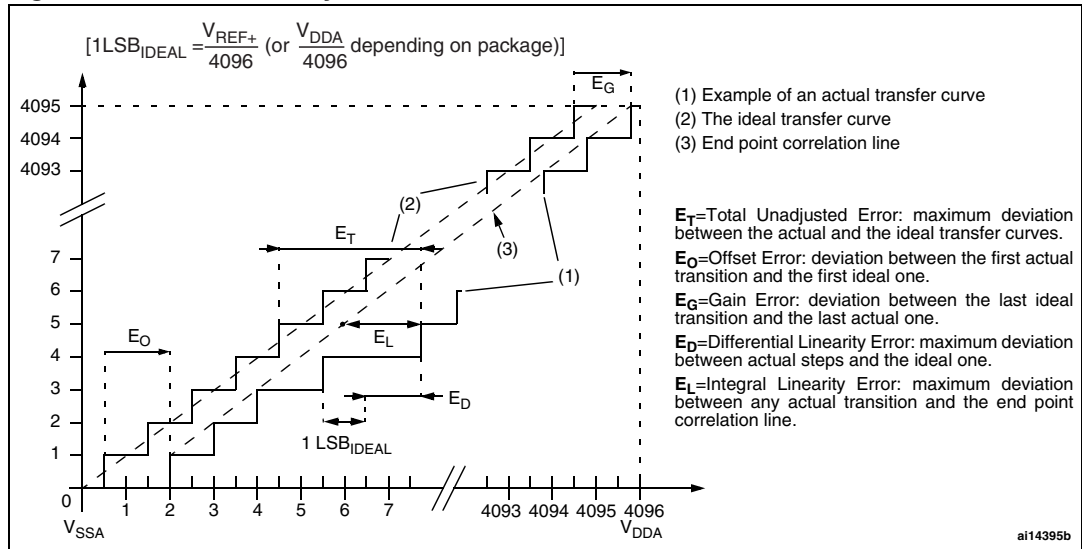
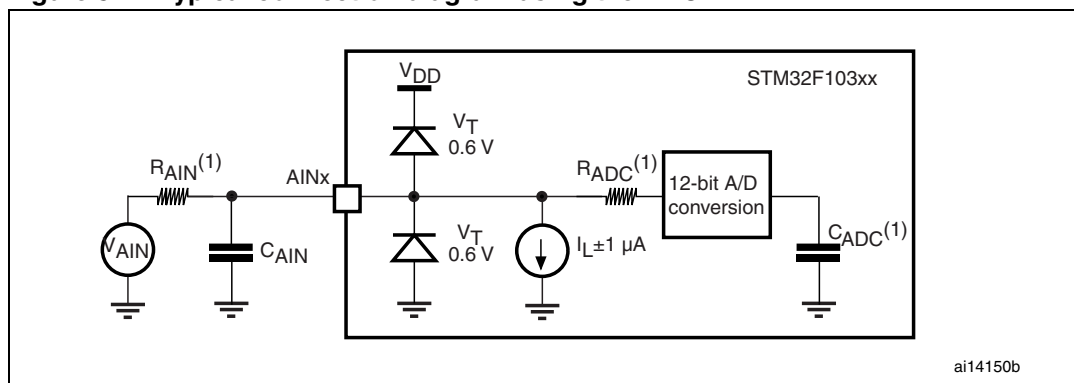


Figure 52. Typical connection diagram using the ADC

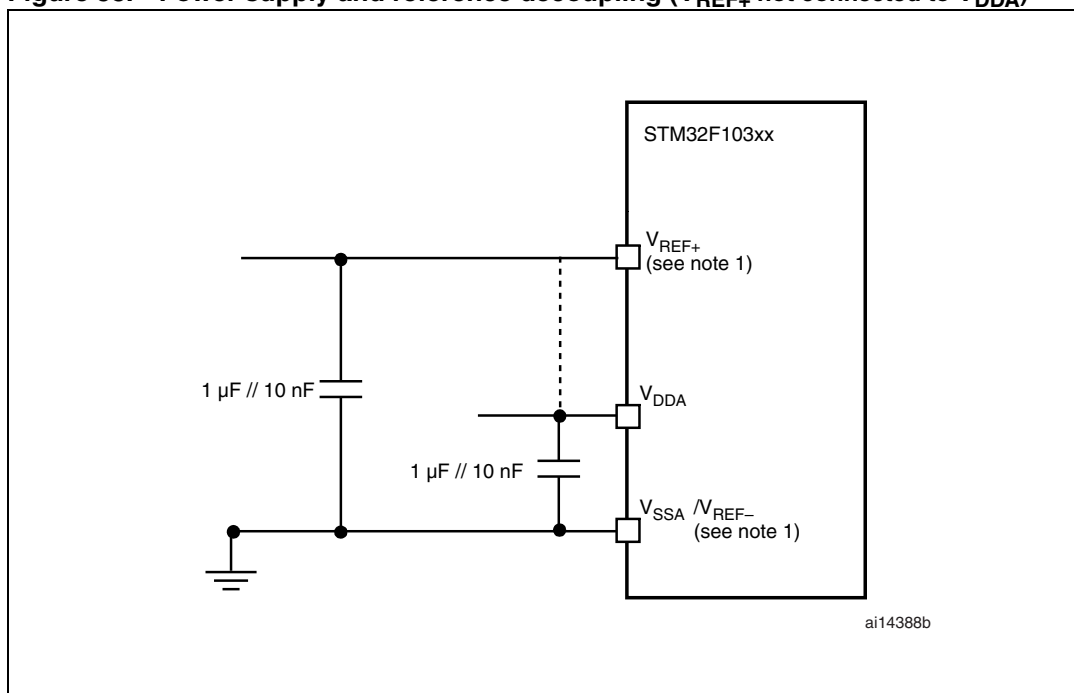


1. Refer to [Table 57](#) for the values of C_{AIN} , R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{PARASITIC}$ must be added to C_{AIN} . It represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

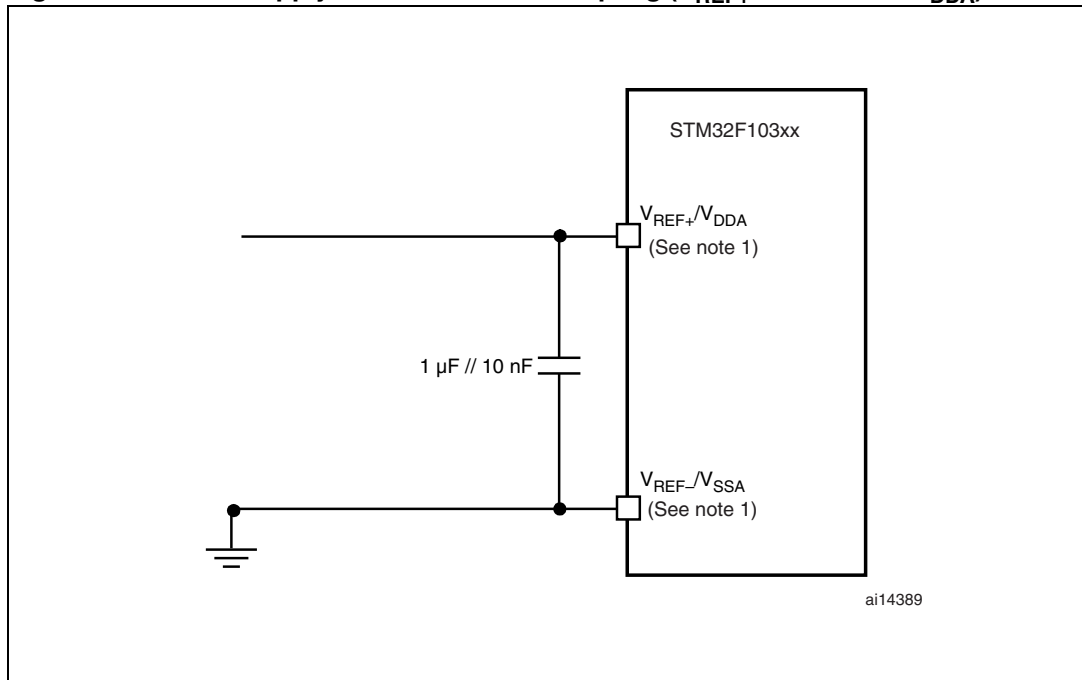
General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 53](#) or [Figure 54](#), depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 53. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Figure 54. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.19 DAC electrical specifications

Table 61. DAC characteristics

Symbol	Parameter	Min	Typ	Max ⁽¹⁾	Unit	Comments
V _{DD33A}	Analog supply voltage	2.4		3.6	V	
V _{DD18D}	Digital supply voltage	1.6	1.8	2	V	
V _{REF+}	Reference supply voltage	2.4		3.6	V	V _{REF+} must always be below V _{DD33A}
V _{SSA}	Ground	0		0	V	
R _L	Resistive load with buffer ON	5			kΩ	Minimum resistive load between DAC_OUT and V _{SSA}
C _L	Capacitive load			50	pF	Maximum capacitive load at DAC_OUT pin.
DAC_OUT min	Lower DAC_OUT voltage with buffer ON	0.2			V	It gives the maximum output excursion of the DAC
DAC_OUT max	Higher DAC_OUT voltage with buffer ON			V _{REF+} - 0.2 V	V	it corresponds to 12-bit input code (0E0)h to (F1C)h @ V _{REF+} = 3.6 V and (155)h and (EAB)h @ V _{REF+} = 2.4 V
I _{DD}	DAC DC current consumption in quiescent mode (Standby mode) (in V _{DD18D} +V _{DD33A} +V _{REF+})		425	600	μA	With no load, middle code (800)H on the inputs
			500	700	μA	With no load, worst code (F1C)H @ V _{REF+} = 3.6 V in terms of DC consumption on the inputs
I _{DDQ}	DAC DC current consumption in Power Down mode (in V _{DD18D} +V _{DD33A} +V _{REF+})		5	350	nA	With no load.
	DAC DC current consumption in Power Down mode (in V _{DD33A} +V _{REF+})		5	200		
DNL	Differential non linearity (Difference between two consecutive code-1LSB)		±0.5		LSB	Given for the DAC in 10-bit configuration (B1=B0=0 always)
INL	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)		±1		LSB	Given for the DAC in 10-bit configuration (B1=B0=0 always)
Offset	Offset error (difference between measured value at Code (800)H and the ideal value = V _{REF+} /2)		±10		mV	Given for the DAC in 10-bit configuration (B1=B0=0 always)
			±3		LSB	Given for the DAC in 10-bit @ V _{REF+} = 3.6 V
Gain error	Gain error		±0.5		%	Given for the DAC in 10-bit configuration (B1=B0=0 always)

Table 61. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max ⁽¹⁾	Unit	Comments
Amplifier gain	Gain of the amplifier in open loop	80	85		dB	with a 5 k Ω load (worst case)
t _{SETTLING}	Settling time (full scale: for an 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ± 1 LSB)		3	4	μ s	C _{LOAD} \leq 50 pF, R _{LOAD} \geq 5 k Ω
Update rate	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)			1	MS/s	C _{LOAD} \leq 50 pF, R _{LOAD} \geq 5 k Ω
t _{WAKEUP}	Wakeup time from off state (PDV18 from 1 to 0)		6.5	10	μ s	C _{LOAD} \leq 50 pF, R _{LOAD} \geq 5 k Ω input code between lowest and highest possible ones.
PSRR+	Power supply rejection ratio (to V _{DD33A}) (static DC measurement)		-67	-40	dB	No R _{LOAD} , C _{LOAD} = 50 pF

1. Guaranteed by characterization, not tested in production.

5.3.20 Temperature sensor characteristics

Table 62. TS characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _L ⁽¹⁾	V _{SENSE} linearity with temperature			± 1	± 2	$^{\circ}$ C
Avg_Slope ⁽¹⁾	Average slope		4.0	4.3	4.6	mV/ $^{\circ}$ C
V ₂₅ ⁽¹⁾	Voltage at 25 $^{\circ}$ C		1.34	1.43	1.52	V
t _{START} ⁽²⁾	Startup time		4		10	μ s
T _{S_temp} ⁽³⁾⁽²⁾	ADC sampling time when reading the temperature			2.2	17.1	μ s

1. Guaranteed by characterization, not tested in production.

2. Data guaranteed by design, not tested in production.

3. Shortest sampling time can be determined in the application by multiple iterations.

6 Package characteristics

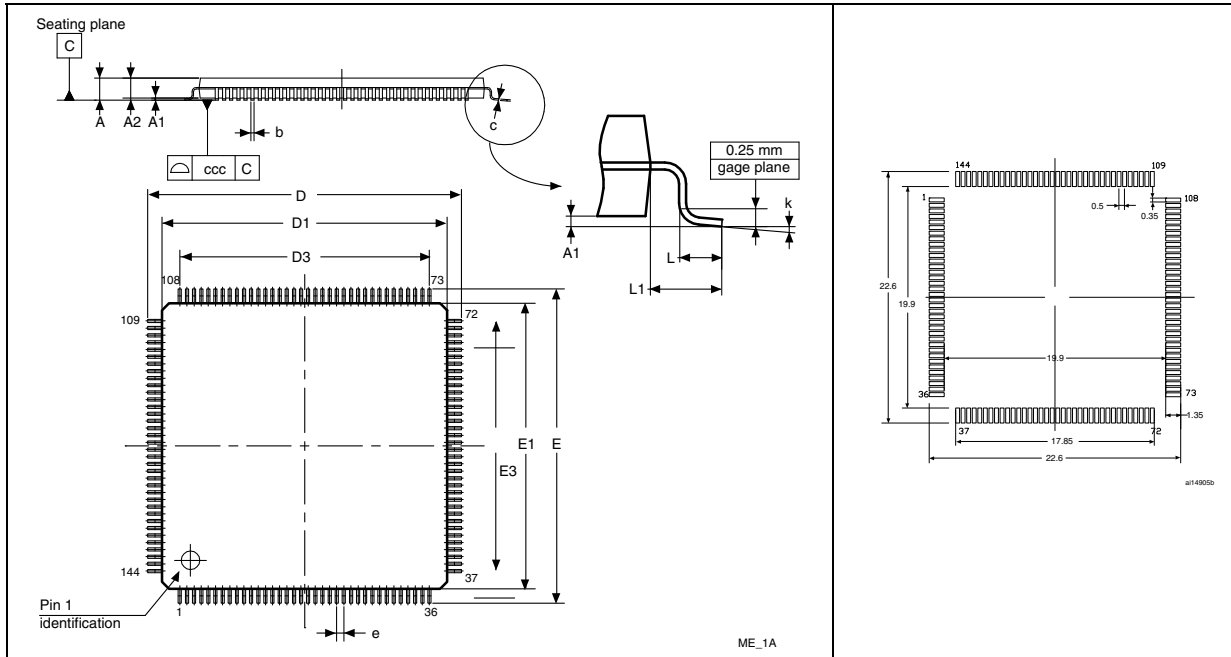
6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 55. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline⁽¹⁾

Figure 56. Recommended footprint⁽¹⁾⁽²⁾



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 63. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Typ	Min	Max	Typ	Min	Max
A			1.60			0.063
A1		0.05	0.15		0.002	0.0059
A2	1.40	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.20		0.0035	0.0079
D	22.00	21.80	22.20	0.8661	0.8583	0.874
D1	20.00	19.80	20.20	0.7874	0.7795	0.7953
D3	17.50			0.689		
E	22.00	21.80	22.20	0.8661	0.8583	0.874
E1	20.00	19.80	20.20	0.7874	0.7795	0.7953
E3	17.50			0.689		
e	0.50			0.0197		
L	0.60	0.45	0.75	0.0236	0.0177	0.0295
L1	1.00			0.0394		
k	3.5°	0°	7°	3.5°	0°	7°
ccc		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 57. LFBGA100 - low profile fine pitch ball grid array package outline

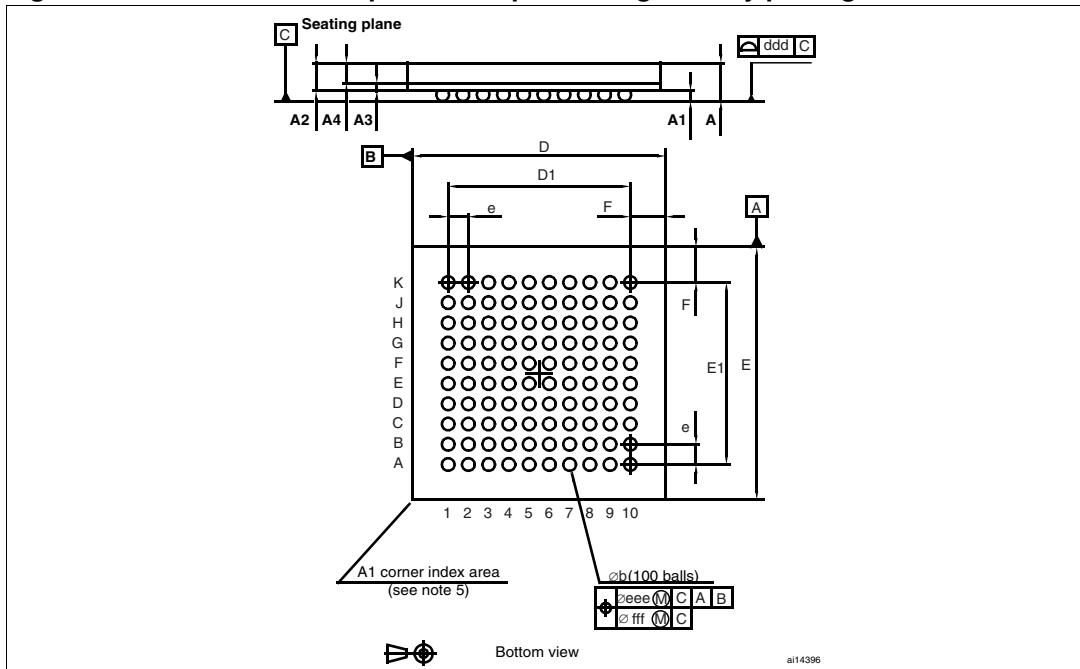


Table 64. LFBGA100 - low profile fine pitch ball grid array package mechanical data

Dim.	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A			1.700			0.0026
A1	0.270			0.0004		
A2		1.085			0.0017	
A3		0.30			0.0005	
A4			0.80			0.0012
b	0.45	0.50	0.55	0.0007	0.0008	0.0009
D	9.85	10.00	10.15	0.0153	0.0155	0.0157
D1		7.20			0.0111	
E	9.85	10.00	10.15	0.0153	0.0155	0.0157
E1		7.20			0.0111	
e		0.80			0.0012	
F		1.40			0.0022	
ddd		0.12			0.0002	
eee		0.15			0.0002	
fff		0.08			0.0001	
N (number of balls)	100					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

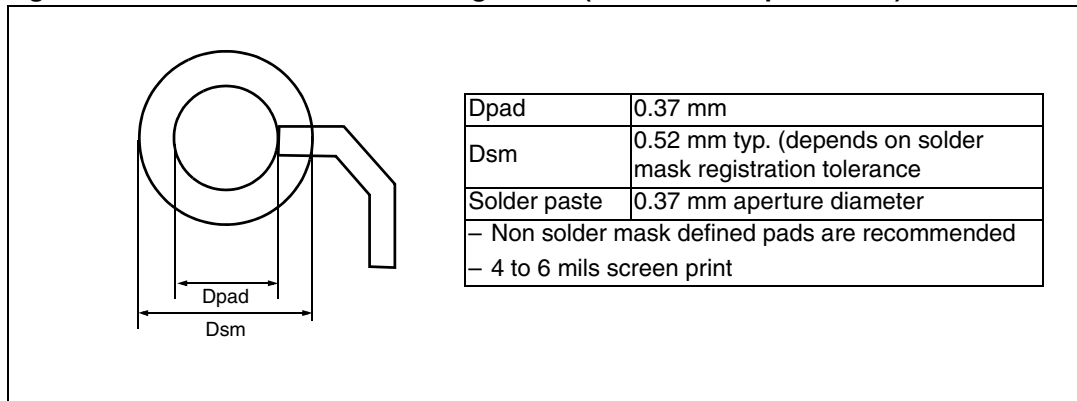
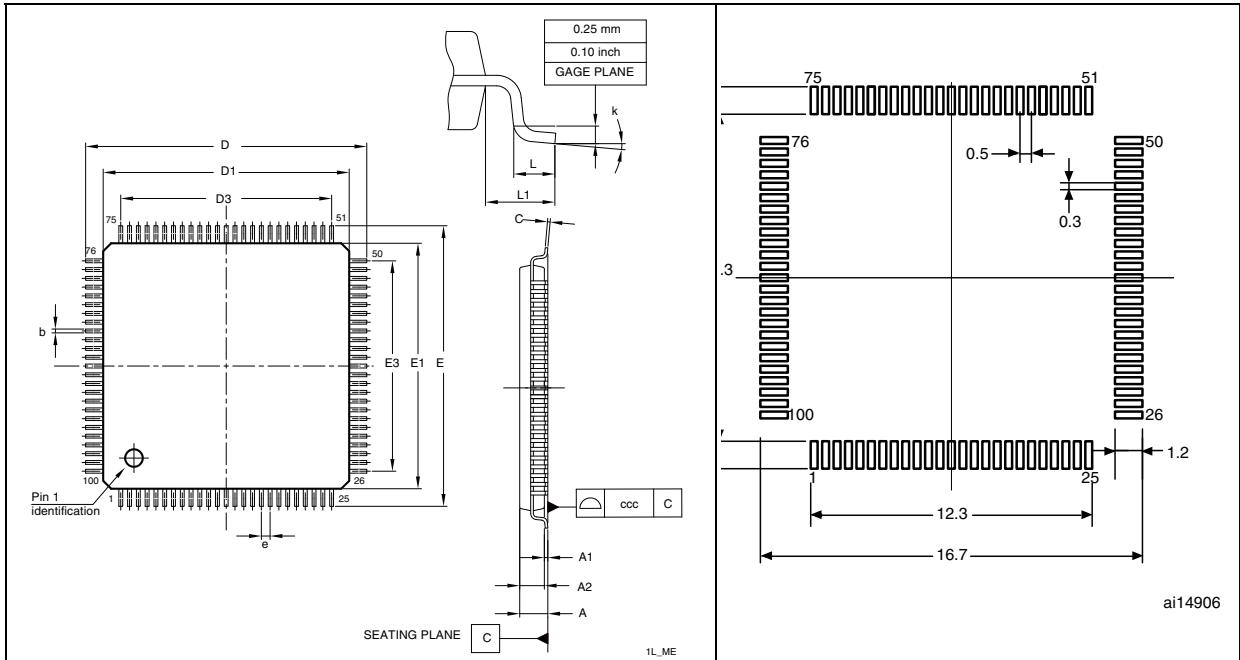
Figure 58. Recommended PCB design rules (0.80/0.75 mm pitch BGA)

Figure 59. LQFP100, 100-pin low-profile quad flat package outline⁽¹⁾

Figure 60. Recommended footprint⁽¹⁾⁽²⁾



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 65. LQFP100 – 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Typ	Min	Max	Typ	Min	Max
A			1.60			0.063
A1		0.05	0.15		0.002	0.0059
A2	1.40	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.20		0.0035	0.0079
D	16.00	15.80	16.20	0.6299	0.622	0.6378
D1	14.00	13.80	14.20	0.5512	0.5433	0.5591
D3	12.00			0.4724		
E	16.00	15.80	16.20	0.6299	0.622	0.6378
E1	14.00	13.80	14.20	0.5512	0.5433	0.5591
E3	12.00			0.4724		
e	0.50			0.0197		
L	0.60	0.45	0.75	0.0236	0.0177	0.0295
L1	1.00			0.0394		
k	3.5°	0°	7°	3.5°	0°	7°
ccc	0.08			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 61. LQFP64 – 64 pin low-profile quad flat package outline⁽¹⁾

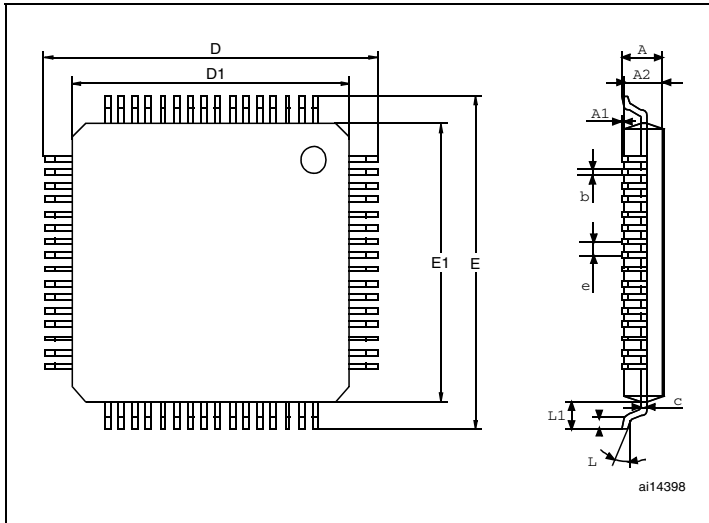
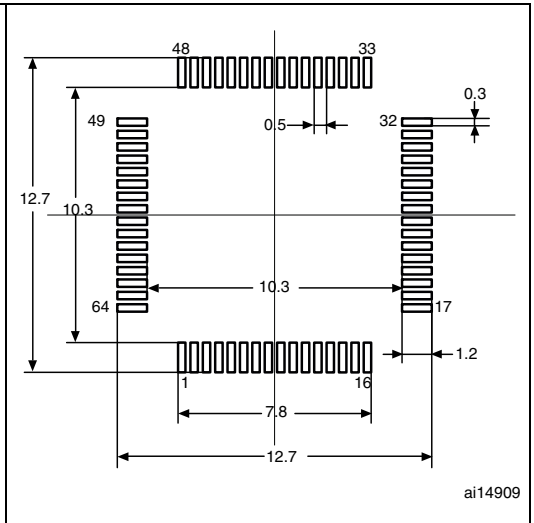


Figure 62. Recommended footprint⁽¹⁾⁽²⁾



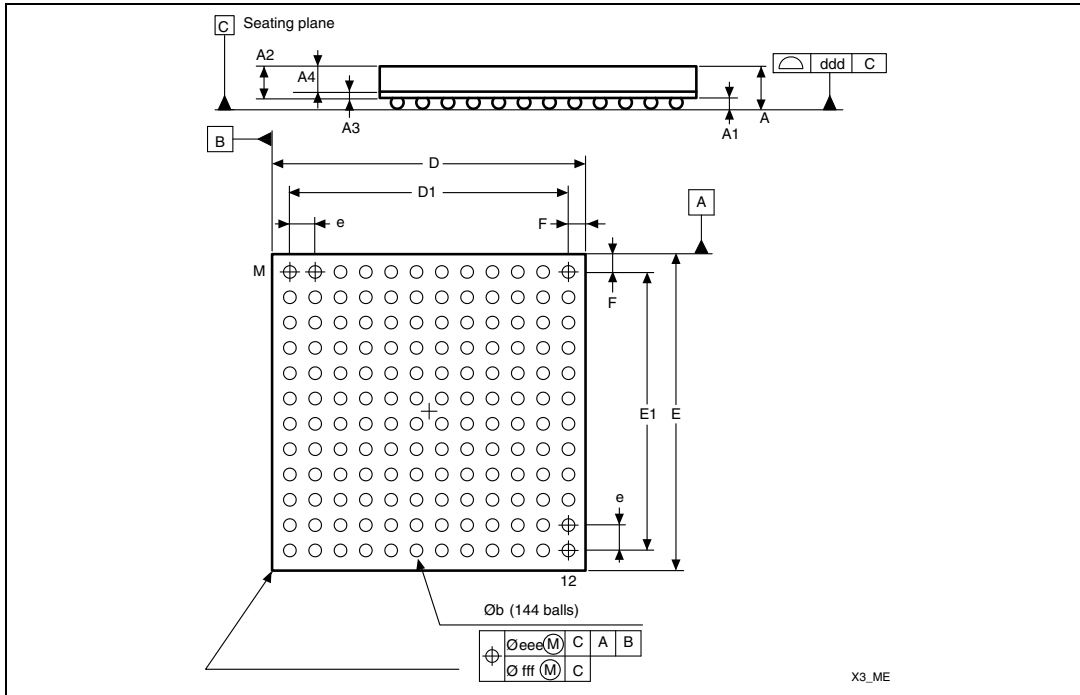
1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 66. LQFP64 – 64 pin low-profile quad flat package mechanical data

Dim.	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of pins					
N	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 63. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline



1. Drawing is not to scale.

Table 67. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package data

Symbol	millimeters			inches ⁽¹⁾		
	Typ	Min	Max	Typ	Min	Max
A			1.70			0.0669
A1	0.21			0.0083		
A2		1.07			0.0421	
A3		0.27			0.0106	
A4			0.85			0.0335
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
D	9.85	10.00	10.15	0.3878	0.3937	0.3996
D1		8.80			0.3465	
E	9.85	10.00	10.15	0.3878	0.3937	0.3996
E1		8.80			0.3465	
e		0.80			0.0315	
F		0.60			0.0236	
ddd		0.10			0.0039	
eee		0.15			0.0059	
fff		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 9: General operating conditions on page 38](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 68. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LFBGA144 - 10 × 10 mm / 0.5 mm pitch	TBD	°C/W
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	TBD	
	Thermal resistance junction-ambient LFBGA100 - 10 × 10 mm / 0.5 mm pitch	41	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	

6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

6.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Table 69: Ordering information scheme](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F103xC at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 82\text{ °C}$ (measured according to JESD51-2),
 $I_{DDmax} = 50\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$ and maximum 8 I/Os used at the same time in output at low level with $I_{OL} = 20\text{ mA}$, $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives: $P_{INTmax} = 175\text{ mW}$ and $P_{IOmax} = 272\text{ mW}$:

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Thus: $P_{Dmax} = 464\text{ mW}$

Using the values obtained in [Table 68](#) T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

$$T_{Jmax} = 82\text{ °C} + (46\text{ °C/W} \times 447\text{ mW}) = 82\text{ °C} + 20.6\text{ °C} = 102.6\text{ °C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105\text{ °C}$).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Table 69: Ordering information scheme](#)).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 115\text{ °C}$ (measured according to JESD51-2),
 $I_{DDmax} = 20\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives: $P_{INTmax} = 70\text{ mW}$ and $P_{IOmax} = 64\text{ mW}$:

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

Thus: $P_{Dmax} = 134\text{ mW}$

Using the values obtained in [Table 68](#) T_{Jmax} is calculated as follows:

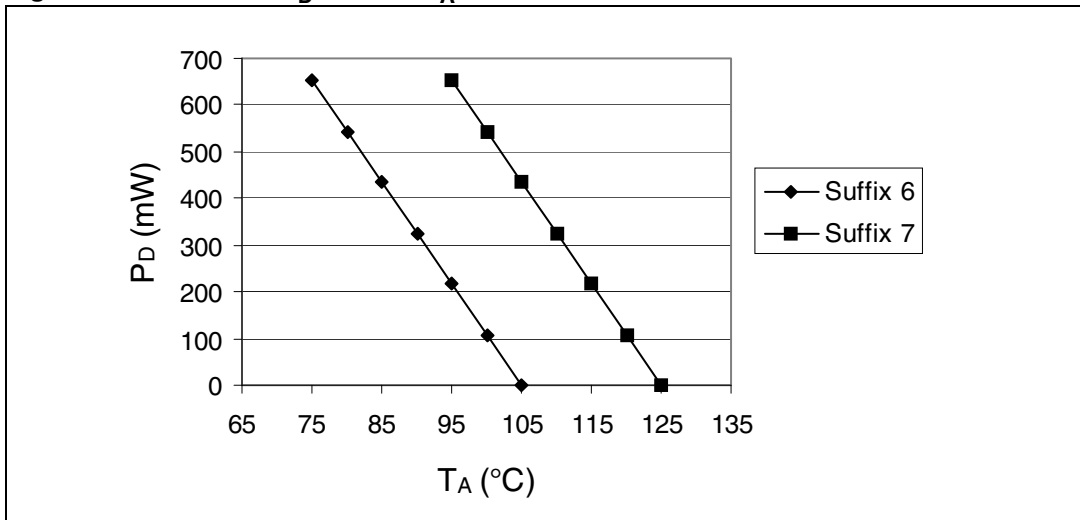
– For LQFP100, 46 °C/W

$$T_{Jmax} = 115\text{ °C} + (46\text{ °C/W} \times 134\text{ mW}) = 115\text{ °C} + 6.2\text{ °C} = 121.2\text{ °C}$$

This is within the range of the suffix 7 version parts ($-40 < T_J < 125\text{ °C}$).

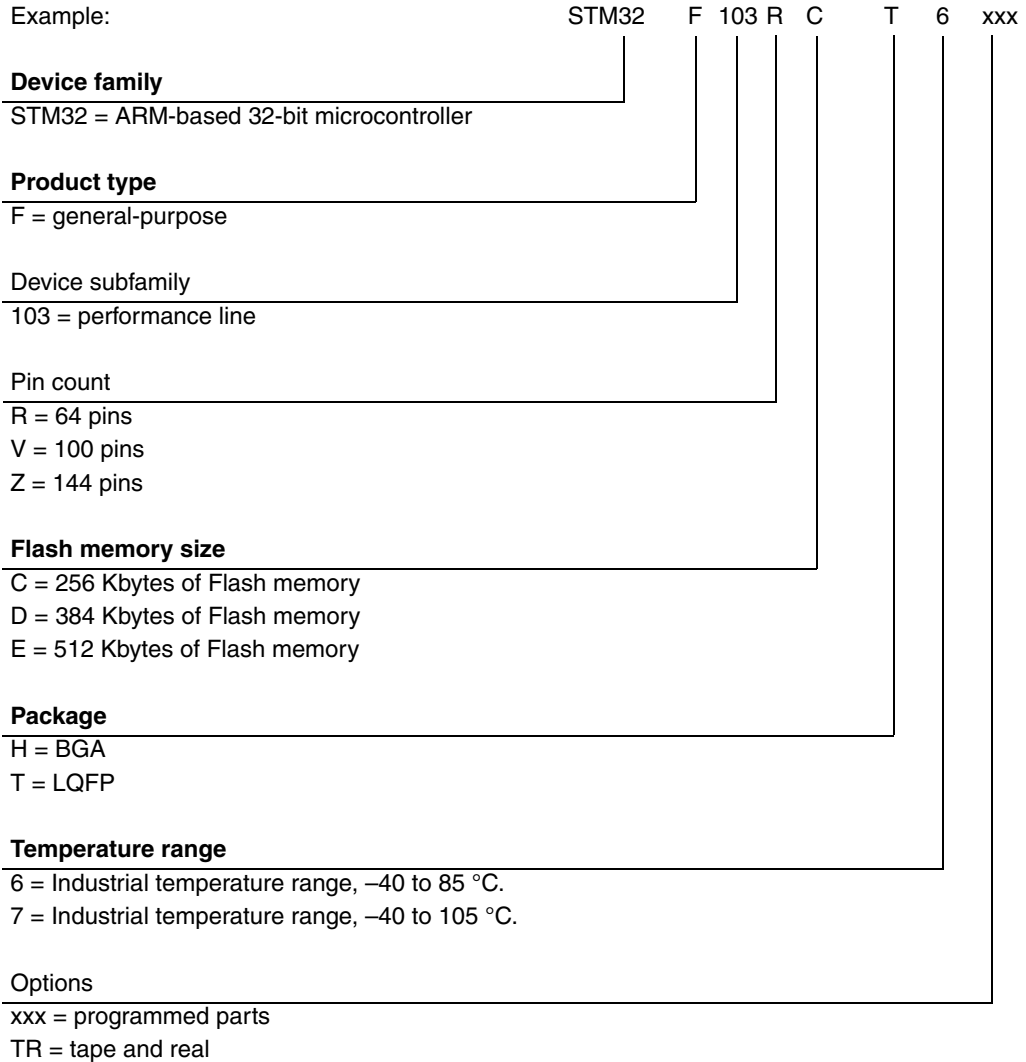
In this case, parts must be ordered at least with the temperature range suffix 7 (see [Table 69: Ordering information scheme](#)).

Figure 64. LQFP100 P_D max vs. T_A



7 Part numbering

Table 69. Ordering information scheme



For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

8 Revision history

Table 70. Document revision history

Date	Revision	Changes
07-Apr-2008	1	Initial release.
22-May-2008	2	<p>Document status promoted from Target Specification to Preliminary Data.</p> <p><i>Section 1: Introduction</i> and <i>Section 2.2: Full compatibility throughout the family</i> modified. Small text changes.</p> <p><i>Note 2</i> added in <i>Table 2: STM32F103xC, STM32F103xD and STM32F103xE features and peripheral counts on page 9</i>.</p> <p>LQPF100/BGA100 column added to <i>Table 5: FSMC pin definition on page 32</i>.</p> <p>Values and Figures added to <i>Maximum current consumption on page 40</i> (see <i>Table 13, Table 14, Table 15</i> and <i>Table 16</i> and see <i>Figure 13, Figure 14, Figure 15, Figure 16</i> and <i>Figure 17</i>).</p> <p>Values added to <i>Typical current consumption on page 46</i> (see <i>Table 17, Table 18</i> and <i>Table 19</i>). <i>Table 19: Typical current consumption in Standby mode</i> removed.</p> <p><i>Note 4</i> and <i>Note 1</i> added to <i>Table 55: USB DC electrical characteristics</i> and <i>Table 56: USB: full-speed electrical characteristics on page 98</i>, respectively.</p> <p>V_{USB} added to <i>Table 55: USB DC electrical characteristics on page 98</i>.</p> <p><i>Figure 56: Recommended footprint(1) on page 107</i> corrected.</p> <p><i>Equation 1</i> corrected. <i>Figure 64: LQFP100 PD max vs. TA on page 115</i> modified.</p> <p>Tolerance values corrected in <i>Table 67: LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package data on page 112</i>.</p>

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