AVERLOGIC

AL4CS211/221/231/241/251

512, 1K, 2K, 4K, 8K x 9 Synchronous FIFOs

Applications

- Multimedia System
- ATM Switches
- Routers
- Cable Modems
- Wireless Base Stations
- SONET(Synchronous Optical Network) Multiplexers
- TBC(Time Base Corrector)
- Hard Disk cache memory

Features

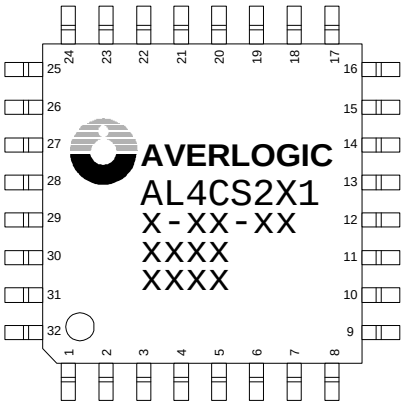
- High performance, low-power, FIFO(First-In First-Out) memory
- 512 x9 bit I/O port (AL4CS211)
- 1K x9 bit 1/O port (AL4CS221)
- 2K x9 bit I/O port (AL4CS231)
- 4K x9 bit I/O port (AL4CS241)
- 8K x9 bit I/O port (AL4CS251)
- High clock speed (133MHz)
- Fully independent read/write access
- Empty, Full, and programmable Almost Empty, Almost Full flags
- Output enable control (data skipping)
- 3.3V power with 5V signal tolerant input
- Standard 32-pin TQFP and PLCC

Description

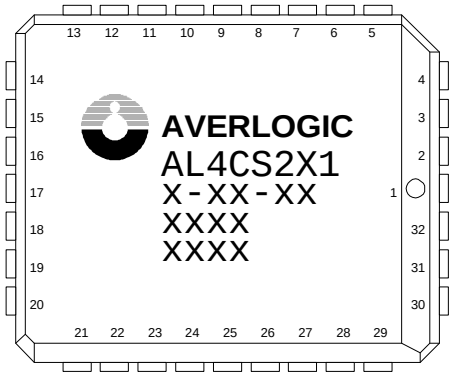
The AL4CS211/AL4CS221/AL4CS231/ AL4CS241/AL4CS251 series memory products are high-performance, low-power 9-bit read/write FIFO (First-In-First-Out) memory chips. They are specially designed to buffer high speed streaming data for a wide range of communication applications, such as optical disk controllers, Local Area Networks (LANs), SONET (Synchronous Optical Network).

Ordering Information

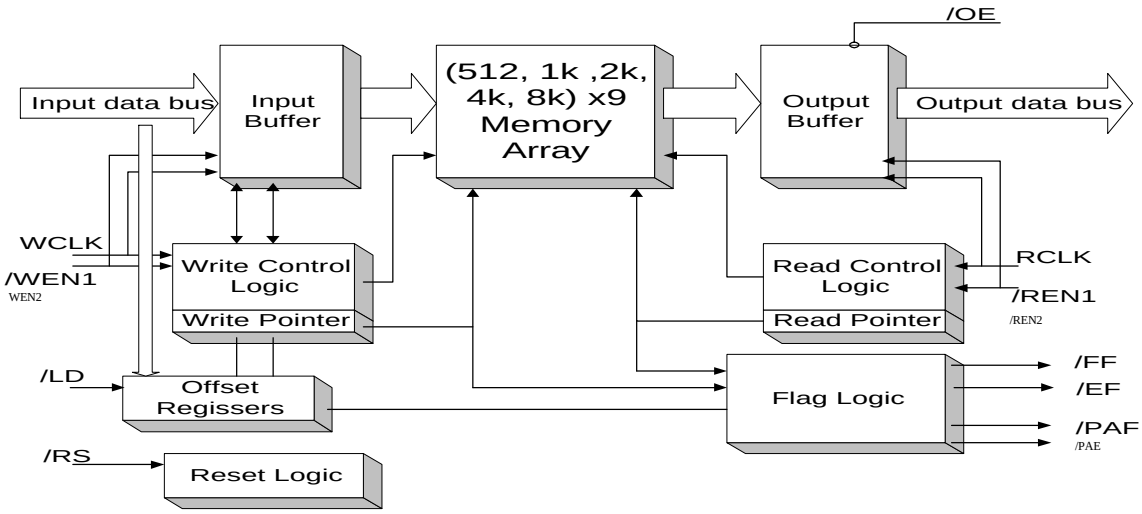
Part number	AL4CS211, AL4CS221, AL4CS231, AL4CS241, AL4CS251
Package	32-pin plastic TQFP and PLCC
Power Supply	+3.3V±10%



TQFP PACKAGE TOP VIEW



PLCC PACKAGE TOP VIEW



AL4CS2x1 FIFO Block Diagram

The 9bit input and output ports operate independently at a maximum speed of 133 MHz. The built-in address decoder and pointer managing circuits provide a straightforward bus interface to serially read/write memory that reduces inter-chip design efforts. The AL4CS2x1 embedded memory array and high performance process technologies with extended controller functions (read skip, fixed and programmable status flags.. etc.) offer flexible memory management.

The input data is synchronous with a free-running clock (WCLK), and input-enable pins (/WEN1, /WEN2). Data is written into the FIFO on every clock when enable pins are asserted. The output is synchronous with the other free-running clock (RCLK) and enables (/REN1, /REN2). An Output Enable pin (/OE) is provided at the read port for tri-state control of the output port. The FIFOs can output two fixed flags, Empty Flag(/EF) and Full Flag (/FF), and two programmable flags, Almost-Empty (/PAE) and Almost-Full (/PAF). The offsets of the /PAE and /PAF flags are loaded when Load pin (/LD) goes low.

These chips are available as a 32-pin TQFP and PLCC Package.