# 512K x 32 Static RAM

## Features

- **High speed**
  - **$t_{AA}$ = 8 ns**
- **Low active power**
  - **1080 mW (max.)**
- **Operating voltages of 3.3 ± 0.3V**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CE_3}$ features**
- **Available in non Pb-free 119-ball PBGA package**

## Functional Description

The CY7C1062AV33 is a high-performance CMOS Static RAM organized as 524,288 words by 32 bits.

Writing to the device is accomplished by enabling the chip ($\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CE_3}$ LOW) and forcing the Write Enable ($\overline{WE}$) input LOW. If Byte Enable A ($\overline{B_A}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$), is written into the location specified on the address pins (A$_0$ through A$_{18}$). If Byte Enable B ($\overline{B_B}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins (A$_0$ through A$_{18}$). Likewise, $\overline{B_C}$ and $\overline{B_D}$ correspond with the I/O pins I/O$_{16}$ to I/O$_{23}$ and I/O$_{24}$ to I/O$_{31}$, respectively.

Reading from the device is accomplished by enabling the chip ($\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CE_3}$ LOW) while forcing the Output Enable ($\overline{OE}$) LOW and Write Enable ($\overline{WE}$) HIGH. If the first Byte Enable ($\overline{B_A}$) is LOW, then data from the memory location specified by the address pins will appear on I/O$_0$ to I/O$_7$. If Byte Enable B ($\overline{B_B}$) is LOW, then data from memory will appear on I/O$_8$ to I/O$_{15}$. Similarly, $\overline{B_c}$ and $\overline{B_D}$ correspond to the third and fourth bytes. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O$_0$ through I/O$_{31}$) are placed in a high-impedance state when the device is deselected ($\overline{CE_1}$, $CE_2$ or $CE_3$ HIGH), the outputs are disabled (OE HIGH), the byte selects are disabled ($\overline{B_{A-D}}$ HIGH), or during a write operation ($\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CE_3}$ LOW, and $\overline{WE}$ LOW).

The CY7C1062AV33 is available in a 119-ball pitch ball grid array (PBGA) package.

## Logic Block Diagram
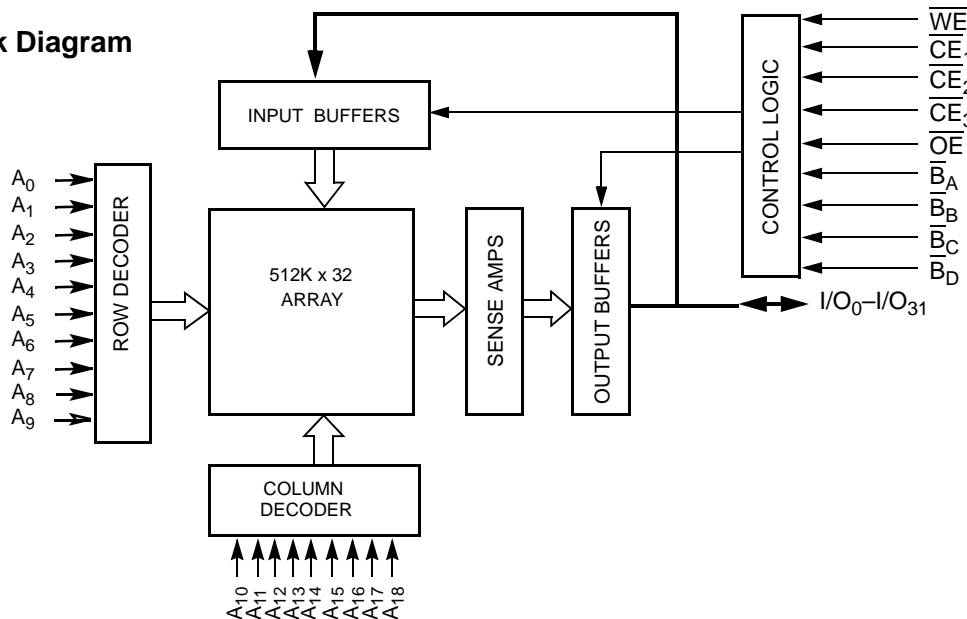


## Selection Guide

| | | −8 | −10 | −12 | Unit |
|---|---|---|---|---|---|
| Maximum Access Time | | 8 | 10 | 12 | ns |
| Maximum Operating Current | Com'l | 300 | 275 | 260 | mA |
| | Ind'l | 300 | 275 | 260 | |
| Maximum CMOS Standby Current | Com'l/Ind'l | 50 | 50 | 50 | mA |

[+] Feedback

**Pin Configurations**[1, 2]

**119-ball PBGA**
**(Top View)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $I/O_{16}$ | A | A | A | A | A | $I/O_0$ |
| **B** | $I/O_{17}$ | A | A | $\overline{CE}_1$ | A | A | $I/O_1$ |
| **C** | $I/O_{18}$ | $\overline{B}_c$ | $\overline{CE}_2$ | NC | $\overline{CE}_3$ | $\overline{B}_a$ | $I/O_2$ |
| **D** | $I/O_{19}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $I/O_3$ |
| **E** | $I/O_{20}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $I/O_4$ |
| **F** | $I/O_{21}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $I/O_5$ |
| **G** | $I/O_{22}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $I/O_6$ |
| **H** | $I/O_{23}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $I/O_7$ |
| **J** | NC | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | DNU |
| **K** | $I/O_{24}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $I/O_8$ |
| **L** | $I/O_{25}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $I/O_9$ |
| **M** | $I/O_{26}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $I/O_{10}$ |
| **N** | $I/O_{27}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $I/O_{11}$ |
| **P** | $I/O_{28}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $I/O_{12}$ |
| **R** | $I/O_{29}$ | A | $\overline{B}_d$ | NC | $\overline{B}_b$ | A | $I/O_{13}$ |
| **T** | $I/O_{30}$ | A | A | $\overline{WE}$ | A | A | $I/O_{14}$ |
| **U** | $I/O_{31}$ | A | A | $\overline{OE}$ | A | A | $I/O_{15}$ |

**Notes:**
1. NC pins are not connected on the die.
2. DNU pins have to be left floating or tied to VSS to ensure proper application.

[+] Feedback

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature  ...................................–65°C to +150°C

Ambient Temperature with
Power Applied.............................................–55°C to +125°C

Supply Voltage on $V_{CC}$ to Relative GND[3] .... –0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State[3] ....................................–0.5V to $V_{CC}$ + 0.5V

DC Input Voltage[3] ................................ –0.5V to $V_{CC}$ + 0.5V

Current into Outputs (LOW)......................................... 20 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ± 0.3V |
| Industrial | –40°C to +85°C | |

## DC Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | −8 Min. | −8 Max. | −10 Min. | −10 Max. | −12 Min. | −12 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = −4.0 mA | | 2.4 | | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | | 0.4 | | 0.4 | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | $V_{CC}$ + 0.3 | 2.0 | $V_{CC}$ + 0.3 | 2.0 | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage[3] | | | −0.3 | 0.8 | −0.3 | 0.8 | −0.3 | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | −1 | +1 | −1 | +1 | −1 | +1 | μA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_{OUT}$ ≤ $V_{CC}$, Output Disabled | | −1 | +1 | −1 | +1 | −1 | +1 | μA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., f = $f_{MAX}$ = 1/$t_{RC}$ | Com'l | | 300 | | 275 | | 260 | mA |
| | | | Ind'l | | 300 | | 275 | | 260 | mA |
| $I_{SB1}$ | Automatic CE Power-down Current —TTL Inputs | Max. $V_{CC}$, $\overline{CE}$ ≥ $V_{IH}$ $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ | | | 70 | | 70 | | 70 | mA |
| $I_{SB2}$ | Automatic CE Power-down Current —CMOS Inputs | Max. $V_{CC}$, $\overline{CE}$ ≥ $V_{CC}$ − 0.3V, $V_{IN}$ ≥ $V_{CC}$ − 0.3V, or $V_{IN}$ ≤ 0.3V, f = 0 | Com'l/ Ind'l | | 50 | | 50 | | 50 | mA |

## Capacitance[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.3V | 8 | pF |
| $C_{OUT}$ | I/O Capacitance | | 10 | pF |

## AC Test Loads and Waveforms[5]



(a)
$Z_0$ = 50Ω
50Ω
30 pF
$V_{TH}$ = 1.5V
Including all Components of Test Equipment

(b)
3.3V
R1 317Ω
OUTPUT
*Including Jig and Scope
*5 pF
R2 351Ω

ALL INPUT PULSES
3.3V
GND
90%
10%
90%
10%
Rise time > 1 V/ns
Fall time: > 1 V/ns

THÉVENIN EQUIVALENT
(c)
OUTPUT
167Ω
1.73V
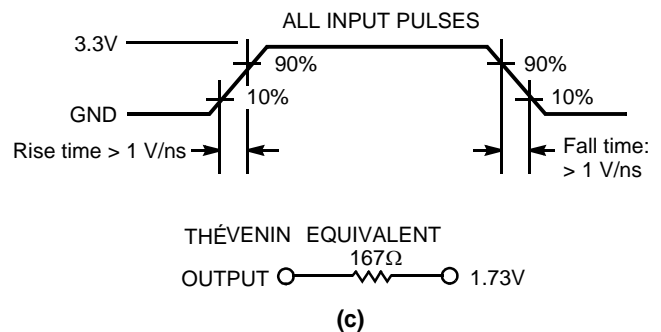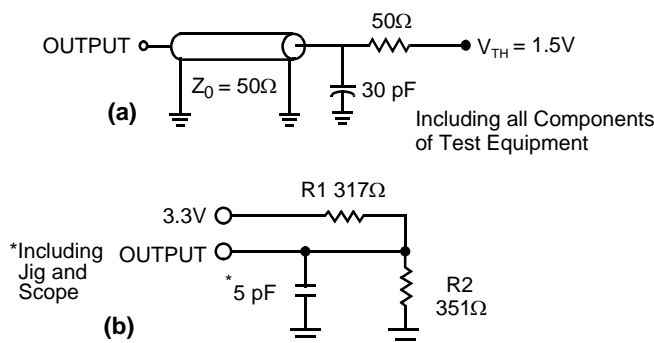
**Notes:**
3. $V_{IL}$ (min.) = −2.0V for pulse durations of less than 20 ns.
4. Tested initially and after any design or process changes that may affect these parameters.
5. Valid SRAM operation does not occur until the power supplies have reached the minimum operating $V_{DD}$ (3.0V). As soon as 1 ms ($T_{power}$) after reaching the minimum operating $V_{DD}$, normal SRAM operation can begin including reduction in $V_{DD}$ to the data retention ($V_{CCDR}$, 2.0V) voltage.

[+] Feedback

## AC Switching Characteristics Over the Operating Range[6]

| Parameter | Description | −8 Min. | −8 Max. | −10 Min. | −10 Max. | −12 Min. | −12 Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | |
| $t_{power}$ | $V_{CC}$ (typical) to the first access[7] | 1 | | 1 | | 1 | | ms |
| $t_{RC}$ | Read Cycle Time | 8 | | 10 | | 12 | | ns |
| $t_{AA}$ | Address to Data Valid | | 8 | | 10 | | 12 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 3 | | 3 | | 3 | | ns |
| $t_{ACE}$ | $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ LOW to Data Valid | | 8 | | 10 | | 12 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 5 | | 5 | | 6 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low-Z[8] | 1 | | 1 | | 1 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High-Z[8] | | 5 | | 5 | | 6 | ns |
| $t_{LZCE}$ | $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ LOW to Low-Z[8] | 3 | | 3 | | 3 | | ns |
| $t_{HZCE}$ | $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH to High-Z[8] | | 5 | | 5 | | 6 | ns |
| $t_{PU}$ | $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ LOW to Power-up[9] | 0 | | 0 | | 0 | | ns |
| $t_{PD}$ | $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH to Power-down[9] | | 8 | | 10 | | 12 | ns |
| $t_{DBE}$ | Byte Enable to Data Valid | | 5 | | 5 | | 6 | ns |
| $t_{LZBE}$ | Byte Enable to Low-Z[8] | 1 | | 1 | | 1 | | ns |
| $t_{HZBE}$ | Byte Disable to High-Z[8] | | 5 | | 5 | | 6 | ns |
| **Write Cycle[10, 11]** | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 8 | | 10 | | 12 | | ns |
| $t_{SCE}$ | $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ LOW to Write End | 6 | | 7 | | 8 | | ns |
| $t_{AW}$ | Address Set-up to Write End | 6 | | 7 | | 8 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | 0 | | ns |
| $t_{SA}$ | Address Set-up to Write Start | 0 | | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 6 | | 7 | | 8 | | ns |
| $t_{SD}$ | Data Set-up to Write End | 5 | | 5.5 | | 6 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low-Z[8] | 3 | | 3 | | 3 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High-Z[8] | | 5 | | 5 | | 6 | ns |
| $t_{BW}$ | Byte Enable to End of Write | 6 | | 7 | | 8 | | ns |

## Data Retention Waveform
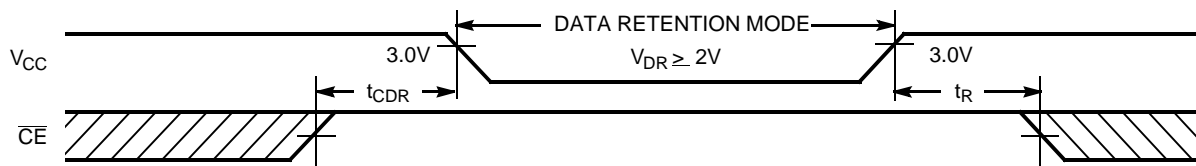


**Notes:**
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{OL}/I_{OH}$ and transmission line loads. Test conditions for the read cycle use output loading as shown in (a) of AC Test Loads, unless specified otherwise.
7. This part has a voltage regulator that steps down the voltage from 3V to 2V internally. $t_{power}$ time has to be provided initially before a read/write operation is started.
8. $t_{HZOE}$, $t_{HZCE}$, $t_{HZWE}$, $t_{HZBE}$, and $t_{LZOE}$, $t_{LZCE}$, $t_{LZWE}$, and $t_{LZBE}$ are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
9. These parameters are guaranteed by design and are not tested.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ HIGH, $\overline{CE}_3$ LOW, and $\overline{WE}$ LOW. The chip enables must be active and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of $t_{HZWE}$ and $t_{SD}$.

[+] Feedback

## Switching Waveforms

**Read Cycle No. 1**[12, 13]
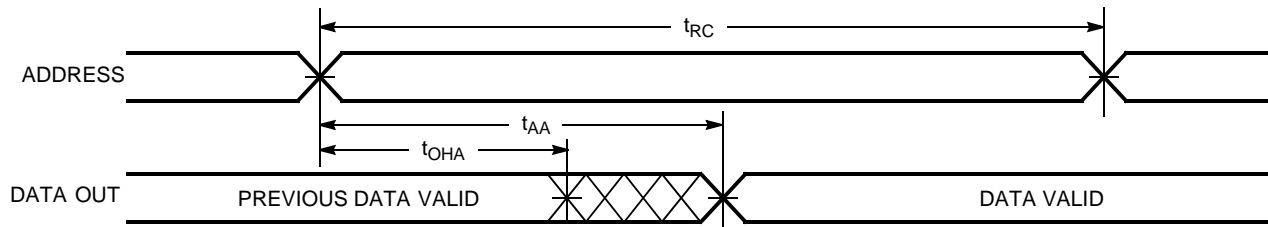
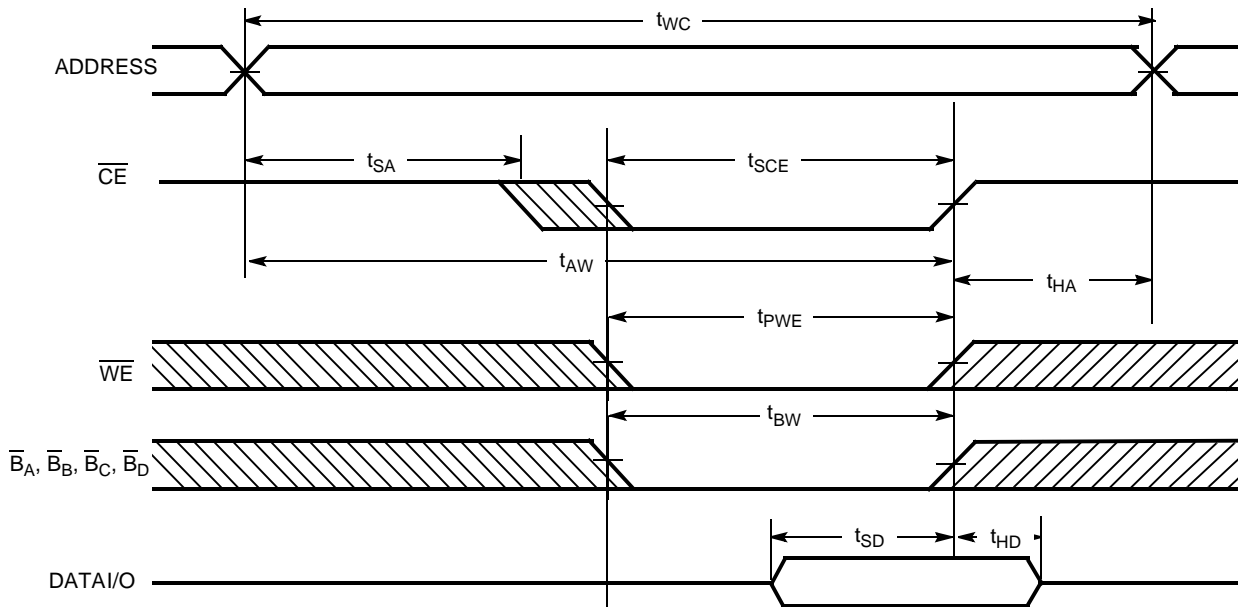

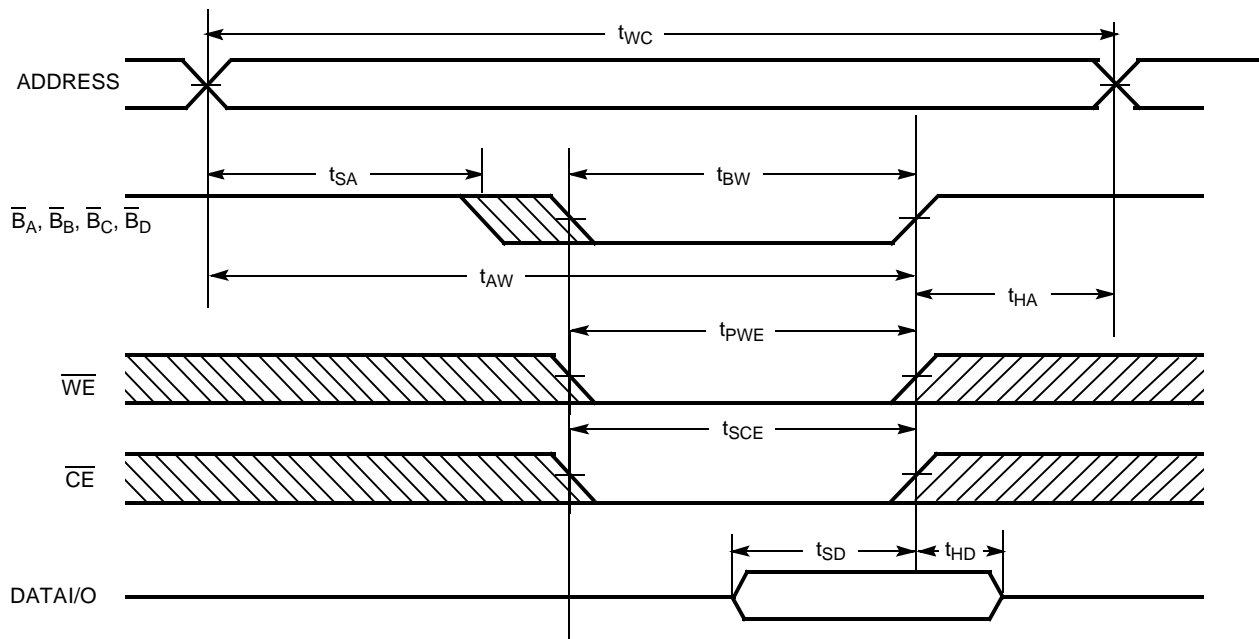**Read Cycle No. 2 ($\overline{OE}$ Controlled)**[13, 14]
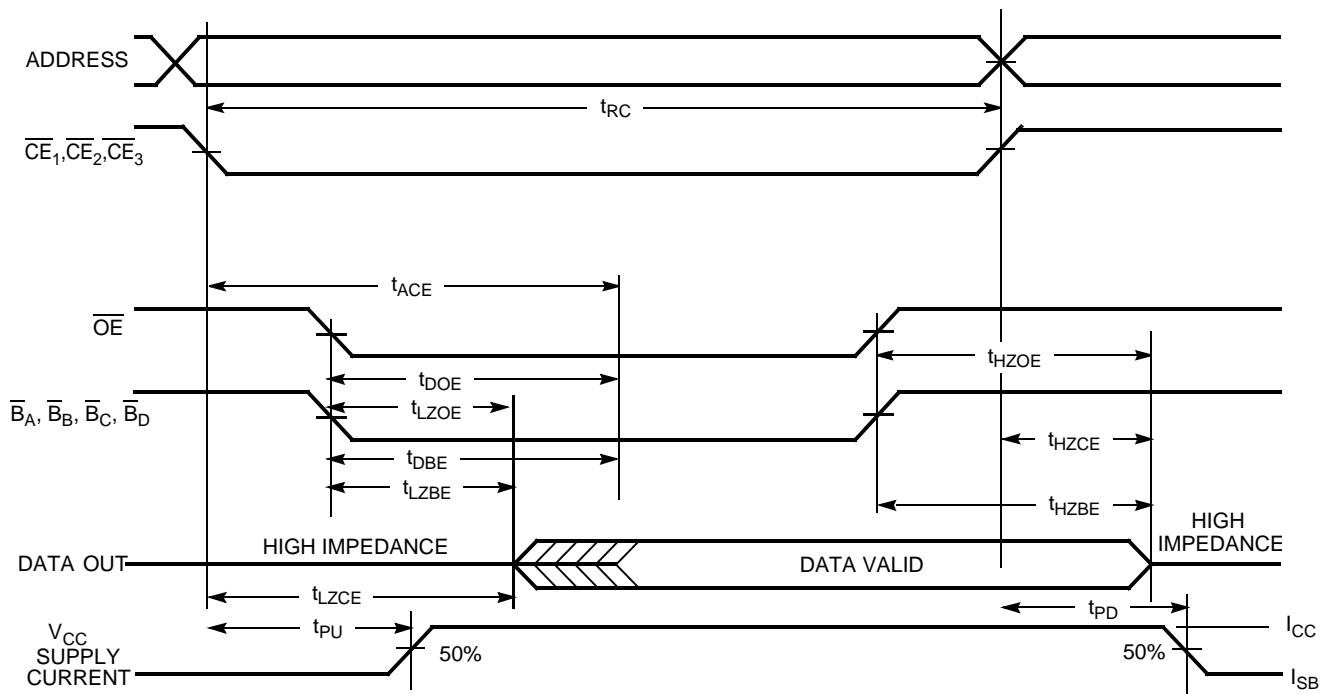


**Notes:**
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ = $V_{IL}$.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

## Switching Waveforms (continued)

### Write Cycle No. 1 ($\overline{CE}$ Controlled)[15, 16, 17]



### Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)[15, 16, 17]



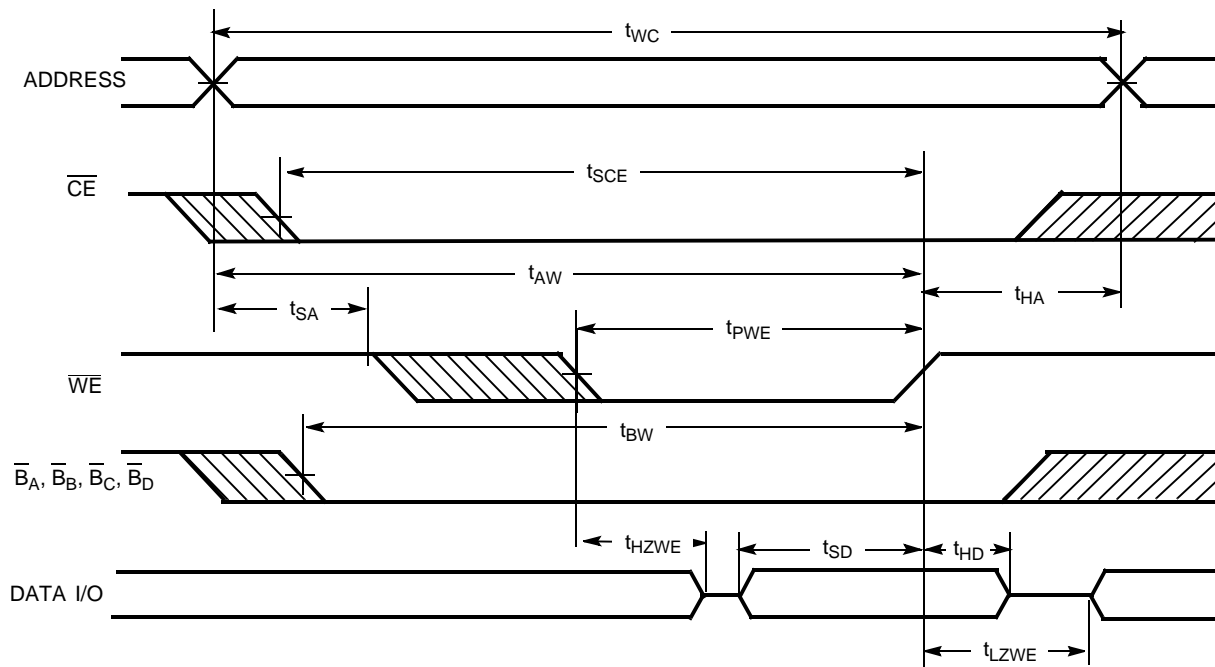**Notes:**
15. $\overline{CE}$ indicates a combination of all three chip enables. When ACTIVE LOW, $\overline{CE}$ indicates the $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ are LOW.
16. Data I/O is high-impedance if $\overline{OE}$ or $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D = V_{IH}$.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

[+] Feedback

## Switching Waveforms (continued)

**Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)**



## Truth Table

| $\overline{CE_1}$ | $\overline{CE_2}$ | $\overline{CE_3}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{B_A}$ | $\overline{B_B}$ | $\overline{B_c}$ | $\overline{B_D}$ | I/O$_0$– I/O$_7$ | I/O$_8$– I/O$_{15}$ | I/O$_{16}$– I/O$_{23}$ | I/O$_{24}$– I/O$_{31}$ | Mode | Power |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | X | X | X | X | High-Z | High-Z | High-Z | High-Z | Power Down | ($I_{SB}$) |
| X | H | X | X | X | X | X | X | X | High-Z | High-Z | High-Z | High-Z | Power Down | ($I_{SB}$) |
| X | X | H | X | X | X | X | X | X | High-Z | High-Z | High-Z | High-Z | Power Down | ($I_{SB}$) |
| L | L | L | L | H | L | L | L | L | Data Out | Data Out | Data Out | Data Out | Read All Bits | ($I_{CC}$) |
| L | L | L | L | H | L | H | H | H | Data Out | High-Z | High-Z | High-Z | Read Byte A Bits Only | ($I_{CC}$) |
| L | L | L | L | H | H | L | H | H | High-Z | Data Out | High-Z | High-Z | Read Byte B Bits Only | ($I_{CC}$) |
| L | L | L | L | H | H | H | L | H | High-Z | High-Z | Data Out | High-Z | Read Byte C Bits Only | ($I_{CC}$) |
| L | L | L | L | H | H | H | H | L | High-Z | High-Z | High-Z | Data Out | Read Byte D Bits Only | ($I_{CC}$) |
| L | L | L | X | L | L | L | L | L | Data In | Data In | Data In | Data In | Write All Bits | ($I_{CC}$) |
| L | L | L | X | L | L | H | H | H | Data In | High-Z | High-Z | High-Z | Write Byte A Bits Only | ($I_{CC}$) |
| L | L | L | X | L | H | L | H | H | High-Z | Data In | High-Z | High-Z | Write Byte B Bits Only | ($I_{CC}$) |
| L | L | L | X | L | H | H | L | H | High-Z | High-Z | Data In | High-Z | Write Byte C Bits Only | ($I_{CC}$) |
| L | L | L | X | L | H | H | H | L | High-Z | High-Z | High-Z | Data In | Write Byte D Bits Only | ($I_{CC}$) |
| L | L | L | H | H | X | X | X | X | High-Z | High-Z | High-Z | High-Z | Selected, Outputs Disabled | ($I_{CC}$) |

[+] Feedback

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 8 | CY7C1062AV33-8BGC | 51-85115 | 119-ball (14 x 22 x 2.4 mm) PBGA | Commercial |
| 10 | CY7C1062AV33-10BGC | | | |
| | CY7C1062AV33-10BGI | | | Industrial |
| 12 | CY7C1062AV33-12BGC | | | Commercial |
| | CY7C1062AV33-12BGI | | | Industrial |

## Package Diagram

119-ball PBGA (14 x 22 x 2.4 mm) (51-85115)
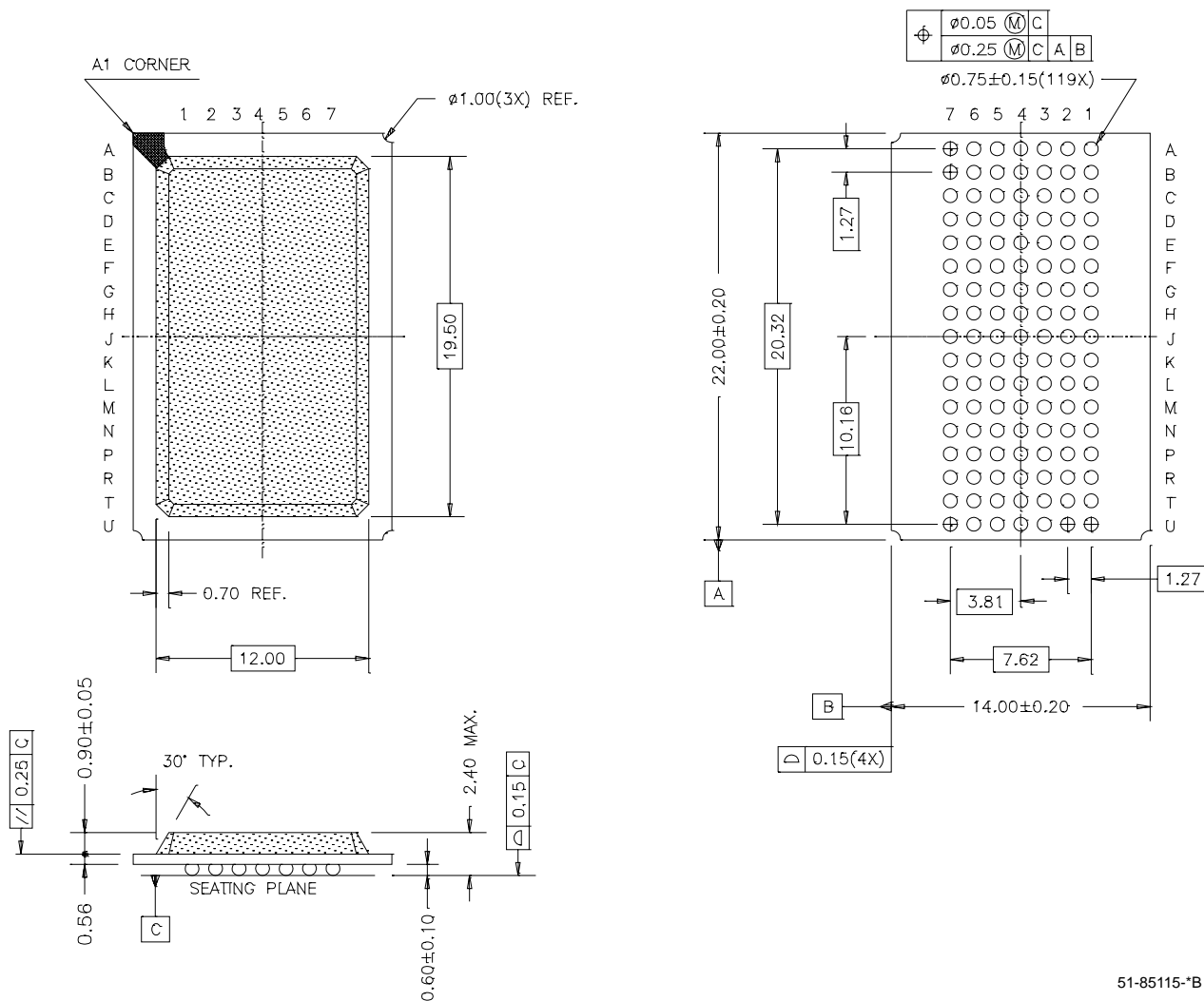


51-85115-*B

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[+] Feedback

## Document History Page

| | | | | |
|---|---|---|---|---|
| **Document Title: CY7C1062AV33 512K x 32 Static RAM** | | | | |
| **Document Number: 38-05137** | | | | |

| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
|---|---|---|---|---|
| ** | 109752 | 02/27/02 | HGK | New Data Sheet |
| *A | 117059 | 09/19/02 | DFP | Removed 15-ns bin and added 8-ns bin.<br>Changed $CE_2$ TO $\overline{CE_2}$.<br>Changed $C_{IN}$ – input capacitance – from 6 pF to 8 pF.<br>Changed $C_{OUT}$ – output capacitance – from 8 pF to 10 pF. |
| *B | 119389 | 10/07/02 | DFP | Updated $I_{CC}$, $T_{sd}$, and $T_{doe}$ parameters.<br>Removed note 7 ($I_Z/h_Z$ comment). |
| *C | 120384 | 11/13/02 | DFP | Final Data Sheet.<br>Removed note 2.<br>Added note 3 to "AC Test Loads and Waveforms" and note 7 to $t_{pu}$ and $t_{pd}$. |
| *D | 124440 | 2/25/03 | MEG | Changed ISB1 from 100 mA to 70 mA |
| *E | 329638 | See ECN | RKF | Removed $\overline{CE_2}$ waveform showing Active High signal timing on Page #5, and included it with the $CE_1$, $CE_3$ waveform<br>Corrected Truth Table on page 7 with $\overline{CE_2}$ active low information |
| *F | 492137 | See ECN | NXR | Included note #1 and 2 on page #2<br>Changed the description of $I_{IX}$ from Input Load Current to Input Leakage Current in DC Electrical Characteristics table<br>Updated Ordering Information Table |

[+] Feedback