Ordering number : ENN8096A

SANYO Semiconductors

DATA SHEET

SDPiC™

Silicon Gate CMOS IC

LC749450NW — Digital RGB Image Processor IC

Overview

The LC749450NW RGB image processing IC converts interlaced video signals such as NTSC and PAL to progressive scan and adjusts the image quality of that signal. Since the LC749450NW can operate at input clock frequencies up to 27 MHz, it is optimal as a pixel display device IC for high-quality high-resolution images. A high image quality progressive scan signal playback system can be implemented easily by combining the LC749450NW with external memory (two 16M SDRAMs).

Features

- Accepts 30-bit (4:4:4) YCbCr signals, 20-bit (4:2:2) YCbCr signals, and 10-bit RT.656 signals as inputs.
- Supports digital TV inputs (480i, 480p, 1080i, and 720p): 30-bit YCbCr digital signal input.
- 30-bit digital RGB signal inputs
- Produces 30-bit and 24-bit digital RGB (or YCbCr) signal outputs
- Provides both YCbCr/YPbPr → RGB conversion and RGB → YCbCr conversion
- Motion adaptive jaggy-less interlaced to progressive conversion
- 3:2 pull down
- Multiple noise reduction systems (1D, 2D, and 3D)
- Cross color and cross luminance cancellers
- Horizontal outline correction (LTI and CTI)
- Sharpness (horizontal and vertical)
- Sharpness adjuster (shading relief enhancement)
- White and black level expansion, white text correction (blue stretch)
- Flesh tone correction
- Hue and color gain adjustments
- Color exciter (6-phase RGBYMC independent saturation adjustment)
- Brightness and contrast adjustment
- White balance and black balance adjustment
- Gamma correction (Independent RGB, programmable LUT system)
- Dithering (10-bit and 8-bit)
- Clamp control
- Aspect ratio conversion (4:3 → 16:9)
- Clock generator (PLL) circuit
- SDRAM interface
- I²C bus and CPU interface circuits

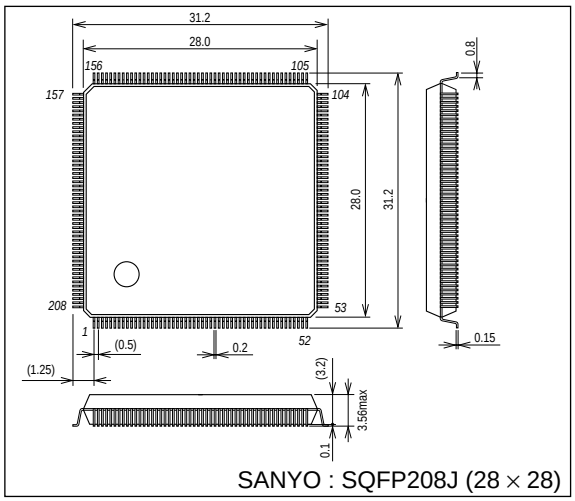
SDPIC™: SANYO Digital Picture Improvement Core
SDPIC™ is a registered trademark of SANYO Electric Co., Ltd.

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Package Dimensions

unit : mm

3261



IC Specifications

- Supply voltage: Core block: 1.8 V, I/O blocks: 3.3 V
- Maximum operating frequency: 27 MHz (IP conversion mode), 135 MHz (IP conversion not used)
- Package: 208-pin SQFP

Main Applications

- LCD TVs, monitors, and projectors
- PDP TVs and progressive scan TVs
- DVD players and recorders

Functional Overview

1. Input signal formats
   The digital data port supports the following input signal formats.
   30-bit RGB
   30-bit (4:4:4) YCbCr/YPbPr
   20-bit (4:2:2) YCbCr/YPbPr
   10-bit signals conforming to the ITU-R BT.656 standard (horizontal and vertical sync inputs required)

   NTSC (480i/480p), PAL (576i/576p), and HD (1080i/720p)
   RGB (up to 135 MHz)

2. IP conversion block
   For NTSC (480i) and PAL (576i) inputs the LC749450NW provides motion adaptive IP conversion or cinema IP conversion (3:2 pull down) with both 2D/3D noise reduction and cross color/cross luminance cancellation. External SDRAM (either 2 × 16 Mbits or 1 × 64 Mbits) is required when the functions of this block are enabled. This block is set to bypass mode for 480p, 576p, 1080i, 720p, and PC (RGB) inputs.

(1) Motion adaptive IP conversion
   The LC749450NW performs motion detection for each pixel that enters the IP conversion block. Based on that result, the block performs interlaced to progressive conversion. Pixels that are found to be static are interpolated between fields and pixels that are found to be moving are interpolated within the field.
   Since this circuit takes correlations in the diagonal directions into account when performing inter-field interpolation for moving sections of the image, it can create smooth video with minimal stair-stepping artifacts (jaggies). Furthermore, this function can handle images that range from relaxed smooth video to video with violent motion by setting parameters and changing the motion threshold values for each pixel.

Continued on next page.

Continued from preceding page.

(2) Cinema mode IP conversion (3:2 pull down)

When an NTSC interlaced signal that was generated by a film (cinema) source is input, it automatically recognizes the signal as a cinema source and performs cinema mode IP conversion that is optimal for cinema sources.
The threshold value for that recognition can be set with a parameter.

(3) Noise reduction (2D, 3D)

The LC749450NW provides three noise reduction functions: 3D noise reduction, which reduces noise between fields, 2D noise reduction, which reduces noise within the field, and 1D noise reduction, which reduces noise in the scan line direction. This block contains the 3D and 2D noise reduction functions and can operate independently for both the luminance signal and the chrominance signal.

(4) Cross color and cross luminance canceller

This circuit can reduce the cross color noise (rainbow-like color smearing) and cross luminance (dot) noise that is generated when a decoder (such as a 3-line decoder) other than 3D YC separator decoder is used for NTSC input. This function makes it possible to produce clear and vivid video with no color blotting and no dot interference.

3. Image quality adjustment block

The LC749450NW provides a full complement of image quality adjustment functions and can perform the image quality adjustments required for optimal flat panel TV display.

(1) Horizontal outline correction (LTI/CTI)

The LTI/CTI block applies outline correction to the input signal. The apparent sharpness in the video image is enhanced by increasing the slope of the input signal. Since this function does not add overshoot or undershoot to edges in the video signal, it creates natural-looking images. This function operates independently on the luminance and chrominance signals.

(2) Sharpness (horizontal and vertical)

The sharpness function can correct the outlines in the input signal. This function differs from the LTI/CTI function described above in that it adds an appropriate peak in the corrected outline area. The amount of this peak and a coring level that prevents fine noise from being aggravated can be set in the control registers for this circuit. This function only operates on the luminance signal.

(3) Shadow adjuster

The shadow adjuster function detects the outlines in the input signal and adds an appropriate peak before and after the outline to add an appearance of a shadow. This creates a video signal that is varied and not dull.

(4) White and black expansion

The white and black expansion function adaptively expands the white and black levels in the Y component of the YCbCr signal using the white and black peak levels in the immediately preceding field, the luminance signal average picture level (APL), distributional information, and microcontroller settings. The white and black peaks are the maximum and minimum values in the input data within a single field. When the white and black expansion function is used, the values of the settings must be set appropriately.

(5) White text correction (blue stretch)

The blue stretch function creates visually pleasing white text by adding a small amount of blue to white characters. A gain adjustment is applied to section of the Y signal recognized as white text and added to the Cb signal.

(6) Flesh tone correction

The flesh tone correction function extracts just the set skin color without affecting other colors and allows just that color to be adjusted.

(7) Hues and color gain adjustment

The hue adjustment adjusts the hue of the whole image. The color gain adjustment adjusts the depth of the color by controlling the gain applied to the color difference signals. This function can adjust the Cb and Cr signals independently.

(8) Color exciter

The color exciter can independently control the red, green, blue, magenta, yellow, and cyan colors.

(9) Brightness and contrast controls

The brightness control adjusts the brightness of the screen as a whole and the contrast control adjusts the gain applied to the brightness.

(10) White balance and black balance adjustments

These adjust the appearance of white and black on the LCD panel.

(11) Gamma correction

This function allows the creation of arbitrary gamma curves to match the characteristics of the LCD panel used. The RGB channels can be adjusted independently, using internal programmable LUT.

(12) Dithering

The LC749450NW performs internal signal processing with a 10-bit precision. When these signals are output as 8-bit values, the lower two bits are rounded by dithering.

4. Outputs and Other Functions

(1) Matrix conversion

The LC749450NW provides the following matrix conversion functions.

YCbCr → RGB
YPbPr → RGB
YPbPr → YCbCr
RGB → YCbCr

(2) Aspect ratio conversion

An input Rec.601 signal (example: 720 × 240) can be expanded in the horizontal direction and displayed on a WVGA panel.

(3) Output formats

The LC749450NW can output video in the following formats.
Digital RGB (30 or 24 bits)
Digital YCbCr (30 or 24 bits)

(4) Clamp control

The LC749450NW can generate the clamp signals required for the front-end A/D converter. It can also generate arbitrary pulses (high, low, or high impedance) by comparing with an IC internal threshold value (that can be set with a register setting).

(5) SDRAM interface

The LC749450NW includes an SDRAM interface that can directly connect either:

Two 16 Mbit SDRAMs (512 words × 16 bits × 2 banks)

or

One 64 Mbit SDRAM (512 words × 32 bits × 4 banks).

This allows end product systems to be constructed easily.
SDRAMs with a speed grade of 70 or better must be used.

(6) I^2C bus interface and CPU interface

The LC749450NW is basically designed to be controlled by setting internal registers over the I^2C bus.
The slave address can be switched to match the system by controlling pin 85 (SLADR).
The following slave addresses are supported.

SLADR = low: E0h
SLADR = high: E2h

Certain registers can also be controlled over the CPU interface.

I/O Specifications

Input Signals

Signal type	Number of pins	Symbol	Description	Notes
Video signals	10	YIN	Y or G	NTSC/PAL/DTV (4801, 480P, 1080I)
	10	CBI	Cb or B or C	or progressive scan RGB (up to SXGA)
	10	CRI	Cr or R or OSD	or NTSC/PAL decoder input
Sync signals	1	DHS	Horizontal sync signal	Pixel sync horizontal sync signal input The polarity can be switched by setting the DVPOLIN internal register.
	1	DVS	Vertical sync signal	Vertical sync signal input The polarity can be switched by setting the DVPOLIN internal register.
Data enable signals	1	DEHI	Data enable	Valid video period enable signal (horizontal/composite)
	1	DEVI	Vertical data enable	Valid video period enable signal (vertical)
	1	FIELD	Field signal input	Field signal input
Pixel clock	1	CLKI	Clock	System clock input
Fixed oscillator	1	DCLKI	Used for the output dot clock	System clock input
	1	XTAL		Fixed clock input or test clock input
System reset	1	XRST	System reset	System reset input, active low
Total	40	—	—	—

Output Signals

Signal type	Number of pins	Symbol	Description	Notes
Video signals	10	ODG	G	RGB output
	10	ODB	B	The LC749450NW also supports dithered 8-bit output.
	10	ODR	R	
Sync signals	1	DHO	Horizontal sync signal	This pin outputs the DHS pin input after a delay. (Used for pixel sync.) (This can be set over the I²C bus.)
	1	DVO	Vertical sync signal	Outputs a vertical pixel sync signal.
Data enable signals	1	AREA	Data enable	Outputs a valid area signal.
Pixel clocks	1	CLKOUT	Outputs the input clock	The polarity can be inverted.
Clamp pulse signals	1	CLAMPO	For A/D conversion	Outputs a pulse signal used for A/D conversion clamp period verification
Clamp levels	1	CLPG	Y/G clamp level	Clamp level discrimination output
	1	CLPB	Cb/B clamp level	(Too large: low, too small: high, match: high-impedance)
	1	CLPR	Cr/R clamp level	
Field discrimination signals	1	ODEVPPO	Field discrimination	Outputs an odd/even field discrimination signal (Used when IP conversion is not used.)
Total	39	—	—	—

Control Signals

Signal type	Number of pins	Symbol	Description	Notes
I²C bus signals	1	SDAIO	Data bus	Used for setting internal registers and reading out the internal status.
	1	SCLI	Bus clock	The slave address is “1110000+(R/W)”.
	1	SLADR	Slave switching	Sets the I²C bus slave address. Normally low, High: E2h, Low: E0h.
Data output signals	1	OE		Data output enable signal
XTAL	1	XTALSW		This signal sets the XTAL clock pin input operation High: The XTAL clock input signal is divided by 2.
Total	5	—	—	—

SDRAM Control Signals

Signal type	Number of pins	Symbol	Description	Notes
Clock signals	1	SDCLKI		SDRAM clock input
	1	SDCLKO		SDRAM clock output
Control system signals	1	SDRAS		SDRAM row address strobe signal output
	1	SDCAS		SDRAM column address strobe signal output
	1	SDWE		SDRAM write enable signal output
Address system signals	11	SAD		SDRAM address signal output
	1	SDBS		SDRAM bank select signal output
Data system signals	1	SDDQM		SDRAM data mask signal output
	32	SDQ		SDRAM data input and output
Total	50	—	—	—

Other Signals

Signal type	Number of pins	Symbol	Description	Notes
CPU and test signals	4	GP_ADR1	GP address input	General-purpose parallel bus address input/test setting
	4	GP_ADR2	GP address input	General-purpose parallel bus address input/test setting
	8	GP_IO	GP I/O	General-purpose parallel bus I/O or test circuit outputs
	1	GP_WR		General-purpose parallel bus write enable
	1	GP_CS		General-purpose parallel bus chip select
	1	GP_MOD		Internal register control method selection High: Parallel bus mode Low: I^2C bus mode
	1	GP_TST_SW		General-purpose parallel bus I/O or test mode switching High: Parallel bus mode Low: Test mode
	6	TSTI	Test input	Test inputs. These pins are normally left open.
	5	TSTO	Test output	Test outputs. These pins are normally left open.
Total	33	—	—	—

Specifications

Absolute Maximum Ragings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage (I/O)	$DV_{DD}33$		–0.3 to +3.96	V
	$AV_{DD}33$			
Maximum supply voltage (core)	$DV_{DD}18$		–0.3 to +2.16	V
	$DPV_{DD}18$			
Input voltage	V_I		–0.5 to 6.0	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max		1	W
Storage temperature	Tstg		–55 to +125	°C
Operating temperature	Topr		–30 to +70	°C

Allowable Operating Ranges at Ta = –30 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage (I/O)	$DV_{DD}33$		3.15	3.3	3.45	V
Supply voltage (core)	$V_{DD}18$		1.71	1.8	1.89	V
Input voltage range	V_{IN}		0		5.5	V

Input and Output Pin Capacitance at Ta = 25°C, V_{DD} = V_I = 0 V

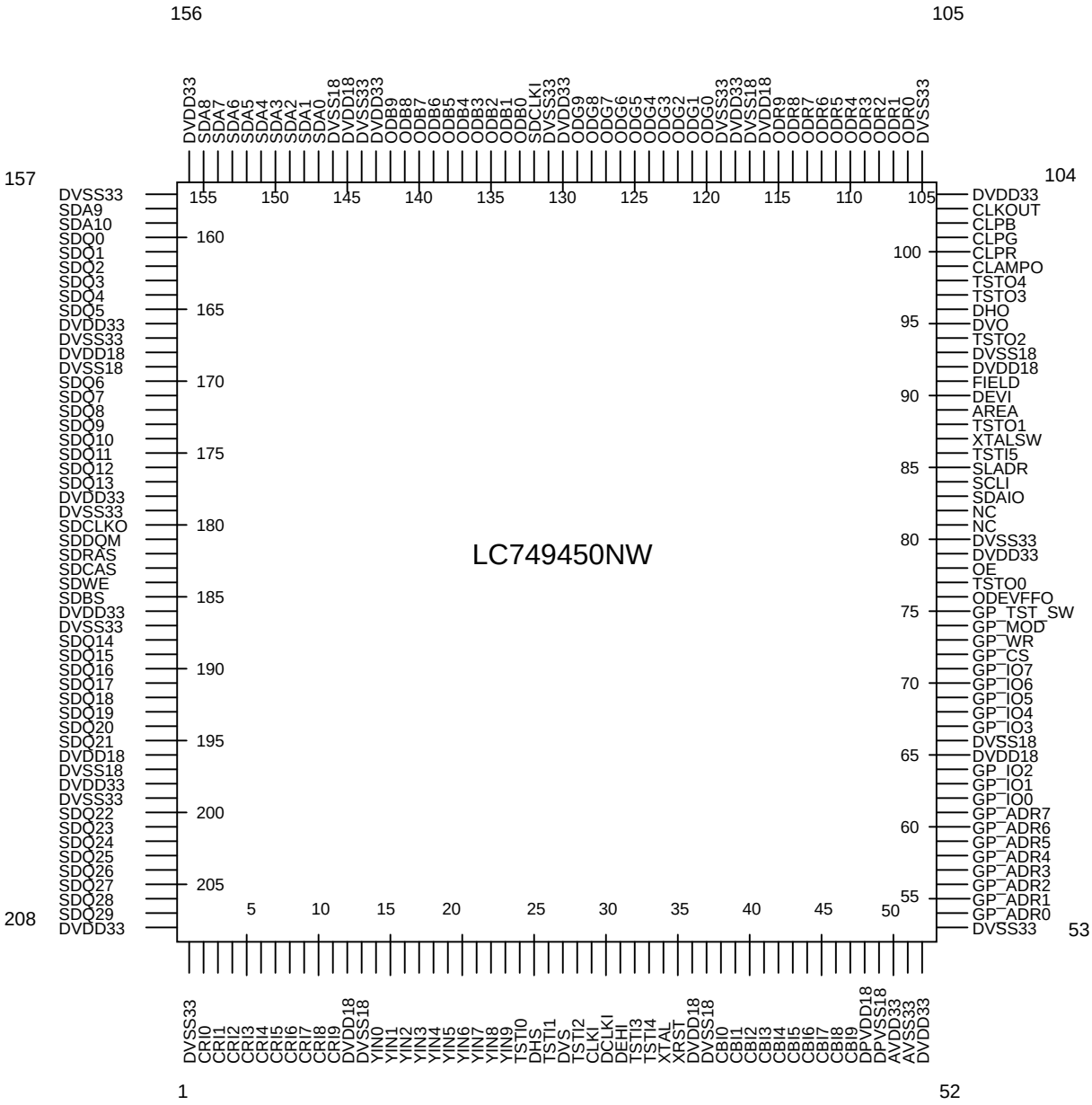
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input pins	C_{IN}	f = 1 MHz			10	pF
Output pins	C_{OUT}	f = 1 MHz			10	pF
I/O pins	$C_{I/O}$	f = 1 MHz			10	pF

DC Characteristics at Ta = –30 to +70°C, V_{DD}33 = 3.15 to 3.45 V, V_{DD}18 = 1.71 to 1.89 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level input voltage	V_{IH}	5 V inputs	2.0		5.5	V
		5 V Schmitt inputs	1.50		5.5	V
Low-level input voltage	V_{IL}	5 V inputs	–0.3		0.8	V
		5 V Schmitt inputs	–0.3		0.90	V
High-level input current	I_{IH}	V_I = V_{DD}	–10		+10	µA
		V_I = V_{DD}, with pull-down resistor used	+10		+100	µA
Low-level input current	I_{IL}	V_I = V_{SS}	–10		+10	µA
High-level output voltage	V_{OH}	T08 type, I_{OH} = –4 mA	V_{DD} – 0.8			V
		T12 type, I_{OH} = –8 mA	V_{DD} – 0.8			V
Low-level output voltage	V_{OL}	T08 type, I_{OL} = 4 mA			0.4	V
		T12 type, I_{OL} = 8 mA			0.4	V
Output leakage current	I_{OZ}	In the high-impedance output state	–10		+10	µA
Pull-down resistor	RDN		43	58	118	kΩ
Operating current drain	IDDOP	tck = 135 MHz		500		mA
Static current drain *1	IDDST	Outputs open, V_I = V_{SS} or V_{DD}		300		µA

*1: Some input pins have a built-in pull-down resistor. Note that there are thus certain circuit structures for which the static current drain cannot be guaranteed.

Pin Assignment



Top view

Pin Listing

Pin No.	Symbol	I/O circuit type		Connected to	Notes
		I/O	Circuit type		
1	$DV_{SS}33$	P	—	GND	3.3 V system ground
2	CRI0	I	PHICD	Digital interface	Cr/R signal input
3	CRI1	I			
4	CRI2	I			
5	CRI3	I			
6	CRI4	I			
7	CRI5	I			
8	CRI6	I			
9	CRI7	I			
10	CRI8	I			
11	CRI9	I			
12	$DV_{DD}18$	P	—	Power supply	1.8 V system power supply
13	$DV_{SS}18$	P	—	GND	1.8 V system ground
14	YIN0	I	PHICD	Digital interface	Y/G signal input RT.656 input
15	YIN1	I			
16	YIN2	I			
17	YIN3	I			
18	YIN4	I			
19	YIN5	I			
20	YIN6	I			
21	YIN7	I			
22	YIN8	I			
23	YIN9	I			
24	TSTI0	I	PHICD	Open	Test input. This pin is normally left open.
25	DHS	I	PHICD		Horizontal sync signal (The polarity can be switched.)
26	TSTI1	I	PHICD	Open	Test input. This pin is normally left open.
27	DVS	I	PHICD		Vertical sync signal (The polarity can be switched.)
28	TSTI2	I	PHISD	Open	Test input. This pin is normally left open.
29	CLKI	I	PHIC		System clock
30	DCLKI	I	PHIC		System clock
31	DEHI	I	PHICD		Valid video period enable signal input
32	TSTI3	I	PHISD	Open	Test input. This pin is normally left open.
33	TSTI4	I	PHICD	Open	Test input. This pin is normally left open.
34	XTAL	I	PHIC		Fixed clock connection
35	XRST	I	PHIS	Initialization circuit	System reset (Reset on a low-level input)
36	$DV_{DD}18$	P	—	Power supply	1.8 V system power supply
37	$DV_{SS}18$	P	—	GND	1.8 V system ground
38	CBI0	I	PHICD	Digital interface	Cb/B signal input
39	CBI1	I			
40	CBI2	I			
41	CBI3	I			
42	CBI4	I			
43	CBI5	I			
44	CBI6	I			
45	CBI7	I			
46	CBI8	I			
47	CBI9	I			
48	$DPV_{DD}18$	P	—	Power supply	PLL 1.8 V digital system power supply
49	$DPV_{SS}18$	P	—	GND	PLL 1.8 V digital system ground
50	$AV_{DD}33$	P	—	Power supply	PLL 3.3 V analog system power supply
51	$AV_{SS}33$	P	—	GND	PLL 3.3 V analog system ground
52	$DV_{DD}33$	P	—	Power supply	3.3 V system power supply
53	$DV_{SS}33$	P	—	GND	3.3 V system ground
54	GP_ADR0	I	PHICD		CPU address input or Test mode subsidiary setting inputs
55	GP_ADR1	I			
56	GP_ADR2	I			
57	GP_ADR3	I			
58	GP_ADR4	I			
59	GP_ADR5	I			
60	GP_ADR6	I			
61	GP_ADR7	I			

Continued on next page.

Continued from preceding page.

Pin No.	Symbol	I/O circuit type		Connected to	Notes
		I/O	Circuit type		
62	GP_IO0	B	PHBT08		CPU I/O or Test circuit outputs
63	GP_IO1	B			
64	GP_IO2	B			
65	$DV_{DD}18$	P	—	Power supply	1.8 V system power supply
66	$DV_{SS}18$	P	—	GND	1.8 V system ground
67	GP_IO3	B	PHBT08		CPU I/O or Test circuit outputs
68	GP_IO4	B			
69	GP_IO5	B			
70	GP_IO6	B			
71	GP_IO7	B			
72	GP_CS	I	PHICD		CPU bus chip enable input
73	GP_WR	I	PHICD		CPU bus write enable input
74	GP_MOD	I	PHICD		CPU bus mode switch
75	CPU_TST_SW	I	PHISD		CPU/test mode switch
76	ODEVFFO	O	PHOT08		Field discrimination signal output
77	TSTO0	O	PHOT12	Open	Test output. This pin is normally left open.
78	OE	I	PHISD		Output enable
79	$DVD_{DD}33$	P	—	Power supply	3.3 V system power supply
80	$DV_{SS}33$	P	—	GND	3.3 V system ground
81	NC	—	—	Open	No connection
82	NC	—	—	Open	No connection
83	SDAIO	B	PHBT12		I^2C bus data I/O
84	SCLI	I	PHISD		I^2C bus clock input
85	SLADR	I	PHISD		I^2C bus slave address setting
86	TST15	I	PHISD	Open	Test input. This pin is normally left open.
87	XTALSW	I	PHISD		XTAL clock pin input mode setting input
88	TSTO1	O	PHOT08	Open	Test output. This pin is normally left open.
89	AREAO	O	PHOT08		Valid area signal output
90	DEVI	I	PHICD		Vertical valid video period enable signal input
91	FIELD	I	PHICD		Field signal input
92	$DV_{DD}18$	P	—	Power supply	1.8 V system power supply
93	$DV_{SS}18$	P	—	GND	1.8 V system ground
94	TSTO2	O	PHOT08	Open	Test output. This pin is normally left open.
95	DVO	O	PHOT08		Vertical sync signal output (The polarity can be switched.)
96	DHO	O	PHOT08		Horizontal sync signal output (The polarity can be switched.)
97	TSTO3	O	PHOT08	Open	Test output. This pin is normally left open.
98	TSTO4	O	PHOT08	Open	Test output. This pin is normally left open.
99	CLAMPOO	O	PHOT08		A/D conversion clamp period verification pulse output
100	CLPR	O	PHOT12		Clamp control output (R/Cr)
101	CLPG	O	PHOT12		Clamp control output (G/Y)
102	CLPB	O	PHOT12		Clamp control output (B/Cb)
103	CLKOUT	O	PHOT12		Clock output
104	$DV_{DD}33$	P	—	Power supply	3.3 V system power supply
105	$DV_{SS}33$	P	—	GND	3.3 V system ground
106	ODR0	O	PHOT08		R signal outputs
107	ODR1	O			
108	ODR2	O			
109	ODR3	O			
110	ODR4	O			
111	ODR5	O			
112	ODR6	O			
113	ODR7	O			
114	ODR8	O			
115	ODR9	O			
116	$DV_{DD}18$	P	—	Power supply	1.8 V system power supply
117	$DV_{SS}18$	P	—	GND	1.8 V system ground
118	$DV_{DD}33$	P	—	Power supply	3.3 V system power supply
119	$DV_{SS}33$	P	—	GND	3.3 V system ground

Continued on next page.

Continued from preceding page.

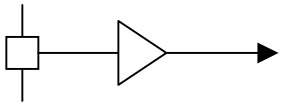
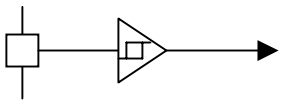
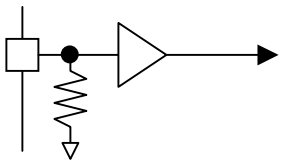
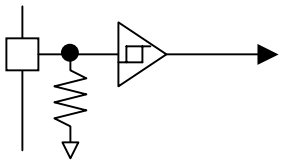
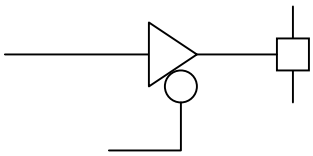
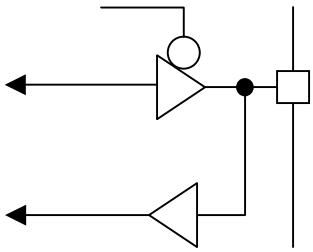
Pin No.	Symbol	I/O circuit type		Connected to	Notes
		I/O	Circuit type		
120	ODG0	O	PHOT08		G signal outputs
121	ODG1	O			
122	ODG2	O			
123	ODG3	O			
124	ODG4	O			
125	ODG5	O			
126	ODG6	O			
127	ODG7	O			
128	ODG8	O			
129	ODG9	O			
130	$DV_{DD}33$	P	—	Power supply	3.3 V system power supply
131	$DV_{SS}33$	P	—	GND	3.3 V system ground
132	SDCLKI	I	PHIC		SDRAM system clock
133	ODB0	O	PHOT08		B signal outputs
134	ODB1	O			
135	ODB2	O			
136	ODB3	O			
137	ODB4	O			
138	ODB5	O			
139	ODB6	O			
140	ODB7	O			
141	ODB8	O			
142	ODB9	O			
143	$DV_{DD}33$	P	—	Power supply	3.3 V system power supply
144	$DV_{SS}33$	P	—	GND	3.3 V system ground
145	$DV_{DD}18$	P	—	Power supply	1.8 V system power supply
146	$DV_{SS}18$	P	—	GND	1.8 V system ground
147	SAD0	O	PHOT12		SDRAM address outputs
148	SAD1	O			
149	SAD2	O			
150	SAD3	O			
151	SAD4	O			
152	SAD5	O			
153	SAD6	O			
154	SAD7	O			
155	SAD8	O			
156	$DV_{DD}33$	P	—	Power supply	3.3 V system power supply
157	$DV_{SS}33$	P	—	GND	3.3 V system ground
158	SAD9	O	PHOT12		SDRAM address outputs
159	SAD10	O			
160	SDQ0	B	PHBT12		SDRAM data I/O
161	SDQ1	B			
162	SDQ2	B			
163	SDQ3	B			
164	SDQ4	B			
165	SDQ5	B			
166	$DV_{DD}33$	P	—	Power supply	3.3 V system power supply
167	$DV_{SS}33$	P	—	GND	3.3 V system ground
168	$DV_{DD}18$	P	—	Power supply	1.8 V system power supply
169	$DV_{SS}18$	P	—	GND	1.8 V system ground
170	SDQ6	B	PHBT12		SDRAM clock output
171	SDQ7	B			
172	SDQ8	B			
173	SDQ9	B			
174	SDQ10	B			
175	SDQ11	B			
176	SDQ12	B			
177	SDQ13	B			
178	$DV_{DD}33$	P	—	Power supply	3.3 V system power supply
179	$DV_{SS}33$	P	—	GND	3.3 V system ground

Continued on next page.

Continued from preceding page.

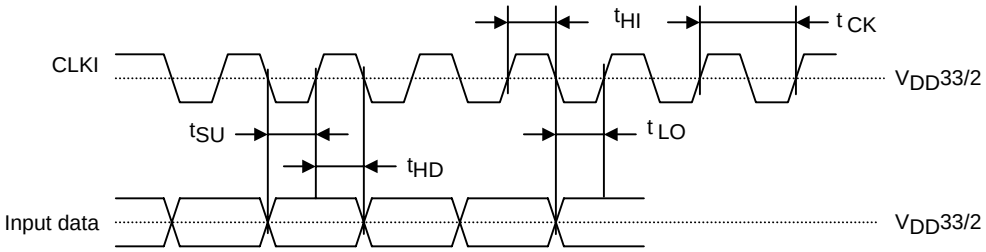
Pin No.	Symbol	I/O circuit type		Connected to	Notes
		I/O	Circuit type		
180	SDCLKO	O	PHOT12		SDRAM clock output
181	SDDQM	O	PHOT12		SDRAM data mask output
182	SDRAS	O	PHOT12		SDRAM row address strobe output
183	SDCAS	O	PHOT12		SDRAM column address strobe output
184	SDWE	O	PHOT12		SDRAM write enable output
185	SDBS	O	PHOT12		SDRAM bank select output
186	$DV_{DD}33$	P	—	Power supply	3.3 V system power supply
187	$DV_{SS}33$	P	—	GND	3.3 V system ground
188	SDQ14	B	PHBT12		SDRAM clock output
189	SDQ15	B			
190	SDQ16	B			
191	SDQ17	B			
192	SDQ18	B			
193	SDQ19	B			
194	SDQ20	B			
195	SDQ21	B			
196	$DV_{DD}18$	P	—	Power supply	1.8 V system power supply
197	$DV_{SS}18$	P	—	GND	1.8 V system ground
198	$DV_{DD}33$	P	—	Power supply	3.3 V system power supply
199	$DV_{SS}33$	P	—	GND	3.3 V system ground
200	SDQ22	B	PHBT12		SDRAM data I/O
201	SDQ23	B			
202	SDQ24	B			
203	SDQ25	B			
204	SDQ26	B			
205	SDQ27	B			
206	SDQ28	B			
207	SDQ29	B			
208	$DV_{DD}33$	P	—	Power supply	3.3 V system power supply

Pin Circuits

I/O type	Function	Applicable pins	Equivalent circuit
PHIC	5 V input	CLKI, DCLKI, XTALI, SDCLKI	
PHIS	5 V Schmitt input	XRST	
PHICD	5 V pull-down resistor input	YIN0 to 9, CBI0 to 9, CRI0 to 9, GP_ADR0 to 7, DEHI, DEVI, DHS, DVS, FIELD, GP_CS, GP_WR, GP_MOD, TSTI0, TSTI1, TSTI4	
PHISD	5 V pull-down resistor Schmitt input	XTAL_SW, SCLI, SLADR, OE, CPU_TST_SW, TSTI2, TSTI3, TSTI5	
PHOT08	8 mA 3-state drive output	ODR0 to 9, ODG0 to 9, ODB0 to 9, DHO, DVO, ODEVFFO, CLAMPOO, AREAO, TSTO1 to 4	
POT08	8 mA 3-state drive output	CLPB, CLPG, CLPR	
PHOT12	12 mA 3-state drive output	CLKOUT, SAD0 to 10, SDCLKO, SDRAS, SDCAS, SDWE, SDDQM, SDBS, TSTO0	
PHBT08	8 mA 3-state drive I/O	GP_IO0 to 7	
PHBT12	12 mA 3-state drive I/O	SDQ0 to 29, SDAIO	

Input and Output Data Timing

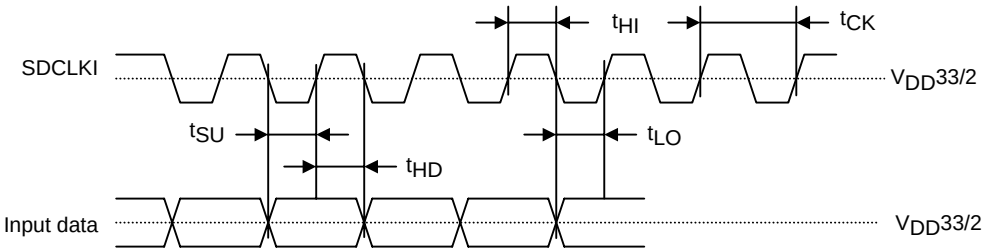
(1) Input Data Timing 1



Parameter	Symbol	Pins	min	max	Unit
Clock low-level time	t_{LO}	CLKI	3.70	—	ns
Clock high-level time	t_{HI}		3.70	—	ns
Clock period	t_{CK}		7.40	—	ns
Input data setup time	t_{SU}	YIN [9:0], CBI [9:0], CRI [9:0],	2.5	—	ns
Input data hold time	t_{HD}	DHS, DVS, DEHI, DEVI, FIELD	0.5	—	ns

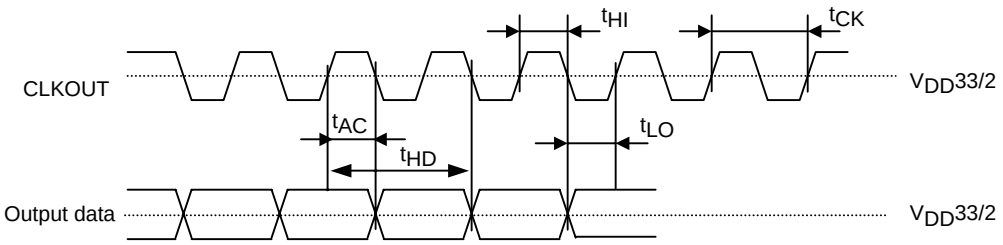
*: We recommend a duty of 50% for the input clock.

(2) Input Data Timing 2



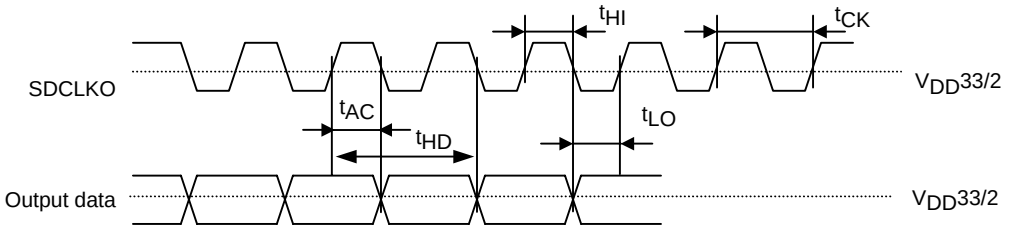
Parameter	Symbol	Pins	min	max	Unit
Clock low-level time	t_{LO}	SDCLKI	3.70	—	ns
Clock high-level time	t_{HI}		3.70	—	ns
Clock period	t_{CK}		7.40	—	ns
Input data setup time	t_{SU}	SDRAS, SDCAS, SDWE, SAD [10:0],	2	—	ns
Input data hold time	t_{HD}	SDBS, SDQ [29:0]	1	—	ns

(3) Output Data Timing 1



Parameter	Symbol	Pins	min	max	Unit
Clock low-level time	t_{LO}	CLKOUT	3.70	—	ns
Clock high-level time	t_{HI}		3.70	—	ns
Clock period	t_{CK}		7.40	—	ns
Output data delay time	t_{AC}	ODR [9:0], ODG [9:0], ODB [9:0], DHO,	–1.5	1.5	ns
Input data hold time	t_{HD}	DVO, AREA	5.90	—	ns

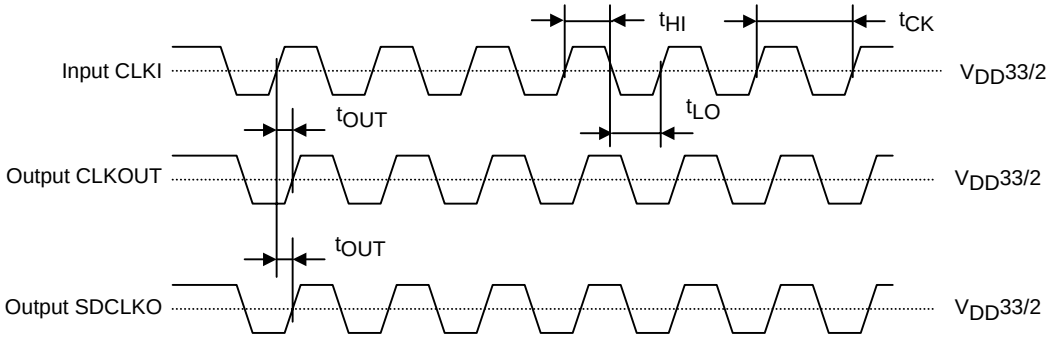
(4) Output Data Timing 2



Parameter	Symbol	Pins	min	max	Unit
Clock low-level time	t_{LO}	SDCLKO	3.70	—	ns
Clock high-level time	t_{HI}		3.70	—	ns
Clock period	t_{CK}		7.40	—	ns
Output data delay time	t_{AC}	SDQ [29:0]	–1.0	1.0	ns
Input data hold time	t_{HD}		4	—	ns

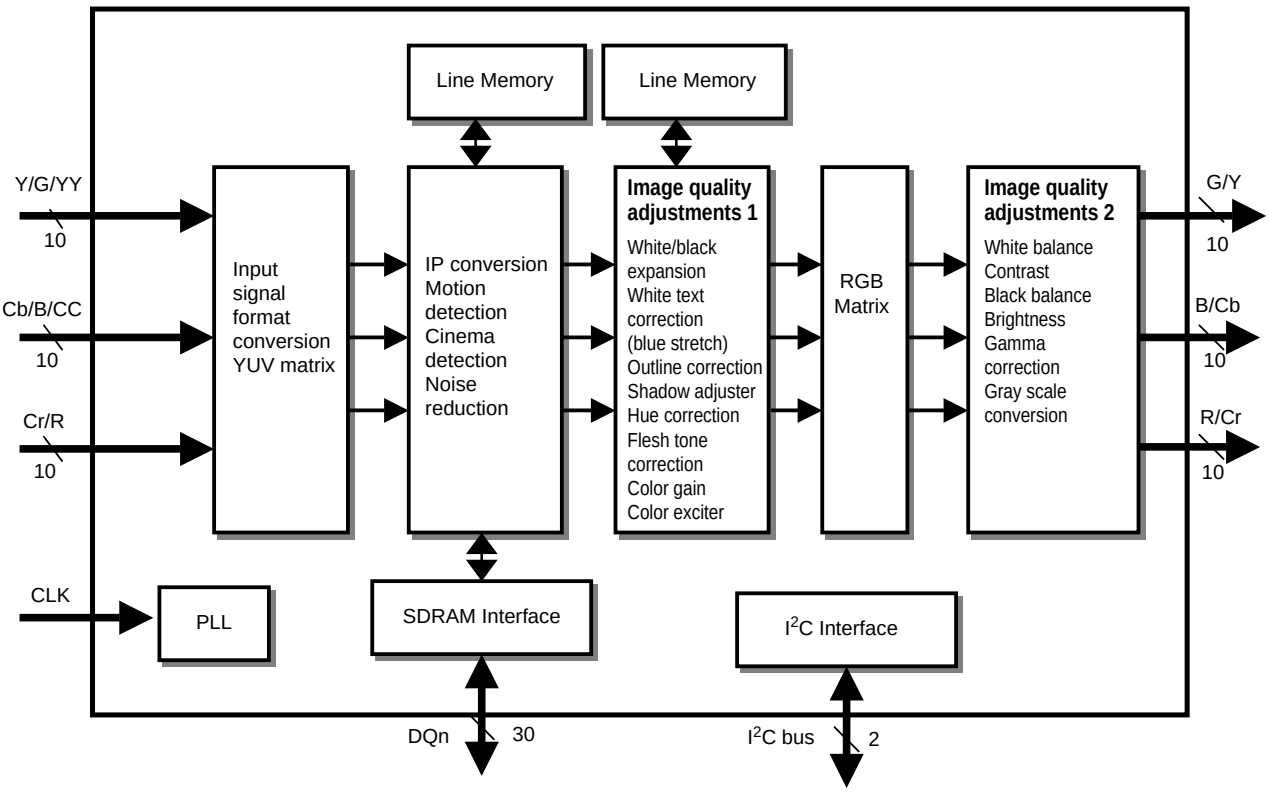
I/O Clock Timing

(1) Input System Clock Timing



Parameter	Symbol	Pins	min	max	Unit
Clock low-level time	t_{LO}	CLKI	3.70	—	ns
Clock high-level time	t_{HI}		3.70	—	ns
Clock period	t_{CK}		7.40	—	ns
CLKOUT delay time	t_{OUT}	CLKOUT	4	17	ns
SDCLK delay time	t_{OUT}	SDCLKO	4	17	ns

Block Diagram



Application Circuit Example