

SANYO Semiconductors DATA SHEET

Silicon Gate CMOS IC LC749450NW — Digital RGB Image Processor IC

Overview

The LC749450NW RGB image processing IC converts interlaced video signals such as NTSC and PAL to progressive scan and adjusts the image quality of that signal. Since the LC749450NW can operate at input clock frequencies up to 27 MHz, it is optimal as a pixel display device IC for high-quality high-resolution images. A high image quality progressive scan signal playback system can be implemented easily by combining the LC749450NW with external memory (two 16M SDRAMs).

Features

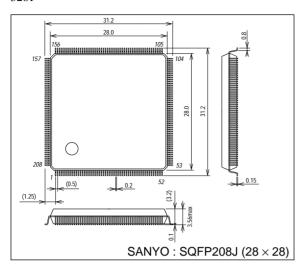
- Accepts 30-bit (4:4:4) YCbCr signals, 20-bit (4:2:2) YCbCr signals, and 10-bit RT.656 signals as inputs.
- Supports digital TV inputs (480i, 480p, 1080i, and 720p): 30-bit YCbCr digital signal input.
- 30-bit digital RGB signal inputs
- Produces 30-bit and 24-bit digital RGB (or YCbCr) signal outputs
- Provides both YCbCr/YPbPr → RGB conversion and RGB → YCbCr conversion
- Motion adaptive jaggy-less interlaced to progressive conversion
- 3:2 pull down
- Multiple noise reduction systems (1D, 2D, and 3D)
- Cross color and cross luminance cancellers
- Horizontal outline correction (LTI and CTI)
- Sharpness (horizontal and vertical)
- Sharpness adjuster (shading relief enhancement)
- White and black level expansion, white text correction (blue stretch)
- Flesh tone correction
- Hue and color gain adjustments
- Color exciter (6-phase RGBYMC independent saturation adjustment)
- · Brightness and contrast adjustment
- White balance and black balance adjustment
- Gamma correction (Independent RGB, programmable LUT system)
- Dithering (10-bit and 8-bit)
- · Clamp control
- Aspect ratio conversion $(4:3 \rightarrow 16:9)$
- Clock generator (PLL) circuit
- · SDRAM interface
- I²C bus and CPU interface circuits

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Package Dimensions

unit : mm 3261



IC Specifications

• Supply voltage: Core block: 1.8 V, I/O blocks: 3.3 V

• Maximum operating frequency: 27 MHz (IP conversion mode), 135 MHz (IP conversion not used)

• Package: 208-pin SQFP

Main Applications

• LCD TVs, monitors, and projectors

• PDP TVs and progressive scan TVs

• DVD players and recorders

Functional Overview

1. Input signal formats

The digital data port supports the following input signal formats.

30-bit RGB

30-bit (4:4:4) YCbCr/YPbPr

20-bit (4:2:2) YCbCr/YPbPr

10-bit signals conforming to the ITU-R BT.656 standard (horizontal and vertical sync inputs required)

NTSC (480i/480p), PAL (576i/576p), and HD (1080i/720p) RGB (up to 135 MHz)

2. IP conversion block

For NTSC (480i) and PAL (576i) inputs the LC749450NW provides motion adaptive IP conversion or cinema IP conversion (3:2 pull down) with both 2D/3D noise reduction and cross color/cross luminance cancellation. External SDRAM (either 2×16 Mbits or 1×64 Mbits) is required when the functions of this block are enabled. This block is set to bypass mode for 480p, 576p, 1080i, 720p, and PC (RGB) inputs.

(1) Motion adaptive IP conversion

The LC749450NW performs motion detection for each pixel that enters the IP conversion block. Based on that result, the block performs interlaced to progressive conversion. Pixels that are found to be static are interpolated between fields and pixels that are found to be moving are interpolated within the field.

Since this circuit takes correlations in the diagonal directions into account when performing inter-field interpolation for moving sections of the image, it can create smooth video with minimal stair-stepping artifacts (jaggies). Furthermore, this function can handle images that range from relaxed smooth video to video with violent motion by setting parameters and changing the motion threshold values for each pixel.

Continued from preceding page.

(2) Cinema mode IP conversion (3:2 pull down)

When an NTSC interlaced signal that was generated by a film (cinema) source is input, it automatically recognizes the signal as a cinema source and performs cinema mode IP conversion that is optimal for cinema sources. The threshold value for that recognition can be set with a parameter.

(3) Noise reduction (2D, 3D)

The LC749450NW provides three noise reduction functions: 3D noise reduction, which reduces noise between fields, 2D noise reduction, which reduces noise within the field, and 1D noise reduction, which reduces noise in the scan line direction. This block contains the 3D and 2D noise reduction functions and can operate independently for both the luminance signal and the chrominance signal.

(4) Cross color and cross luminance canceller

This circuit can reduce the cross color noise (rainbow-like color smearing) and cross luminance (dot) noise that is generated when a decoder (such as a 3-line decoder) other than 3D YC separator decoder is used for NTSC input. This function makes it possible to produce clear and vivid video with no color blotting and no dot interference.

3. Image quality adjustment block

The LC749450NW provides a full complement of image quality adjustment functions and can perform the image quality adjustments required for optimal flat panel TV display.

(1) Horizontal outline correction (LTI/CTI)

The LTI/CTI block applies outline correction to the input signal. The apparent sharpness in the video image is enhanced by increasing the slope of the input signal. Since this function does not add overshoot or undershoot to edges in the video signal, it creates natural-looking images. This function operates independently on the luminance and chrominance signals.

(2) Sharpness (horizontal and vertical)

The sharpness function can correct the outlines in the input signal. This function differs from the LTI/CTI function described above in that it adds an appropriate peak in the corrected outline area. The amount of this peak and a coring level that prevents fine noise from being aggravated can be set in the control registers for this circuit. This function only operates on the luminance signal.

(3) Shadow adjuster

The shadow adjuster function detects the outlines in the input signal and adds an appropriate peak before and after the outline to add an appearance of a shadow. This creates a video signal that is varied and not dull.

(4) White and black expansion

The white and black expansion function adaptively expands the white and black levels in the Y component of the YCbCr signal using the white and black peak levels in the immediately preceding field, the luminance signal average picture level (APL), distributional information, and microcontroller settings. The white and black peaks are the maximum and minimum values in the input data within a single field. When the white and black expansion function is used, the values of the settings must be set appropriately.

(5) White text correction (blue stretch)

The blue stretch function creates visually pleasing white text by adding a small amount of blue to white characters. A gain adjustment is applied to section of the Y signal recognized as white text and added to the Cb signal.

(6) Flesh tone correction

The flesh tone correction function extracts just the set skin color without affecting other colors and allows just that color to be adjusted.

(7) Hues and color gain adjustment

The hue adjustment adjusts the hue of the whole image. The color gain adjustment adjusts the depth of the color by controlling the gain applied to the color difference signals. This function can adjust the Cb and Cr signals independently.

(8) Color exciter

The color exciter can independently control the red, green, blue, magenta, yellow, and cyan colors.

(9) Brightness and contrast controls

The brightness control adjusts the brightness of the screen as a whole and the contrast control adjusts the gain applied to the brightness.

(10) White balance and black balance adjustments

These adjust the appearance of white and black on the LCD panel.

(11) Gamma correction

This function allows the creation of arbitrary gamma curves to match the characteristics of the LCD panel used. The RGB channels can be adjusted independently, using internal programmable LUT.

(12) Dithering

The LC749450NW performs internal signal processing with a 10-bit precision. When these signals are output as 8-bit values, the lower two bits are rounded by dithering.

4. Outputs and Other Functions

(1) Matrix conversion

The LC749450NW provides the following matrix conversion functions.

 $YCbCr \rightarrow RGB$ $YPbPr \rightarrow RGB$ $YPbPr \rightarrow YCbCr$ $RGB \rightarrow YCbCr$

(2) Aspect ratio conversion

An input Rec.601 signal (example: 720×240) can be expanded in the horizontal direction and displayed on a WVGA panel.

(3) Output formats

The LC749450NW can output video in the following formats.

Digital RGB (30 or 24 bits)

Digital YCbCr (30 or 24 bits)

(4) Clamp control

The LC749450NW can generate the clamp signals required for the front-end A/D converter. It can also generate arbitrary pulses (high, low, or high impedance) by comparing with an IC internal threshold value (that can be set with a register setting).

(5) SDRAM interface

The LC749450NW includes an SDRAM interface that can directly connect either:

Two 16 Mbit SDRAMs (512 words \times 16 bits \times 2 banks)

or

One 64 Mbit SDRAM (512 words \times 32 bits \times 4 banks).

This allows end product systems to be constructed easily.

SDRAMs with a speed grade of 70 or better must be used.

(6) I2C bus interface and CPU interface

The LC749450NW is basically designed to be controlled by setting internal registers over the I²C bus.

The slave address can be switched to match the system by controlling pin 85 (SLADR).

The following slave addresses are supported.

SLADR = low: E0h SLADR = high: E2h

Certain registers can also be controlled over the CPU interface.

I/O Specifications

Input Signals

Signal type	Number of pins	Symbol	Description	Notes
Video signals	10	YIN	Y or G	NTSC/PAL/DTV (4801, 480P, 1080I)
	10	CBI	Cb or B or C	or progressive scan RGB (up to SXGA)
	10	CRI	Cr or R or OSD	or NTSC/PAL decoder input
Sync signals	1	DHS	Horizontal sync signal	Pixel sync horizontal sync signal input
				The polarity can be switched by setting the DVPOLIN internal register.
	1	DVS	Vertical sync signal	Vertical sync signal input
				The polarity can be switched by setting the DVPOLIN internal register.
Data enable	1	DEHI	Data enable	Valid video period enable signal (horizontal/composite)
signals	1	DEVI	Vertical data enable	Valid video period enable signal (vertical)
	1	FIELD	Field signal input	Field signal input
Pixel clock	1	CLKI	Clock	System clock input
Fixed oscillator	1	DCLKI	Used for the output dot clock	System clock input
	1	XTAL		Fixed clock input or test clock input
System reset	1	XRST	System reset	System reset input, active low
Total	40	_		_

Output Signals

Signal type	Number of pins	Symbol	Description	Notes
Video signals	10	ODG	G	RGB output
	10	ODB	В	The LC749450NW also supports dithered 8-bit output.
	10	ODR	R	
Sync signals	1	DHO	Horizontal sync signal	This pin outputs the DHS pin input after a delay. (Used for pixel sync.)
				(This can be set over the I2C bus.)
	1	DVO	Vertical sync signal	Outputs a vertical pixel sync signal.
Data enable	1	AREA	Data enable	Outputs a valid area signal.
signals				
Pixel clocks	1	CLKOUT	Outputs the input clock	The polarity can be inverted.
Clamp pulse	1	CLAMPO	For A/D conversion	Outputs a pulse signal used for A/D conversion clamp period verification
signals				
Clamp levels	1	CLPG	Y/G clamp level	Clamp level discrimination output
	1	CLPB	Cb/B clamp level	(Too large: low, too small: high, match: high-impedance)
	1	CLPR	Cr/R clamp level	
Field	1	ODEVPPO	Field discrimination	Outputs an odd/even field discrimination signal
discrimination				(Used when IP conversion is not used.)
signals				
Total	39	_	_	_

Control Signals

Signal type	Number of pins	Symbol	Description	Notes
I ² C bus signals	1	SDAIO	Data bus	Used for setting internal registers and reading out the internal status.
	1	SCLI	Bus clock	The slave address is "1110000+(R/W)".
	1	SLADR	Slave switching	Sets the I ² C bus slave address.
				Normally low, High: E2h, Low: E0h.
Data output	1	OE		Data output enable signal
signals				
XTAL	1	XTALSW		This signal sets the XTAL clock pin input operation
				High: The XTAL clock input signal is divided by 2.
Total	5	_	_	_

SDRAM Control Signals

Signal type	Number of pins	Symbol	Description	Notes
Clock signals	1	SDCLKI		SDRAM clock input
	1	SDCLKO		SDRAM clock output
Control system	1	SDRAS		SDRAM row address strobe signal output
signals	1	SDCAS		SDRAM column address strobe signal output
	1	SDWE		SDRAM write enable signal output
Address system	11	SAD		SDRAM address signal output
signals	1	SDBS		SDRAM bank select signal output
Data system	1	SDDQM		SDRAM data mask signal output
signals	32	SDQ		SDRAM data input and output
Total	50	_	_	_

Other Signals

Signal type	Number of pins	Symbol	Description	Notes
CPU and test	4	GP_ADR1	GP address input	General-purpose parallel bus address input/test setting
signals	4	GP_ADR2	GP address input	General-purpose parallel bus address input/test setting
	8	GP_IO	GP I/O	General-purpose parallel bus I/O or test circuit outputs
	1	GP_WR		General-purpose parallel bus write enable
	1	GP_CS		General-purpose parallel bus chip select
	1	GP_MOD		Internal register control method selection
				High: Parallel bus mode
				Low: I ² C bus mode
	1	GP_TST_SW		General-purpose parallel bus I/O or test mode switching
				High: Parallel bus mode
				Low: Test mode
	6	TSTI	Test input	Test inputs. These pins are normally left open.
	5	TSTO	Test output	Test outputs. These pins are normally left open.
Total	33	_	_	_

Specifications

Absolute Maximum Ragings at $V_{SS} = 0 \ V$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum aupply voltage (I/O)	DV _{DD} 33		-0.3 to +3.96	V
Maximum supply voltage (I/O)	AV _{DD} 33		-0.3 10 +3.90	V
Maximum aunah valtaga (aara)	DV _{DD} 18		-0.3 to +2.16	V
Maximum supply voltage (core)	DPV _{DD} 18		-0.3 (0 +2.16	V
Input voltage	VI		-0.5 to 6.0	V
Output voltage	Vo		-0.3 to $V_{DD} + 0.3$	V
Allowable power dissipation	Pd max		1	W
Storage temperature	Tstg		-55 to +125	°C
Operating temperature	Topr		-30 to +70	°C

Allowable Operating Ranges at $Ta = -30 \text{ to } +70^{\circ}\text{C}$

Parameter	Symbol	Conditions		Ratings		Unit
Faranietei	Symbol	Conditions	min	typ	max	Offic
Supply voltage (I/O)	DV _{DD} 33		3.15	3.3	3.45	V
Supply voltage (core)	V _{DD} 18		1.71	1.8	1.89	V
Input voltage range	V _{IN}		0		5.5	V

Input and Output Pin Capacitance at $Ta=25^{\circ}C,\,V_{DD}=V_{I}=0~V$

Parameter	Symbol	Conditions		Ratings		Unit
Faranielei	Symbol	Conditions	min	typ	max	Offic
Input pins	C _{IN}	f = 1 MHz			10	pF
Output pins	C _{OUT}	f = 1 MHz			10	pF
I/O pins	C _{I/O}	f = 1 MHz			10	pF

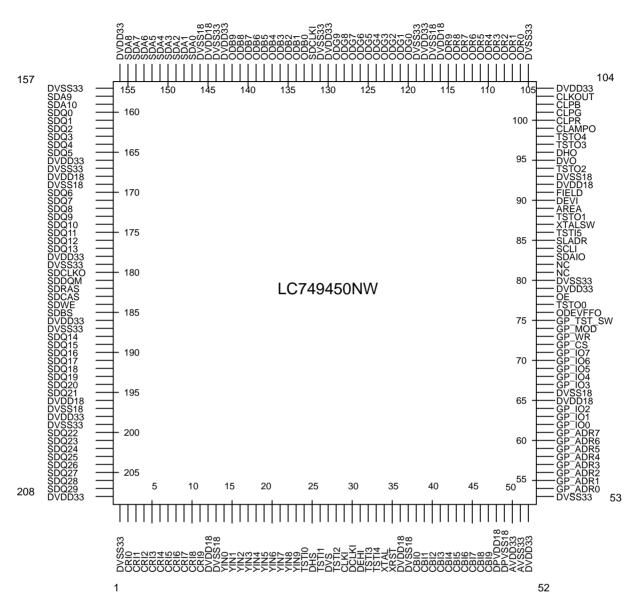
DC Characteristics at $Ta = -30 \text{ to } +70^{\circ}\text{C}$, $V_{DD}33 = 3.15 \text{ to } 3.45 \text{ V}$, $V_{DD}18 = 1.71 \text{ to } 1.89 \text{ V}$

D	0	O and distance		I India		
Parameter	Symbol	Conditions	min	typ	max	Unit
High level input voltage	W	5 V inputs	2.0		5.5	V
High-level input voltage	V _{IH}	5 V Schmitt inputs	1.50		5.5	V
Law level input valtage	.,	5 V inputs	-0.3		0.8	V
Low-level input voltage	V _{IL}	5 V Schmitt inputs	-0.3		0.90	V
High level input current		$V_I = V_{DD}$	-10		+10	μΑ
High-level input current	Ін	$V_I = V_{DD}$, with pull-down resistor used	+10		+100	μΑ
Low-level input current	I _{IL}	V _I = V _{SS}	-10		+10	μΑ
Llieb lovel output voltage	.,	T08 type, $I_{OH} = -4 \text{ mA}$	V _{DD} – 0.8			V
High-level output voltage	Voh	T12 type, $I_{OH} = -8 \text{ mA}$	V _{DD} – 0.8			V
Low level output voltage	V	T08 type, I _{OL} = 4 mA			0.4	V
Low-level output voltage	V _{OL}	T12 type, I _{OL} = 8 mA			0.4	V
Output leakage current	I _{OZ}	In the high-impedance output state	-10		+10	μΑ
Pull-down resistor	RDN		43	58	118	kΩ
Operating current drain	IDDOP	tck = 135 MHz		500		mA
Static current drain *1	IDDST	Outputs open, $V_I = V_{SS}$ or V_{DD}		300		μΑ

^{*1:} Some input pins have a built-in pull-down resistor. Note that there are thus certain circuit structures for which the static current drain cannot be guaranteed.

Pin Assignment





Top view

Pin Listing

Pin No.	Symbol	1/0	circuit type Circuit type	Connected to	Notes
1	DV _{SS} 33	1/O P		GND	3.3 V system ground
2	CRI0	I	_	GND	3.3 v system ground
3		-			
	CRI1	<u> </u>			
4	CRI2	l			
5	CRI3	l			
6	CRI4	I	PHICD	Digital interface	Cr/R signal input
7	CRI5	I		· ·	
8	CRI6	I			
9	CRI7	I			
10	CRI8	I			
11	CRI9	I			
12	DV _{DD} 18	Р	_	Power supply	1.8 V system power supply
13	DV _{SS} 18	Р	_	GND	1.8 V system ground
14	YIN0	I			
15	YIN1	ı			
16	YIN2	ı			
17	YIN3	i			
18	YIN4	ı			Y/G signal input
19	YIN5	i	PHICD	Digital interface	RT.656 input
20	YIN6	i			TT. 500 input
21	YIN7	l			
22	YIN8	l			
23	YIN9	I			<u> </u>
24	TSTI0	I	PHICD	Open	Test input. This pin is normally left open.
25	DHS	I	PHICD		Horizontal sync signal (The polarity can be switched.)
26	TSTI1	I	PHICD	Open	Test input. This pin is normally left open.
27	DVS	I	PHICD		Vertical sync signal (The polarity can be switched.)
28	TSTI2	I	PHISD	Open	Test input. This pin is normally left open.
29	CLKI	I	PHIC		System clock
30	DCLKI	I	PHIC		System clock
31	DEHI	I	PHICD		Valid video period enable signal input
32	TSTI3	I	PHISD	Open	Test input. This pin is normally left open.
33	TSTI4	I	PHICD	Open	Test input. This pin is normally left open.
34	XTAL	ı	PHIC		Fixed clock connection
35	XRST	ı	PHIS	Initialization circuit	System reset (Reset on a low-level input)
36	DV _{DD} 18	Р	_	Power supply	1.8 V system power supply
37	DV _{SS} 18	Р	_	GND	1.8 V system ground
38	CBI0	1			
39	CBI1	ı			
40	CBI2	i			
41	CBI2	i			
42	CBI4	ı			
			PHICD	Digital interface	Cb/B signal input
43	CBI5	ı			
44	CBI6	l			
45	CBI7	- I			
46	CBI8	l .			
47	CBI9	I			
48	DPV _{DD} 18	Р	_	Power supply	PLL 1.8 V digital system power supply
49	DPV _{SS} 18	Р	_	GND	PLL 1.8 V digital system ground
50	AV _{DD} 33	Р	_	Power supply	PLL 3.3 V analog system power supply
51	AV _{SS} 33	Р	_	GND	PLL 3.3 V analog system ground
52	DV _{DD} 33	Р	_	Power supply	3.3 V system power supply
53	DV _{SS} 33	Р	_	GND	3.3 V system ground
54	GP_ADR0	I			
55	GP_ADR1	i			
56	GP_ADR2	ı			
57	GP_ADR3	ı			CPU address input or
58	GP_ADR3 GP_ADR4	<u>'</u>	PHICD		Test mode subsidiary setting inputs
					rest mode subsidiary setting inputs
59	GP_ADR5	ı			
60	GP_ADR6	l			
61	GP_ADR7	I			

Continued from preceding page.

Pin No. Symbol Connected to Connected to CPU I/O or Test circuit outputs CPU I/O or Test output CPU I/O or Test output			1/0 (circuit type		
CPU I/O or	Pin No.	Symbol			Connected to	Notes
63	62	GP IO0		Circuit type		
Section Sect				PHRTOR		CPU I/O or
66 DV ₂₀ 18 P −				1110100		Test circuit outputs
66					Dawaraunnly	4.0.V system power symply
68 GP_IO3 B 69 GP_IO5 B 70 GP_IO6 B 71 GP_IO6 B 71 GP_IO7 B 72 GP_IO7 B 72 GP_IO7 B 73 GP_IO7 B 74 GP_IO7 B 74 GP_IO7 GP_IO				_		
Sea				_	GND	1.8 v system ground
GP GP GP GP GP GP GP GP						
Post						CPU I/O or
71				PHB108		Test circuit outputs
72 GP_CS I PHICD CPU bus chip enable input						·
73 GP_WR						
T4		GP_CS	ı	PHICD		CPU bus chip enable input
75	73	GP_WR	I	PHICD		CPU bus write enable input
76	74	GP_MOD	I	PHICD		CPU bus mode switch
77	75	CPU_TST_SW	I	PHISD		CPU/test mode switch
78 OE I PHISD Output enable 79 DVD _{DD33} 3 P — Power supply 3.3 V system power supply 80 DVS _S 33 P — GND 3.3 V system ground 81 NC — — Open No connection 82 NC — — Open No connection 83 SDAIO B PHBT12 PIBSD PIC bus clock input 84 SCLI I PHISD PIC bus slave address setting 85 SLADR I PHISD Open Test input. This pin is normally left open. 87 XTALSW I PHISD Open Test output. This pin is normally left open. 88 TST01 O PHOT08 Open Test output. This pin is normally left open. 89 AREAO O PHOT08 Valid area signal output 90 DEVI I PHICD Vertical syna signal output in put mode setting input 91 FIELD I	76	ODEVFFO	0	PHOT08		Field discrimination signal output
79 DVD _{DD} 33 P — Power supply 3.3 V system ground 80 DV _{SS} 33 P — GND 3.3 V system ground 81 NC — — Open No connection 82 NC — — Open No connection 83 SDAIO B PHBT12 PE Dus data I/O 84 SCLI I PHISD PE Dus data I/O 85 SLADR I PHISD PC Dus data I/O 86 TST15 I PHISD PC Dus data I/O 86 TST15 I PHISD Open Test input. This pin is normally left open. 87 XTALSW I PHISD XTAL clock pin input mode setting input 88 TST01 O PHOT08 Valid area signal output 90 DEVI I PHICD Vertical valid video period enable signal input 91 Field by I PHICD Vertical valid video period enable signal input 92 <td>77</td> <td>TSTO0</td> <td>0</td> <td>PHOT12</td> <td>Open</td> <td>Test output. This pin is normally left open.</td>	77	TSTO0	0	PHOT12	Open	Test output. This pin is normally left open.
80 DVss33 P — GND 3.3 V system ground	78	OE	I	PHISD		Output enable
81	79	DVD _{DD} 33	Р	_	Power supply	3.3 V system power supply
81	80	DV _{SS} 33	Р	_	GND	3.3 V system ground
82	81			_	Open	
83	82	NC		_	· · · · · · · · · · · · · · · · · · ·	No connection
SCLI			В	PHBT12	- Span	
85						
Ref						
87 XTALSW I PHISD XTAL clock pin input mode setting input 88 TSTO1 O PHOT08 Open Test output. This pin is normally left open. 89 AREAO O PHOT08 Valid area signal output 90 DEVI I PHICD Vertical valid video period enable signal input 91 FIELD I PHICD Field signal input 92 DV _{DD} 18 P — Power supply 1.8 V system power supply 93 DV _{SS} 18 P — GND 1.8 V system power supply 94 TSTO2 O PHOT08 Open Test output. This pin is normally left open. 95 DVO O PHOT08 Open Test output. This pin is normally left open. 96 DHO O PHOT08 Horizontal sync signal output (The polarity can be switched.) 97 TSTO3 O PHOT08 Open Test output. This pin is normally left open. 98 TSTO4 O PHOT08 Open Test output. This p			-		Open	
Record R					Ореп	
AREAO O PHOT08 Valid area signal output					0	
90				 	Open	
91						
92 DV _{DD} 18 P						
93 DVs_S18 P — GND 1.8 V system ground 94				PHICD		
94 TSTO2 O PHOT08 Open Test output. This pin is normally left open. 95 DVO O PHOT08 Vertical sync signal output (The polarity can be switched.) 96 DHO O PHOT08 Horizontal sync signal output (The polarity can be switched.) 97 TSTO3 O PHOT08 Open Test output. This pin is normally left open. 98 TSTO4 O PHOT08 Open Test output. This pin is normally left open. 99 CLAMPOO O PHOT08 Open Test output. This pin is normally left open. 100 CLPR O PHOT08 Open Test output. This pin is normally left open. 100 CLPR O PHOT08 Open Test output. This pin is normally left open. 100 CLPR O PHOT08 A/D conversion clamp period verification pulse output 101 CLPR O PHOT12 Clamp control output (R/Cr) 102 CLPB O PHOT12 Clamp control output (B/Cb) 103 CLKOUT O <td></td> <td></td> <td></td> <td>_</td> <td></td> <td></td>				_		
95 DVO O PHOT08 Vertical sync signal output (The polarity can be switched.) 96 DHO O PHOT08 Horizontal sync signal output (The polarity can be switched.) 97 TST03 O PHOT08 Open Test output. This pin is normally left open. 98 TST04 O PHOT08 Open Test output. This pin is normally left open. 99 CLAMPOO O PHOT08 A/D conversion clamp period verification pulse output 100 CLPR O PHOT12 Clamp control output (R/Cr) 101 CLPG O PHOT12 Clamp control output (G/Y) 102 CLPB O PHOT12 Clamp control output (B/Cb) 103 CLKOUT O PHOT12 Clock output 104 DV _{DD} 33 P — Power supply 3.3 V system power supply 105 DV _{SS} 33 P — GND 3.3 V system ground 106 ODR0 O O O O O O O O <td></td> <td></td> <td></td> <td>_</td> <td>GND</td> <td></td>				_	GND	
96 DHO 0 PHOT08 Horizontal sync signal output (The polarity can be switched. 97 TSTO3 0 PHOT08 Open Test output. This pin is normally left open. 98 TSTO4 0 PHOT08 Open Test output. This pin is normally left open. 99 CLAMPOO 0 PHOT08 A/D conversion clamp period verification pulse output 100 CLPR 0 PHOT12 Clamp control output (R/Cr) 101 CLPG 0 PHOT12 Clamp control output (B/Cr) 102 CLPB 0 PHOT12 Clamp control output (B/Cr) 103 CLKOUT 0 PHOT12 Clock output 104 DV _{DD} 33 P — Power supply 3.3 V system power supply 105 DV _{SS} 33 P — GND 3.3 V system ground 106 ODR0 0 107 ODR1 0 110 ODR4 0 111 ODR5 0 112 ODR6				PHOT08	Open	
97 TST03 O PHOT08 Open Test output. This pin is normally left open. 98 TST04 O PHOT08 Open Test output. This pin is normally left open. 99 CLAMPOO O PHOT08 A/D conversion clamp period verification pulse output 100 CLPR O PHOT12 Clamp control output (R/Cr) 101 CLPG O PHOT12 Clamp control output (G/Y) 102 CLPB O PHOT12 Clamp control output (B/Cb) 103 CLKOUT O PHOT12 Clock output 104 DV _{DD33} 3 P — Power supply 3.3 V system power supply 105 DV _{SS33} 3 P — GND 3.3 V system ground 106 ODR0 O ODR1 O 109 ODR3 O O 110 ODR4 O 111 ODR5 O 112 ODR6 O 113 ODR7 O	95	DVO	0	PHOT08		
98 TSTO4 O PHOT08 Open Test output. This pin is normally left open. 99 CLAMPOO O PHOT08 A/D conversion clamp period verification pulse output 100 CLPR O PHOT12 Clamp control output (R/Cr) 101 CLPG O PHOT12 Clamp control output (G/Y) 102 CLPB O PHOT12 Clamp control output (B/Cb) 103 CLKOUT O PHOT12 Clock output 104 DV _{DD} 33 P — Power supply 3.3 V system power supply 105 DV _{SS} 33 P — GND 3.3 V system ground 106 ODR0 O O O O O 107 ODR1 O <td< td=""><td>96</td><td>DHO</td><td>0</td><td>PHOT08</td><td></td><td>Horizontal sync signal output (The polarity can be switched.)</td></td<>	96	DHO	0	PHOT08		Horizontal sync signal output (The polarity can be switched.)
99	97	TSTO3	0	PHOT08	Open	Test output. This pin is normally left open.
100	98	TSTO4	0	PHOT08	Open	Test output. This pin is normally left open.
101	99	CLAMPOO	0	PHOT08		A/D conversion clamp period verification pulse output
102	100	CLPR	0	PHOT12		Clamp control output (R/Cr)
103	101	CLPG	0	PHOT12		Clamp control output (G/Y)
104	102	CLPB	0			Clamp control output (B/Cb)
104	103	CLKOUT	0	PHOT12		Clock output
105	104	DV _{DD} 33	Р	_	Power supply	3.3 V system power supply
106			Р	_		
107						· ·
108 ODR2 O 109 ODR3 O 110 ODR4 O 111 ODR5 O 112 ODR6 O 113 ODR7 O 114 ODR8 O 115 ODR9 O 116 DV _{DD} 18 P — Power supply 1.8 V system power supply				1		
109 ODR3 O 110 ODR4 O 111 ODR5 O 112 ODR6 O 113 ODR7 O 114 ODR8 O 115 ODR9 O 116 DV _{DD} 18 P — Power supply 1.8 V system power supply						
110 ODR4 O 111 ODR5 O 112 ODR6 O 113 ODR7 O 114 ODR8 O 115 ODR9 O 116 DV _{DD} 18 P — Power supply 1.8 V system power supply						
111						
112 ODR6 O 113 ODR7 O 114 ODR8 O 115 ODR9 O 116 DV _{DD} 18 P — Power supply 1.8 V system power supply				PHOT08		R signal outputs
113 ODR7 O 114 ODR8 O 115 ODR9 O 116 DV _{DD} 18 P — Power supply 1.8 V system power supply						
114 ODR8 O 115 ODR9 O 116 DV _{DD} 18 P — Power supply 1.8 V system power supply						
115 ODR9 O 116 DV _{DD} 18 P — Power supply 1.8 V system power supply						
116 DV _{DD} 18 P — Power supply 1.8 V system power supply						
						<u> </u>
117 DV _{SS} 18 P — GND 1.8 V system ground						
				_		
118 DV _{DD} 33 P — Power supply 3.3 V system power supply				_		
119 DV _{SS} 33 P — GND 3.3 V system ground	119	DV _{SS} 33	Р	_	GND	3.3 V system ground

Continued from preceding page.

Pin No.	Symbol		circuit type	Connected to	Notes
	-	1/0	Circuit type		
120	ODG0	0			
121	ODG1	0			
122	ODG2	0			
123	ODG3	0			
124	ODG4	0	PHOT08		G signal outputs
125	ODG5	0			
126	ODG6	0			
127	ODG7	0			
128	ODG8	0			
129	ODG9	0			
130	DV _{DD} 33	Р	_	Power supply	3.3 V system power supply
131	DV _{SS} 33	Р		GND	3.3 V system ground
132	SDCLKI	ı	PHIC		SDRAM system clock
133	ODB0	0]		
134	ODB1	0			
135	ODB2	0	1		
136	ODB3	0			
137	ODB4	0	PHOT08		B signal outputs
138	ODB5	0			V
139	ODB6	0	1		
140	ODB7	0]		
141	ODB8	0]		
142	ODB9	0			
143	DV _{DD} 33	Р	_	Power supply	3.3 V system power supply
144	DV _{SS} 33	Р	_	GND	3.3 V system ground
145	DV _{DD} 18	Р	_	Power supply	1.8 V system power supply
146	DV _{SS} 18	P	_	GND	1.8 V system ground
147	SAD0	0]		
148	SAD1	0]		
149	SAD2	0]		
150	SAD3	0]		
151	SAD4	0	PHOT12		SDRAM address outputs
152	SAD5	0]		
153	SAD6	0			
154	SAD7	0			
155	SAD8	0			
156	DV _{DD} 33	Р	_	Power supply	3.3 V system power supply
157	DV _{SS} 33	Р	_	GND	3.3 V system ground
158	SAD9	0	PHOT12		SDRAM address outputs
159	SAD10	0	1.70172		
160	SDQ0	В			
161	SDQ1	В]		
162	SDQ2	В	PHBT12		SDRAM data I/O
163	SDQ3	В	FIIDITZ		ODITATIVI data 1/O
164	SDQ4	В]		
165	SDQ5	В			
166	DV _{DD} 33	Р	_	Power supply	3.3 V system power supply
166				CND	3.3 V system ground
166	DV _{SS} 33	Р	_	GND	
		+	_	Power supply	1.8 V system power supply
167	DV _{SS} 33	Р	 		
167 168	DV _{SS} 33 DV _{DD} 18	P P	_	Power supply	1.8 V system power supply
167 168 169	DV _{SS} 33 DV _{DD} 18 DV _{SS} 18	P P P	_	Power supply	1.8 V system power supply
167 168 169 170	DV _{SS} 33 DV _{DD} 18 DV _{SS} 18 SDQ6	P P P B	_	Power supply	1.8 V system power supply
167 168 169 170 171	DV _{SS} 33 DV _{DD} 18 DV _{SS} 18 SDQ6 SDQ7	P P P B B		Power supply	1.8 V system power supply 1.8 V system ground
167 168 169 170 171 172	DV _{SS} 33 DV _{DD} 18 DV _{SS} 18 SDQ6 SDQ7 SDQ8	P P P B B B B	_	Power supply	1.8 V system power supply
167 168 169 170 171 172 173	DV _{SS} 33 DV _{DD} 18 DV _{SS} 18 SDQ6 SDQ7 SDQ8 SDQ9	P P P B B B B B		Power supply	1.8 V system power supply 1.8 V system ground
167 168 169 170 171 172 173 174	DV _{SS} 33 DV _{DD} 18 DV _{SS} 18 SDQ6 SDQ7 SDQ8 SDQ9 SDQ10	P P P B B B B B B B		Power supply	1.8 V system power supply 1.8 V system ground
167 168 169 170 171 172 173 174	DV _{SS} 33 DV _{DD} 18 DV _{SS} 18 SDQ6 SDQ7 SDQ8 SDQ9 SDQ10 SDQ11	P P P B B B B B B B B B		Power supply	1.8 V system power supply 1.8 V system ground
167 168 169 170 171 172 173 174 175	DV _{SS} 33 DV _{DD} 18 DV _{SS} 18 SDQ6 SDQ7 SDQ8 SDQ9 SDQ10 SDQ11 SDQ12	P P P B B B B B B B B B B B B B B B B B		Power supply	1.8 V system power supply 1.8 V system ground

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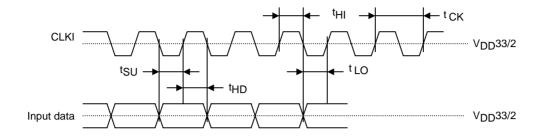
Pin No.	Symbol	I/O circuit type		Connected to	Notes		
Till No. Symbol		I/O	Circuit type		Notes		
180	SDCLKO	0	PHOT12		SDRAM clock output		
181	SDDQM	0	PHOT12		SDRAM data mask output		
182	SDRAS	0	PHOT12		SDRAM row address strobe output		
183	SDCAS	0	PHOT12		SDRAM column address strobe output		
184	SDWE	0	PHOT12		SDRAM write enable output		
185	SDBS	0	PHOT12		SDRAM bank select output		
186	DV _{DD} 33	Р	_	Power supply	3.3 V system power supply		
187	DV _{SS} 33	Р	_	GND	3.3 V system ground		
188	SDQ14	В					
189	SDQ15	В					
190	SDQ16	В					
191	SDQ17	В	PHBT12		SDRAM clock output		
192	SDQ18	В	РПБ112		SDRAW Clock output		
193	SDQ19	В					
194	SDQ20	В					
195	SDQ21	В					
196	DV _{DD} 18	Р	_	Power supply	1.8 V system power supply		
197	DV _{SS} 18	Р	_	GND	1.8 V system ground		
198	DV _{DD} 33	Р	_	Power supply	3.3 V system power supply		
199	DV _{SS} 33	Р	_	GND	3.3 V system ground		
200	SDQ22	В					
201	SDQ23	В					
202	SDQ24	В					
203	SDQ25	В	PHBT12		SDRAM data I/O		
204	SDQ26	В					
205	SDQ27	В					
206	SDQ28	В					
207	SDQ29	В					
208	DV _{DD} 33	Р	_	Power supply	3.3 V system power supply		

Pin Circuits

I/O type	Function	Applicable pins	Equivalent circuit
PHIC	5 V input	CLKI, DCLKI, XTALI, SDCLKI	
PHIS	5 V Schmitt input	XRST	
PHICD	5 V pull-down resistor input	YIN0 to 9, CBI0 to 9, CRI0 to 9, GP_ADR0 to 7, DEHI, DEVI, DHS, DVS, FIELD, GP_CS, GP_WR, GP_MOD, TSTI0, TSTI1, TSTI4	
PHISD	5 V pull-down resistor Schmitt input	XTAL_SW, SCLI, SLADR, OE, CPU_TST_SW, TSTI2, TSTI3, TSTI5	
PHOT08	8 mA 3-state drive output	ODR0 to 9, ODG0 to 9, ODB0 to 9, DHO, DVO, ODEVFFO, CLAMPOO, AREAO, TSTO1 to 4	
POT08	8 mA 3-state drive output	CLPB, CLPG, CLPR	
PHOT12	12 mA 3-state drive output	CLKOUT, SAD0 to 10, SDCLKO, SDRAS, SDCAS, SDWE, SDDQM, SDBS, TSTO0	
РНВТ08	8 mA 3-state drive I/O	GP_IO0 to 7	
PHBT12	12 mA 3-state drive I/O	SDQ0 to 29, SDAIO	

Input and Output Data Timing

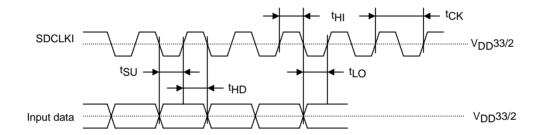
(1) Input Data Timing 1



Parameter	Symbol	Pins	min	max	Unit
Clock low-level time	t _{LO}		3.70	_	ns
Clock high-level time	t _{HI}	CLKI	3.70	_	ns
Clock period	t _{CK}		7.40	_	ns
Input data setup time	t _{SU}	YIN [9:0], CBI [9:0], CRI [9:0],	2.5	_	ns
Input data hold time	t _{HD}	DHS, DVS, DEHI, DEVI, FIELD	0.5		ns

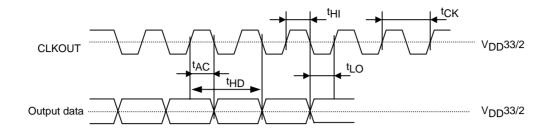
^{*:} We recommend a duty of 50% for the input clock.

(2) Input Data Timing 2



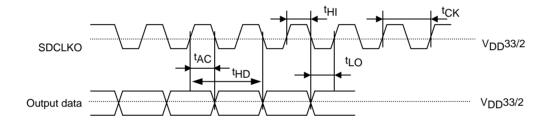
Parameter	Symbol	Pins	min	max	Unit
Clock low-level time	t _{LO}		3.70	_	ns
Clock high-level time	t _{HI}	SDCLKI	3.70	_	ns
Clock period	t _{CK}		7.40	_	ns
Input data setup time	t _{SU}	SDRAS, SDCAS, SDWE, SAD [10:0],	2	_	ns
Input data hold time	t _{HD}	SDBS, SDQ [29:0]	1	_	ns

(3) Output Data Timing 1



Parameter	Symbol	Pins	min	max	Unit
Clock low-level time	t _{LO}		3.70		ns
Clock high-level time	t _{HI}	CLKOUT	3.70	_	ns
Clock period	t _{CK}		7.40	_	ns
Output data delay time	t _{AC}	ODR [9:0], ODG [9:0], ODB [9:0], DHO,	-1.5	1.5	ns
Input data hold time	t _{HD}	DVO, AREA	5.90	_	ns

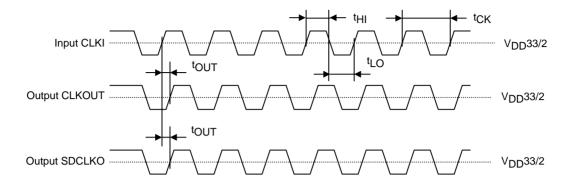
(4) Output Data Timing 2



Parameter	Symbol	Pins	min	max	Unit
Clock low-level time	t _{LO}		3.70	_	ns
Clock high-level time	t _{HI}	SDCLKO	3.70	_	ns
Clock period	t _{CK}		7.40	_	ns
Output data delay time	t _{AC}	SDQ [29:0]	-1.0	1.0	ns
Input data hold time	t _{HD}		4	_	ns

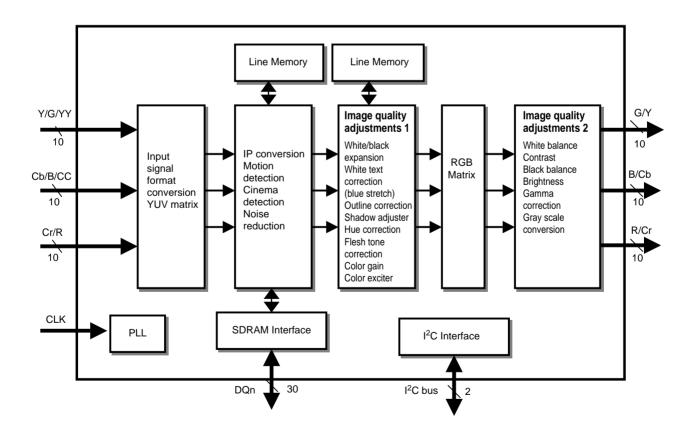
I/O Clock Timing

(1) Input System Clock Timing

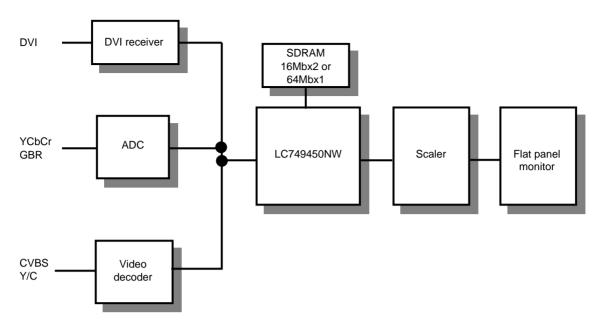


Parameter	Symbol	Pins	min	max	Unit
Clock low-level time	t _{LO}		3.70		ns
Clock high-level time	t _{HI}	CLKI	3.70	_	ns
Clock period	t _{CK}		7.40	_	ns
CLKOUT delay time	tout	CLKOUT	4	17	ns
SDCLK delay time	tout	SDCLKO	4	17	ns

Block Diagram



Application Circuit Example



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