AAT2785

SystemPower™

3-Channel Step-Down DC/DC Converter

General Description

The AAT2785 is a 3-channel 1.8MHz step-down converter for applications where power efficiency and solution size are critical. The input voltage range is 2.7V to 5.5V and the outputs are adjustable from 0.6V to V_{IN}.

The AAT2785 incorporates a unique low noise architecture which reduces ripple and spectral noise. Channel 3 delivers up to 1.5A output current and channels 1 and 2 deliver up to 600mA each. The AAT2785 uses a high switching frequency to minimize the size of external components. The AAT2785 requires a minimum of external components to realize a high efficiency triple-output buck converter minimizing solution cost and PCB footprint.

Each of the 3 regulators has an independent enable pin, adjustable output voltage and operates with low no load quiescent current, providing high efficiency over the entire load range.

The AAT2785 is available in a Pb-free 16 pin TDFN34 package, and is rated over the -40°C to +85°C operating temperature range.

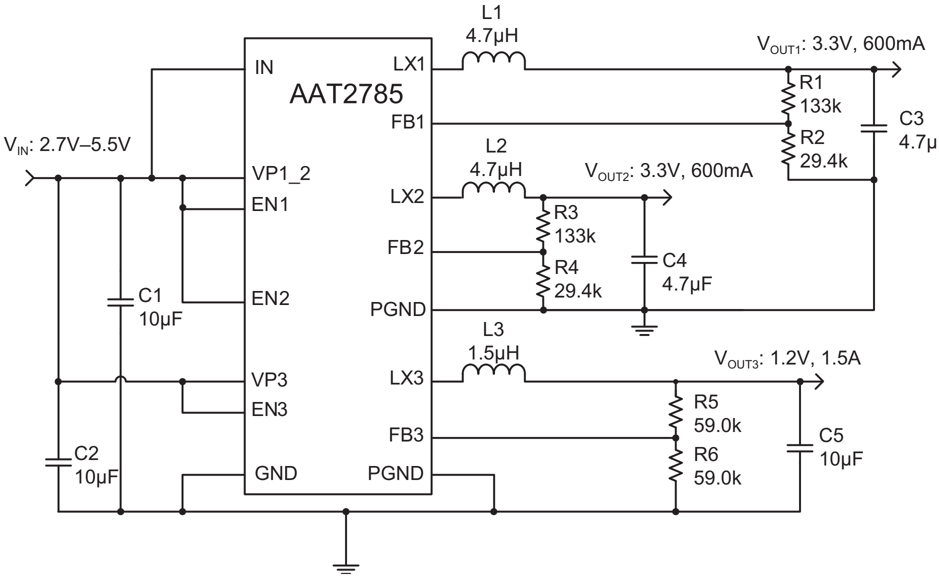
Features

- V_{IN} Range: 2.7 to 5.5V
- Output Voltage Range: 0.6V to V_{IN}
- Output Current:
  - Channel 3: 1.5A
  - Channel 1: 600mA
  - Channel 2: 600mA
- Low Noise Light Load Mode
- Low Ripple PWM Mode
- Highly Efficient Step-Down Converters
- Low $R_{DS(ON)}$ Integrated Power Switches
- 100% Duty Cycle
- 1.8MHz Switching Frequency
- Internal Soft Start
- Fast 150µs Turn-On Time
- Over-Temperature Protection
- Current Limit Protection
- TDFN34-16 Package
- -40°C to 85°C Temperature Range

Applications

- Cellular and Smart Phones
- Digital Cameras
- Handheld Instruments
- Mass Storage Systems
- Microprocessor / DSP Core / IO Power
- PDAs and Handheld Computers
- Portable Media Players
- USB Devices
- Wireless LAN

Typical Application

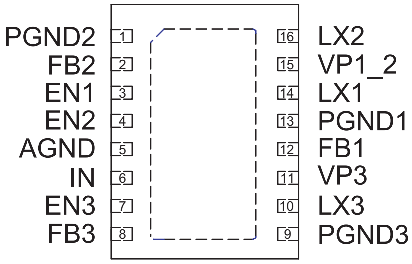


Pin Descriptions

Pin #	Symbol	Function
1	PGND2	Power ground return pin 2. Connect to the output and input capacitor return.
2	FB2	Feedback input pin for channel 2. Connect an external resistor divider to this pin to program the output voltage to the desired value.
3	EN1	Enable pin for channel 1. Active high.
4	EN2	Enable pin for channel 2. Active high.
5	AGND	Signal ground.
6	IN	Input supply pin for device. Supplies bias for the internal circuitry.
7	EN3	Enable pin for channel 3. Active high.
8	FB3	Feedback input pin for channel 3. Connect an external resistor divider to this pin to program the output voltage to the desired value.
9	PGND3	Power ground return pin 3. Connect to the output and input capacitor return.
10	LX3	Power switching node for channel 3. Output switching node connects to the output inductor.
11	VP3	Input power supply pin for channel 3. Must be closely decoupled.
12	FB1	Feedback input pin for channel 1. Connect an external resistor divider to this pin to program the output voltage to the desired value.
13	PGND1	Power ground return pin 1. Connect to the output and input capacitor return.
14	LX1	Power switching node for channel 1 and 2. Output switching node connects to the output inductor.
15	VP1_2	Input power supply pin for channels 1 and 2. Must be closely decoupled.
16	LX2	Power switching node for channel 2. Output switching node connects to the output inductor.
EP	EP	Exposed pad. Connect to ground directly under the device. Use properly sized vias for thermal coupling to the ground plane. See section on PCB layout guidelines.

Pin Configuration

TDFN34-16
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}, V_P	Input Voltages to AGND/PGND	6.0	V
V_{LX}	LX1, LX2, LX3 to AGND/PGND	-0.3 to V_{IN} + 0.3	V
V_{FB}	FB1, FB2, FB3 to AGND/PGND	-0.3 to V_{IN} + 0.3	V
V_{EN}	EN1, EN2, EN3 to AGND/PGND	-0.3 to 6.0	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information

Symbol	Description	Value	Units
P_D	Maximum Power Dissipation[2]	2.0	W
θ_{JA}	Thermal Resistance[3]	50	°C/W

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1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.
3. Derate 20mW/°C above 25°C ambient temperature.

Electrical Characteristics[1]

$V_{IN} = V_P = 3.6V$; T_A = -40°C to 85°C, unless noted otherwise. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage		2.7		5.5	V
V_{OUT}	Output Voltage Tolerance	I_{OUT3} = 0 to 1.5A; $I_{OUT1,2}$ = 0 to 600mA; V_{IN} = 2.7 to 5.5V	-3.0		3.0	%
V_{OUT}	Output Voltage Range		0.6		V_{IN}	V
$I_{Q1,2}$	Quiescent Current Channels 1, 2	Per Channel, No Load		50	100	μA
I_{Q3}	Quiescent Current Channel 3	No Load		45	90	μA
I_{SHDN}	Shutdown Current	$V_{EN1} = V_{EN2} = V_{EN3}$ = GND			1.0	μA
I_{LX_LEAK}	LX Reverse Leakage Current	V_{IN} Open, V_{LX} = 5.5V; V_{EN} = 0V			1.0	μA
I_{LX_LEAK}	LX Leakage Current	V_{IN} = 5.5V, V_{LX} = 0 to V_{IN}			1.0	μA
I_{FB}	Feedback Leakage	V_{FB} = 1.0V			0.2	μA
$I_{LIM1,2}$	P-Channel Current Limit			1.8		A
I_{LIM3}	P-Channel Current Limit			3.8		A
$R_{DS(ON)H1,2}$	High Side Switch On-Resistance			400		mΩ
$R_{DS(ON)L1,2}$	Low Side Switch On-Resistance			400		mΩ
$R_{DS(ON)H3}$	High Side Switch On-Resistance			150		mΩ
$R_{DS(ON)L3}$	Low Side Switch On-Resistance			120		mΩ
$\Delta V_{LOADREG}$	Load Regulation	$I_{LOAD1,2}$ = 0 to 600 mA; I_{LOAD3} = 0 to 1.5A		0.8		%
$\Delta V_{LINEREG}$	Line Regulation	V_{IN} = 2.7 to 5.5V		0.5		%
$F_{OSC1,2}$	Oscillator Frequency Channels 1,2			1.8		MHz
F_{OSC3}	Oscillator Frequency Channel 3			1.8		MHz
T_S	Start-Up Time	From Enable to Output Regulation		150		μs
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
V_{IL}	Enable Threshold Low				0.6	V
V_{IH}	Enable Threshold High		1.4			V
I_{EN}	Enable Input Current	$V_{IN} = V_{EN}$ = 5.5V	-1.0		1.0	μA

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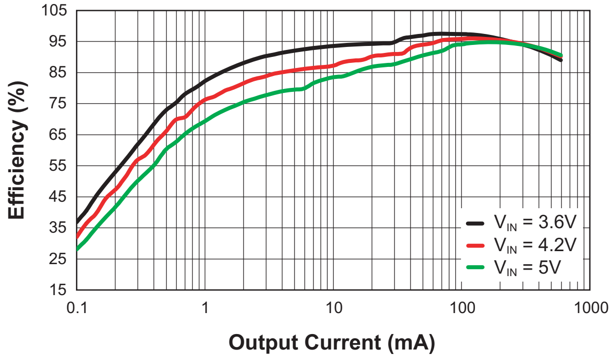
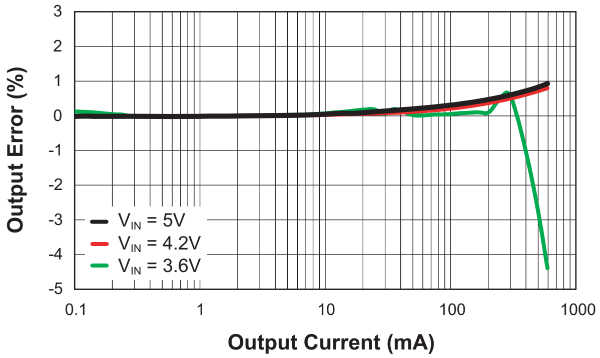
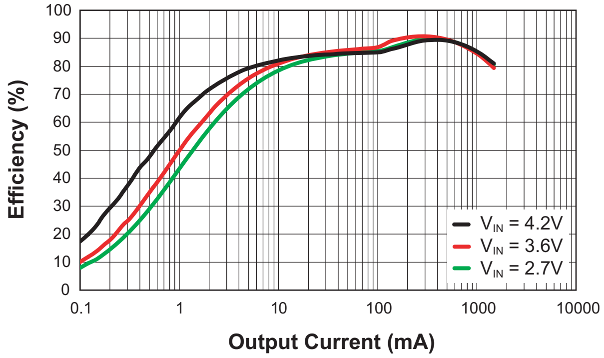
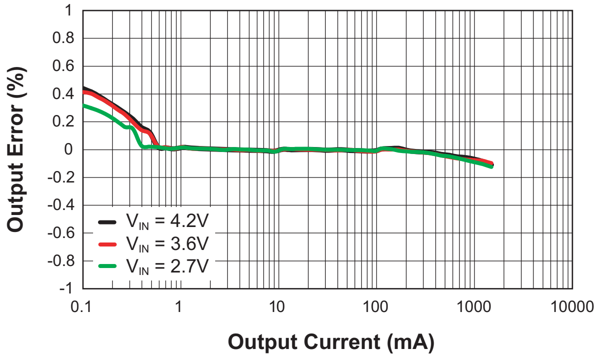
[1] The AAT2785 is guaranteed to meet performance specifications over the −40°C to +85°C operating temperature range, and is assured by design, characterization and correlation with statistical process controls.

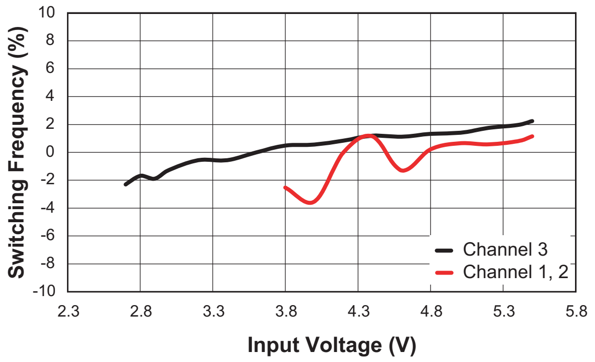
Typical Characteristics

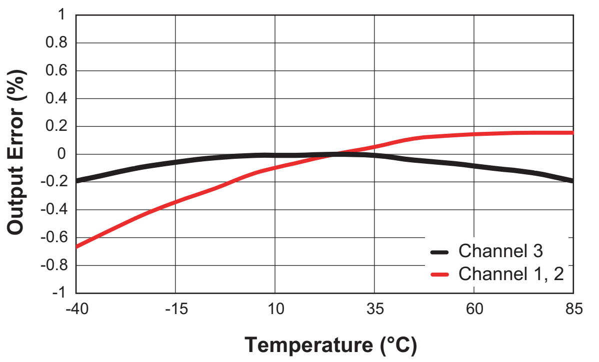

Efficiency vs. Output Current
(Channel 1, 2; V_{OUT} = 3.3V)


Load Regulation
(Channel 1, 2; V_{OUT} = 3.3V)


Efficiency vs. Output Current
(Channel 3; V_{OUT} = 1.2V)

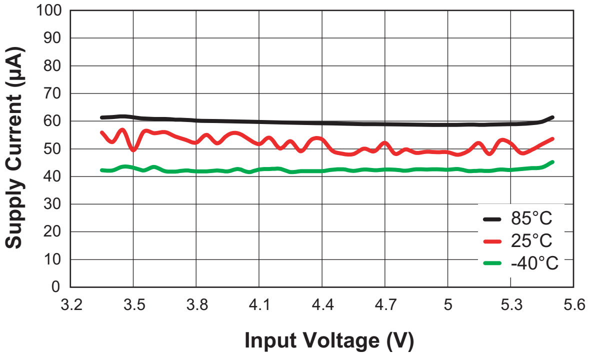

Load Regulation
(Channel 3; V_{OUT} = 1.2V)


Switching Frequency vs. Input Voltage

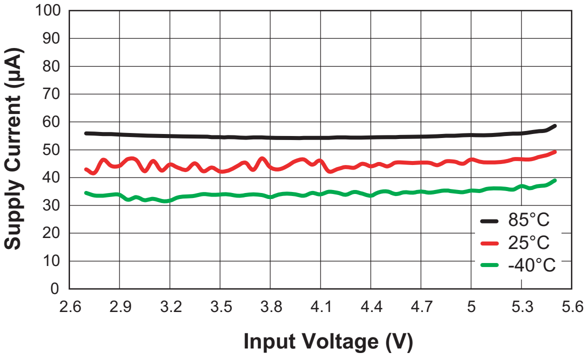

Output Error vs. Temperature

Typical Characteristics

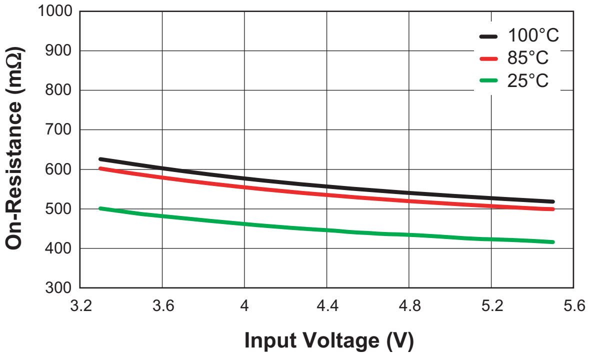
Quiescent Current vs. Input Voltage
(Channel 1, 2; V_{OUT} = 3.3V; No Load; Open Loop)



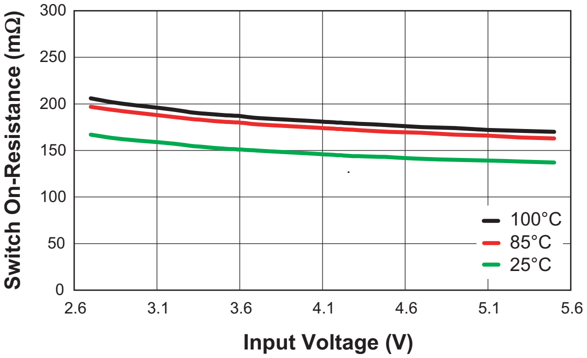
Quiescent Current vs. Input Voltage
(Channel 3; V_{OUT} = 1.2V; No Load; Open Loop)



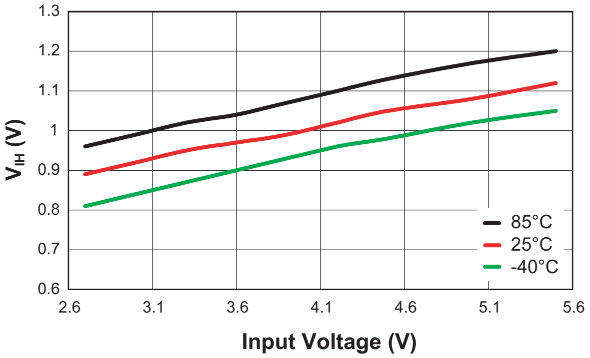
P-Channel On-Resistance vs. Input Voltage
(Channel 1, 2; V_{OUT} = 3.3V)



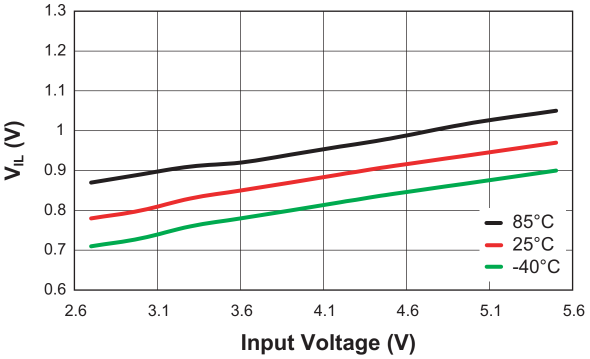
P-Channel On-Resistance vs. Input Voltage
(Channel 3; V_{OUT} = 1.2V)



V_{IH} vs. Input Voltage

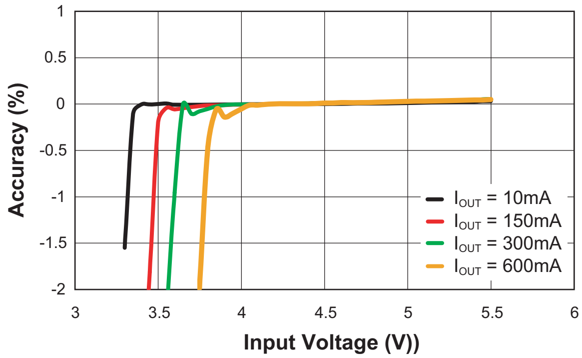


V_{IL} vs. Input Voltage

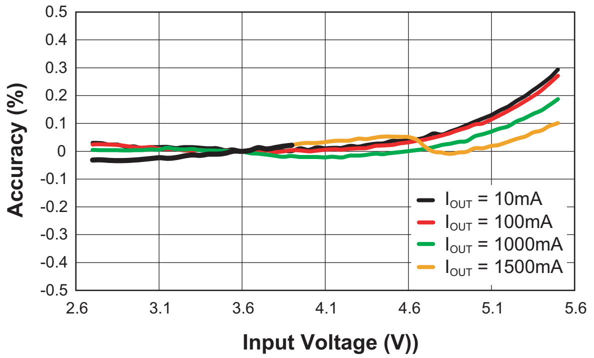


Typical Characteristics

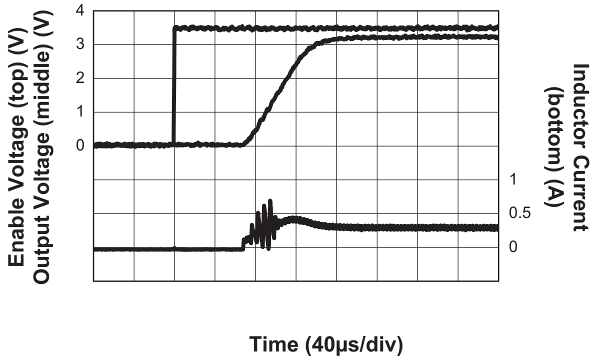
Line Regulation
(Channel 1, 2; V_{OUT} = 3.3V)



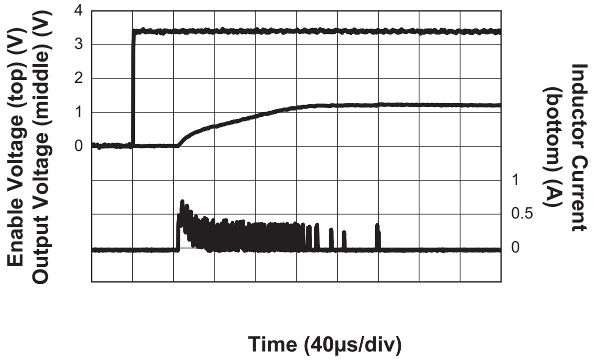
Line Regulation
(Channel 3; V_{OUT} = 1.2V)



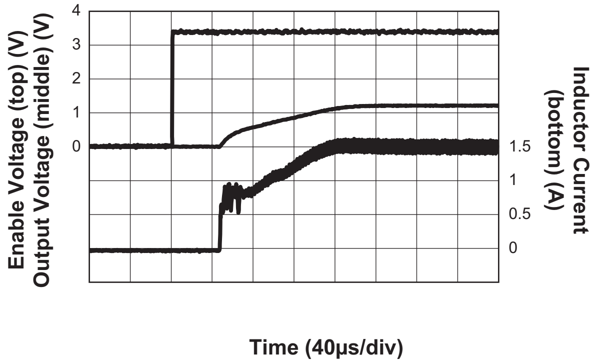
Soft Start
(Channel 1, 2; V_{IN} = 5V; V_{OUT} = 3.3V; I_{OUT} = 300mA)



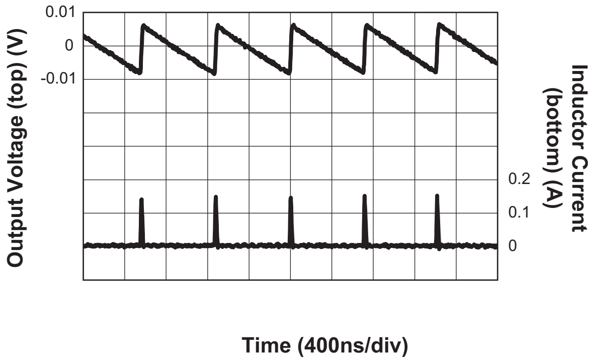
Soft Start
(Channel 3; V_{IN} = 5V; V_{OUT} = 1.2V; I_{OUT} = 1mA)



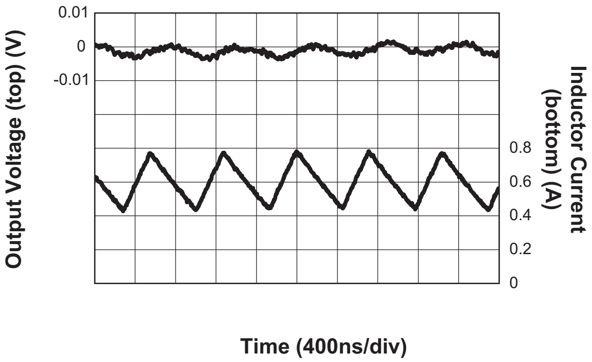
Soft Start
(Channel 3; V_{IN} = 5V; V_{OUT} = 1.2V; I_{OUT} = 1.5A)

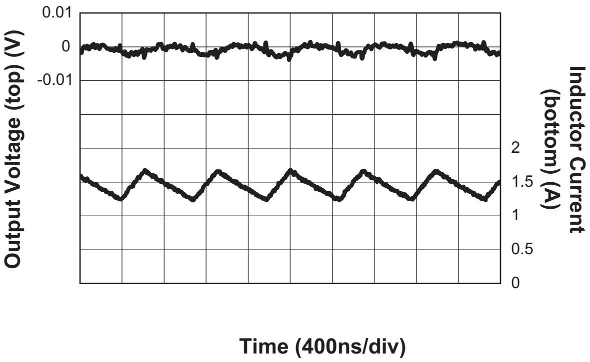


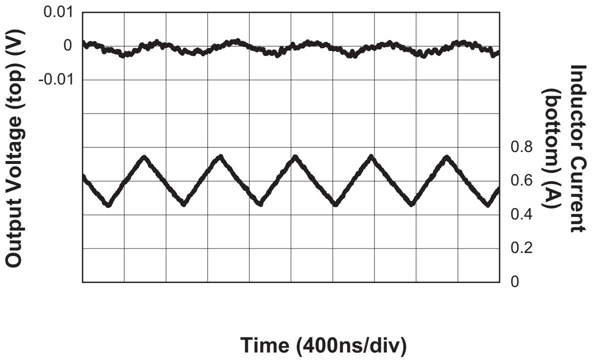
Output Ripple
(Channel 1, 2; V_{OUT} = 3.3V; V_{IN} = 4.6V; I_{OUT} = 1mA)

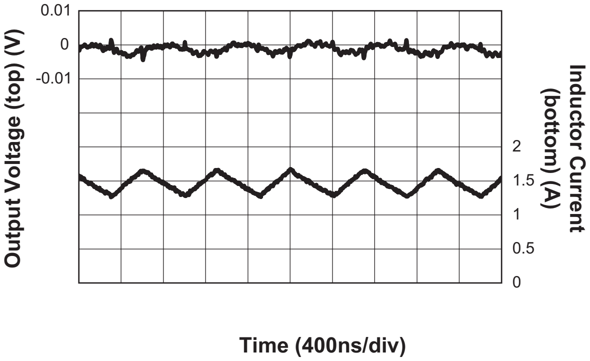


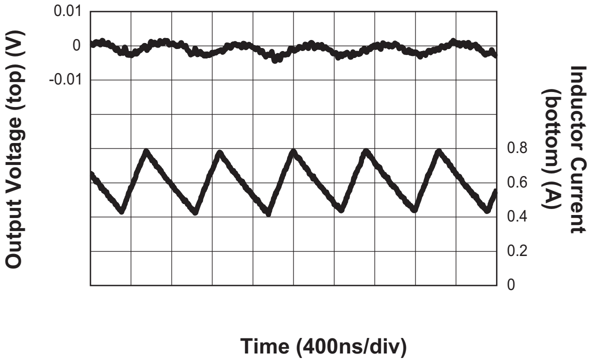
Typical Characteristics

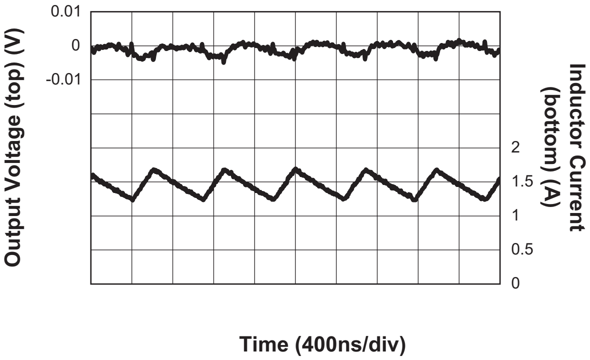

Output Ripple
(Channel 1, 2; V_{OUT} = 3.3V; V_{IN} = 4.6V; I_{OUT} = 600mA)


Output Ripple
(Channel 3; V_{OUT} = 1.2V; V_{IN} = 4.6V; I_{OUT} = 1.5A)


Output Ripple
(Channel 1, 2; V_{OUT} = 3.3V; V_{IN} = 3.6V; I_{OUT} = 600mA)

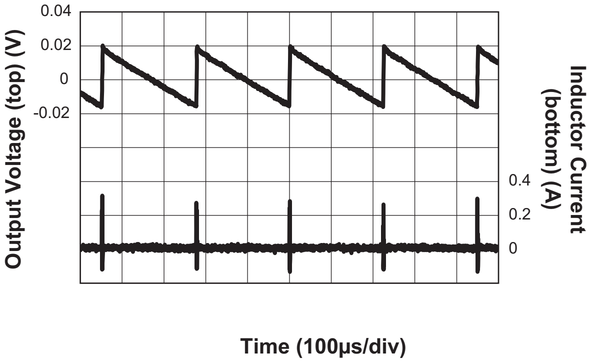

Output Ripple
(Channel 3; V_{OUT} = 1.2V; V_{IN} = 3.6V; I_{OUT} = 1.5A)


Output Ripple
(Channel 1, 2; V_{OUT} = 3.3V; V_{IN} = 5V; I_{OUT} = 600mA)

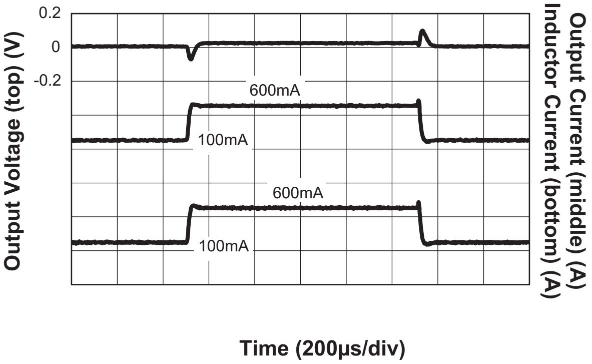

Output Ripple
(Channel 3; V_{OUT} = 1.2V; V_{IN} = 5V; I_{OUT} = 1.5A)

Typical Characteristics

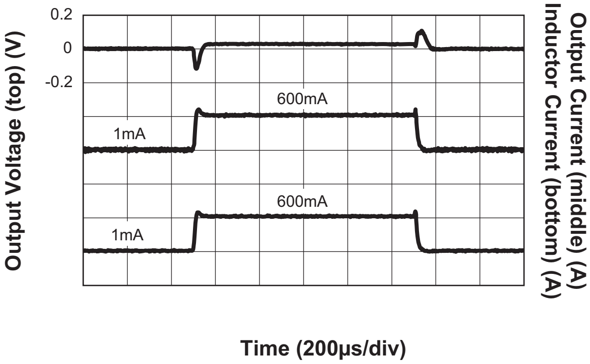
Output Ripple
(Channel 3; V_{OUT} = 1.2V; V_{IN} = 4.2V; I_{OUT} = 1mA)



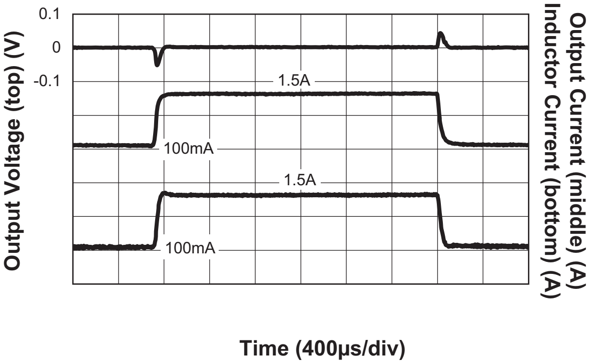
Load Transient
(Channel 1, 2; V_{IN} = 3.6V; I_{OUT} = 100mA to 600mA; V_{OUT} = 3.3V)



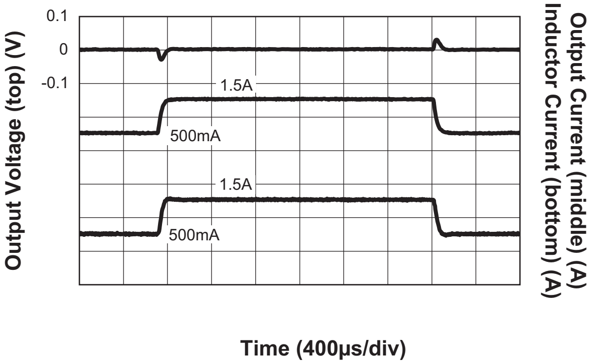
Load Transient
(Channel 1, 2; V_{IN} = 3.6V; I_{OUT} = 1mA to 600mA; V_{OUT} = 3.3V)



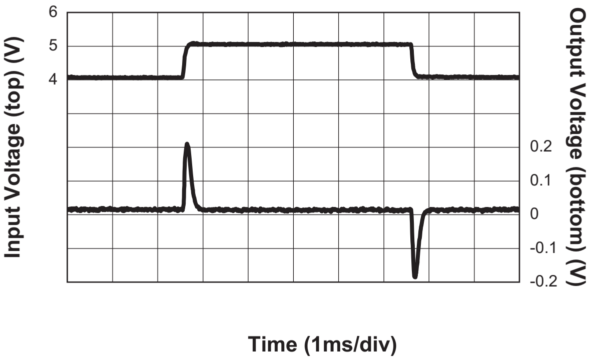
Load Transient
(Channel 3; V_{IN} = 5V; I_{OUT} = 0.1A to 1.5A; V_{OUT} = 1.2V)



Load Transient
(Channel 3; V_{IN} = 5V; I_{OUT} = 0.5A to 1.5A; V_{OUT} = 1.2V)

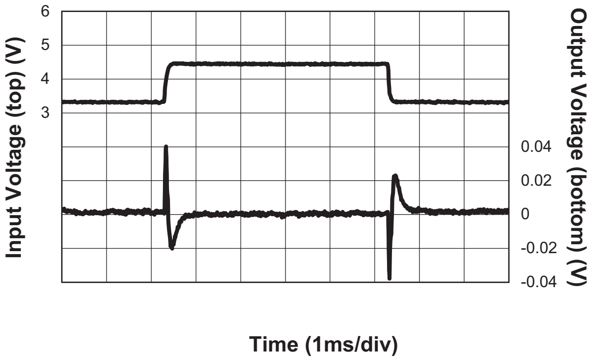


Line Transient
(Channel 1, 2; V_{IN} = 4V to 5V; I_{OUT} = 600mA; V_{OUT} = 3.3V)

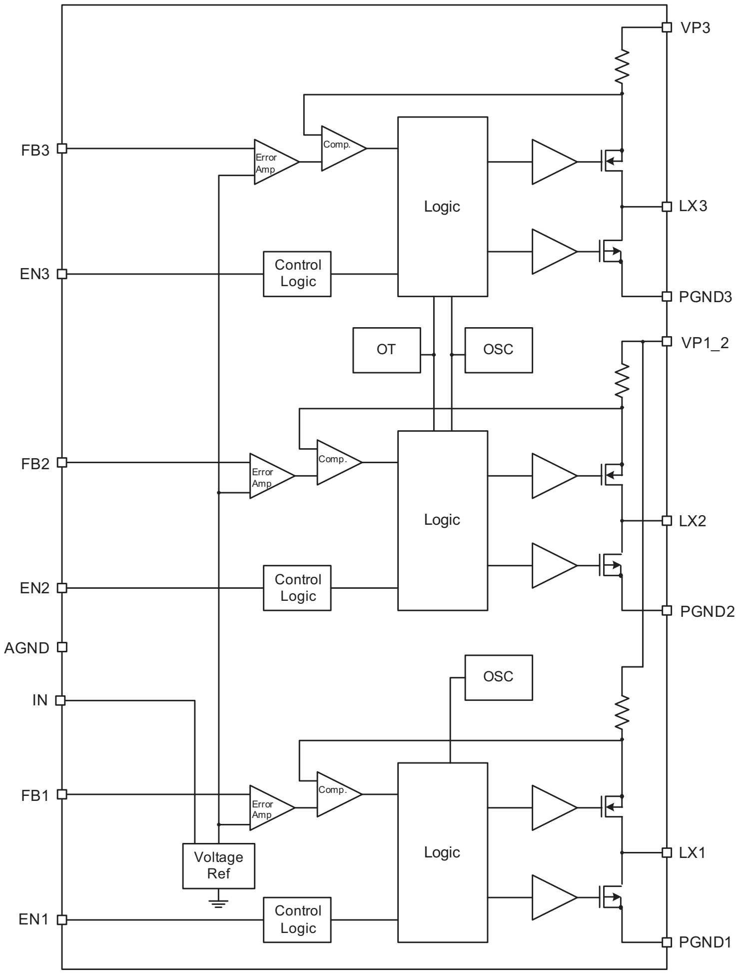


Typical Characteristics

Line Transient
(Channel 3; V_{IN} = 3.6V to 4.2V; I_{OUT} = 1.5A; V_{OUT} = 1.2V)



Functional Block Diagram



Functional Description

The AAT2785 is a high performance power management IC comprised of 3 buck converters. Each channel has an independent input voltage and enable pin. Operating at a switching frequency of 1.8MHz, the converter requires a minimum of small external components, reducing the solution cost and PCB footprint.

All converters operate with an input voltage range of 2.7V to 5.5V. The output voltage range is 0.6V to V_{IN} and is adjustable with an external resistor divider. Channel 3 power devices are sized for 1.5A output current. Channels 1 and 2 power devices are sized for 600mA output current while maintaining over 85% efficiency at full load. Peak efficiency is above 95%. Light load efficiency is maintained at greater than 80% down to 85% of full load current. All channels have excellent transient response, load and line regulation. Transient response time is typically less than 20µs.

Soft start limits the current surge seen at the input and eliminates output voltage overshoot. The enable inputs, when pulled low, force the respective converter into a low power non-switching state consuming less than 1µA of current.

For overload conditions, the peak input current is limited. Also, thermal protection completely disables switching if internal dissipation becomes excessive, thus protecting the device from damage. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuits prior to activation.

Control Loop

The AAT2785 is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short-circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor. The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. The reference voltage is internally set to program the converter output voltage greater than or equal to 0.6V.

Soft Start/Enable

Soft start limits the current surge seen at the input and eliminates output voltage overshoot. When pulled low, the enable input forces the AAT2785 into a low-power, non-switching state. The total input current during shutdown is less than 1μA.

Low Dropout Operation

For conditions where the input voltage drops to the output voltage level, the converter duty cycle increases to 100%. As the converter approaches the 100% duty cycle, the minimum off time initially forces the high side in time to exceed the 1.8MHz clock cycle and reduce the effective switching frequency. Once the input drops below the level where the converter can regulate the output, the high side P-channel MOSFET is enabled continuously for 100% duty cycle. At 100% duty cycle the output voltage tracks the input voltage minus the I*R drop of the high side P-channel MOSFET.

Current Limit and Over-Temperature Protection

For overload conditions, the peak input current is limited. To minimize power dissipation and stresses under current limit and short-circuit conditions, switching is terminated after entering current limit for a series of pulses. Switching is terminated for seven consecutive clock cycles after a current limit has been sensed for a series of four consecutive clock cycles. Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault condition is removed, the output voltage automatically recovers.

Under-Voltage Lockout

Internal bias of all circuits is controlled via the V_{IN} input. Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuitry prior to activation.

Component Selection

Inductor Selection: Channels 1 and 2

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The internal slope compensation for the adjustable and low voltage fixed versions of channels 1 and 2 is 0.6A/μs. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.8V output and 2.2μH inductor.

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.8V}{2.2\mu H} = 0.6\frac{A}{\mu s}$$

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot 3.3V}{0.6\frac{A}{\mu s}} = 4.1\mu H$$

In this case a standard 4.7μH value is selected. Table 1 displays the suggested inductor values for channels 1 and 2. The 4.7μH CDRH2D11 series inductor selected from Sumida has a 170mΩ DCR and a 0.88A DC current rating. At full load the inductor DC loss is 15mW which corresponds to a 1.5% loss in efficiency for a 600mA, 3.3V output.

Inductor Selection: Channel 3

The internal slope compensation for the adjustable and low voltage fixed versions of channel 3 is 0.75A/μs. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.8V output and 1.8μH inductor.

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.8V}{1.8\mu H} = 0.75\frac{A}{\mu s}$$

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot 1.2V}{0.75\frac{A}{\mu s}} = 1.2\mu H$$

The inductor should be set equal to the output voltage numeric value in micro henries (µH). This guarantees that there is sufficient internal slope compensation. Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor. For channel 3, the 1.5µH LQH32PN1R5NN0L series Murata inductor has a 68.4mΩ worst case DCR and a 1.75A DC current rating. At full 1.5A load, the inductor DC loss is 154mW which gives less than 5% loss in efficiency for a 1.5A, 1.2V output.

Input Capacitor

Select a 10µF to 22µF X7R or X5R ceramic capacitor for the VP1_2 and VP3 inputs. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C_{IN}. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

Configuration	Output Voltage	Inductor	Slope Compensation
0.6V adjustable with external resistive divider	0.6V-2.0V	2.2µH	0.6A/µs
	2.5V	3.3µH	
	3.3V	4.7µH	

Table 1: AAT2785 Inductor Values.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF. The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is at a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle. The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2785. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple. The proper placement of the input capacitor (C1) can be seen in the evaluation board layout in the Layout section of this datasheet (see Figure 2). A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result. Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem. In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR/ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Output Capacitor: Channels 1 and 2

The output capacitor limits the output ripple and provides holdup during large load transitions. A 4.7μF to 10μF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple. The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients. The internal voltage loop compensation also limits the minimum output capacitor value to 4.7μF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

Output Capacitor: Channel 3

The output capacitor limits the output ripple and provides holdup during large load transitions. A 10μF to 22μF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

Adjustable Output Resistor Selection

The output voltage for each channel of the AAT2785 is programmed with external resistors R1, R2, R3, R4, R5, and R6. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2 and R4 are 29.4 kΩ, and R6 is 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 2 and Table 3 summarize the resistor values for various output voltages of channel 1, channel 2, and channel 3.

V_{OUT} (V)	R2 = R4 = 29.4kΩ R1 = R3 (kΩ)
0.8	10
0.9	15
1.0	20
1.1	25
1.2	29
1.3	34
1.4	39
1.5	44
1.8	59
1.9	61
2.0	69
2.5	93
3.0	118
3.3	132

Table 2: AAT2785 Resistor Values for Various Output Voltages of Channel 1 and Channel 2.

V_{OUT} (V)	R6 = 59kΩ R5 (kΩ)	R6 = 221kΩ R5 (kΩ)
0.8	19.6	75
0.9	29.4	113
1.0	39.2	150
1.1	49.9	187
1.2	59.0	221
1.3	68.1	261
1.4	78.7	301
1.5	88.7	332
1.8	118	442
1.85	124	464
2.0	137	523
2.5	187	715
3.0	237	887
3.3	267	1000

Table 3: AAT2785 Resistor Values for Various Output Voltages of Channel 3.

Thermal Calculations

There are three types of losses associated with the AAT2785 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the losses is given by:

$$P_{TOTAL} = \frac{I_O^2 \cdot (R_{DS(ON)H} \cdot V_O + R_{DS(ON)L} \cdot [V_{IN} - V_O])}{V_{IN}}$$

$$+ (t_{sw} \cdot F_S \cdot I_O + I_Q) \cdot V_{IN}$$

I_Q is the step-down converter quiescent current. The term t_{SW} is used to estimate the full load step-down converter switching losses. For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_O^2 \cdot R_{DSON(H)} + I_Q \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range. Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the TDFN34-16 package, which is 50°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

Layout

The suggested PCB layout for the AAT2785 is shown in Figures 2 and 3. The following guidelines should be used to help ensure a proper layout.

1. The power input capacitors (C5 and C8) should be connected as closely as possible to VP1_2, VP3 and PGND1,2,3 as shown in Figure 2. Due to the pin placement of VP1_2 and VP3 for all converters, proper decoupling is not possible with just one input capacitor.
2. C1 and R7 are optional low pass filter components for the IN supply pin for the device if additional noise decupling is required in a noisy system
3. C2 and L1, C6 and L2, C10 and L3 should be connected as closely as possible. The connection of L1, 2, 3 to the LX1, 2, 3 pin should be as short as possible.
4. The feedback trace or FB pin should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
5. The resistance of the trace from the load returns to PGND1, 2 and 3 should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
6. Connect unused signal pins to ground to avoid unwanted noise coupling.
7. For good thermal coupling, PCB vias are required from the pad for the TDFN paddle to the bottom ground plane. The via diameter should be 0.3mm to 0.33mm and positioned on a 1.2mm grid.

Evaluation Board Schematic

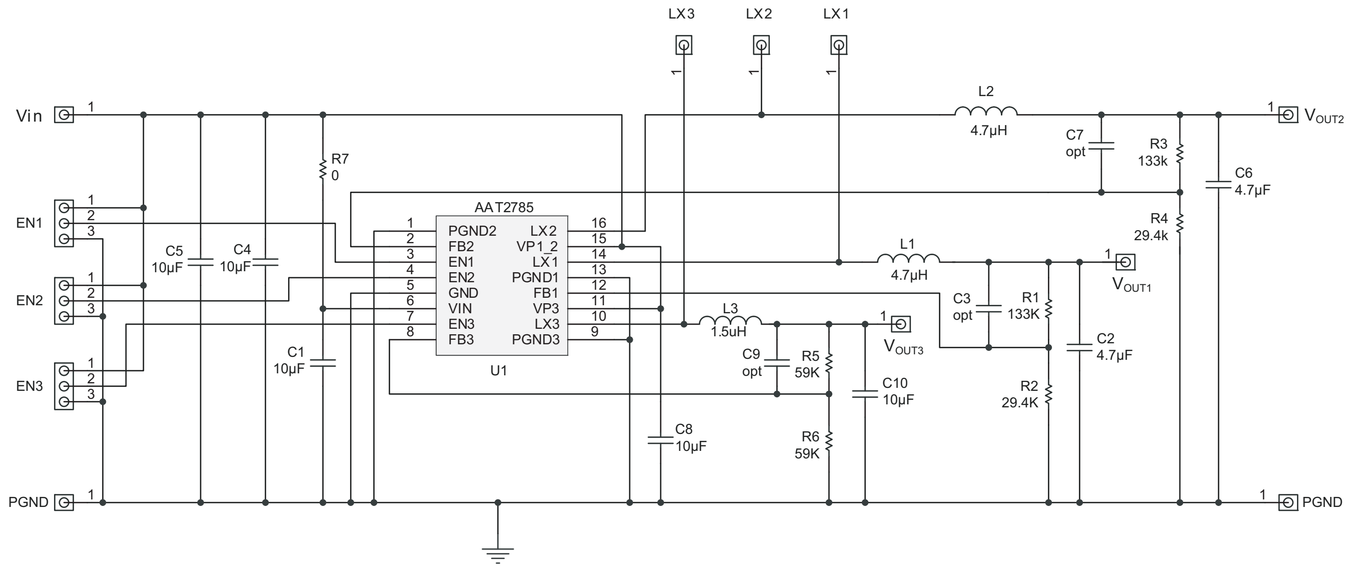


Figure 1: AAT2785 Evaluation Board Schematic.

Evaluation Board Layout

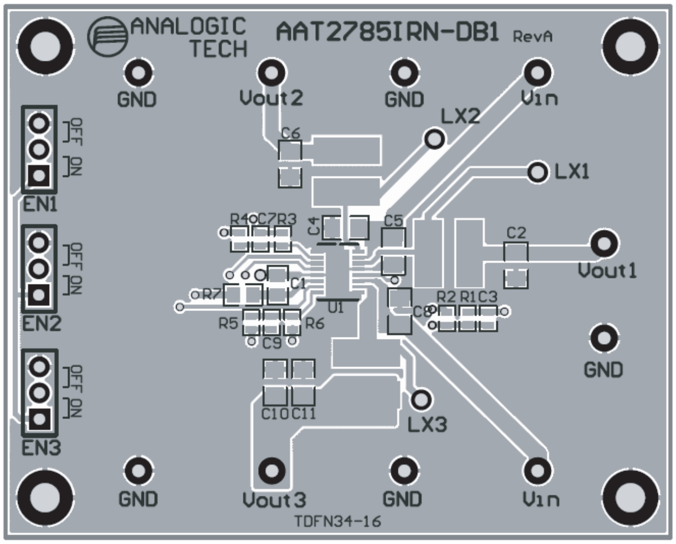


Figure 2: AAT2785 Evaluation Board Component Side Layout.

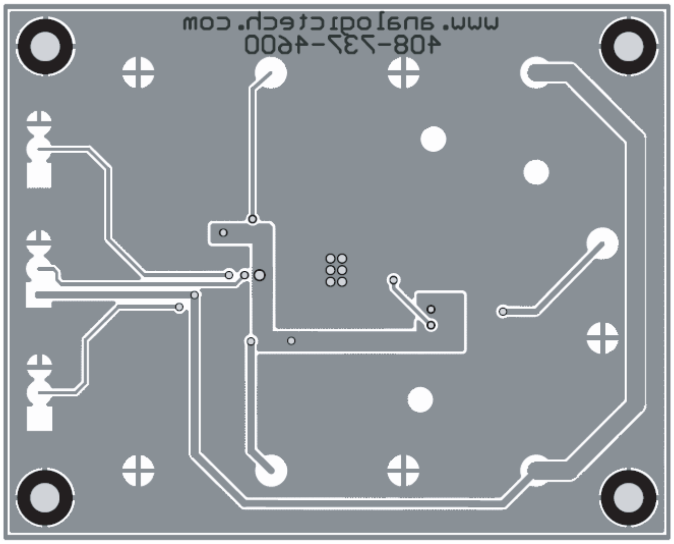


Figure 3: AAT2785 Evaluation Board Solder Side Layout.

Component	Part Number	Manufacturer	Description
U1	AAT2785	AATI	3-Channel Step-Down DC/DC Converter
L1, L2	CDRX2D11	Sumida	4.7μH 0.88A 170mΩ (3.2x3.2x1.2)mm Shielded
L3	LQH32PN1R5NN0L	Murata	1.5μH series Murata inductor has a 68.4mΩ worst case DCR and a 1.75A DC
C1		Generic	Optional
C2, C6	GMR219R61A475KE19	Murata	4.7μF 10V 0805
C5, C8, C10	GMR21BR60J106KE19	Murata	10μF 6.3V 0805
C9		Generic	56pF 6.3V 0402
R1, R3		Generic	133KΩ 0402
R2, R4		Generic	29.4KΩ 0402
R5, R6		Generic	59KΩ 0402
R7		Generic	Optional

Table 4: AAT2785 Evaluation Board Bill of Materials.

Design Example

Specifications

V_{O3}	1.2V @ 1.5A (adjustable using 0.6V version), pulsed load ΔI_{LOAD} = 1.5A
V_{O1}	3.3V @ 600mA (adjustable using 0.6V version), pulsed load ΔI_{LOAD} = 600mA
V_{O2}	3.3V @ 600mA (adjustable using 0.6V version), pulsed load ΔI_{LOAD} = 600mA
V_{IN}	2.7V to 4.2V (3.6V nominal)
F_S	1.8MHz
T_{AMB}	85°C

Channel 3 Output Inductor

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot 1.2V}{0.75\,\frac{A}{\mu s}} = 1.2\mu H\text{; use 1.5μH. (see Table 4).}$$

Select Murata LQH32PN1R5NN0L 1.5μH 1.75A DC current rating DCR = 68mΩ.

$$\Delta I_3 = \frac{V_{O3}}{L \cdot F}\left(1 - \frac{V_{O3}}{V_{IN}}\right) = \frac{1.5V}{1.5\mu H \cdot 1.8MHz} \cdot \left(1 - \frac{1.5V}{4.2V}\right) = 357mA$$

$$I_{PK3} = 1.5A + 0.357A = 1.9A$$

$$P_{L3} = I_{O3}^2 \cdot DCR = 1.5A^2 \cdot 68m\Omega = 153mW$$

Channels 1 and 2 Output Inductors

$$L1 = L2 = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot 3.3V}{0.6\,\frac{A}{\mu s}} = 4.1\mu H\text{; use 4.7μH. (see Table 4)}$$

Select Sumida CDRH2D11 4.7μH 0.88A DC current rating DCR = 170mΩ.

$$\Delta I_1 = \Delta I_2 = \frac{V_{O1}}{L \cdot F}\left(1 - \frac{V_{O1}}{V_{IN}}\right) = \frac{3.3V}{4.7\mu H \cdot 1.8MHz} \cdot \left(1 - \frac{3.3V}{4.2V}\right) = 84mA$$

$$I_{PK1} = I_{PK2} = 0.6A + 0.084A = 0.7A$$

$$P_{L1} = P_{L2} = I_{O1}^2 \cdot DCR = 0.6^2 \cdot 170m\Omega = 61.2mW$$

Channel 3 Output Capacitor

$$C_{OUT3} = \frac{3 \cdot \Delta I_{LOAD1}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 1.5A}{0.2V \cdot 1.8MHz} = 12.5\mu F\text{; use 10 to 22}\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{1.2V \cdot (4.2V - 1.2V)}{1.5\mu H \cdot 1.8MHz \cdot 4.2V} = 92mA$$

$$P_{ESR} = ESR \cdot I_{RMS}{}^2 = 5m\Omega \cdot 92mA^2 = 0.04mW$$

Channels 1 and 2 Output Capacitors

$$C_{OUT1} = C_{OUT2} = \frac{3 \cdot \Delta I_{LOAD1}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 0.6A}{0.2V \cdot 1.8MHz} = 5\mu F\text{; use }5.6\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT1} \cdot (V_{IN(MAX)} - V_{OUT1})}{L \cdot F_S \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{3.3V \cdot (4.2V - 3.3V)}{4.7\mu H \cdot 1.8MHz \cdot 4.2V} = 24mA$$

$$P_{ESR} = ESR \cdot I_{RMS}{}^2 = 5m\Omega \cdot 28.9mA^2 = 2.9\mu W$$

Channel 3 Input Capacitor

Input Ripple V_{PP} = 30mV

$$C_{IN3} = \frac{1}{\left(\frac{V_{PP}}{I_{O3}} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{30mV}{1.5A} - 5m\Omega\right) \cdot 4 \cdot 1.8MHz} = 9.3\mu F\text{; use }10\mu F$$

$$I_{RMS(MAX)} = \frac{I_O}{2} = 0.75A$$

$$P_{ESR} = ESR \cdot I_{RMS}{}^2 = 5m\Omega \cdot (0.75A)^2 = 3mW$$

Channels 1 and 2 Input Capacitors

Input Ripple V_{PP} = 15mV

$$C_{IN1} = C_{IN2} = \frac{1}{\left(\frac{V_{PP}}{I_{O1}} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{15mV}{0.6A} - 5m\Omega\right) \cdot 4 \cdot 1.8MHz} = 7\mu F\text{; use }10\mu F$$

$$I_{RMS(MAX)} = \frac{I_O}{2} = 0.3A$$

$$P_{ESR} = ESR \cdot I_{RMS}{}^2 = 5m\Omega \cdot (0.3A)^2 = 0.45mW$$

AAT2785 Losses

Total loss can be estimated by calculating the dropout ($V_{IN} = V_O$) losses where the power MOSFETs' $R_{DS(ON)}$ will be at the maximum value. All values assume an 85°C ambient temperature and a 120°C junction temperature with the TDFN 50°C/W package.

$$P_{LOSS} = I_{O3}2 \cdot R_{DS(ON)H3} + 2 \cdot (I_{O1}2 \cdot R_{DS(ON)H1,2}) = 1.5A^2 \cdot 120m\Omega + 2 \cdot (0.6A^2 \cdot 400m\Omega) = 0.558W$$

$$T_{J(MAX)} = T_{AMB} + \theta_{JA} \cdot P_{LOSS} = 85°C + 50°C \cdot 0.558W = 113°C.$$

Manufacturer	Part Number	Inductance (µH)	Max DC Current (A)	DCR (Ω)	Size (mm) LxWxH	Type
Sumida	CDRH2D11	1.5	1.48	0.068	3.2x3.2x1.2	Shielded
Sumida	CDRH2D11	2.2	1.27	0.098	3.2x3.2x1.2	Shielded
Sumida	CDRH2D11	3.3	1.02	0.123	3.2x3.2x1.2	Shielded
Sumida	CDRH2D11	4.7	0.88	0.170	3.2x3.2x1.2	Shielded
Taiyo Yuden	CBC2518T	1.0	1.2	0.08	2.5x1.8x1.8	Wire Wound Chip
Taiyo Yuden	CBC2518T	2.2	1.1	0.13	2.5x1.8x1.8	Wire Wound Chip
Taiyo Yuden	CBC2518T	4.7	0.92	0.2	2.5x1.8x1.8	Wire Wound Chip
Taiyo Yuden	CBC2016T	2.2	0.83	0.2	2.0x1.6x1.6	Wire Wound Chip

Table 5: Typical Surface Mount Inductors.

Ordering Information

Package	Voltage			Marking[1]	Part Number (Tape and Reel)[2]
	Channel 1	Channel 2	Channel 3		
TDFN34-16	0.6	0.6	0.6	2NXYY	AAT2785IRN-AAA-T1

Pb-free

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/about/quality.aspx.

Legend	
Voltage	Code
Adjustable (0.6V)	A

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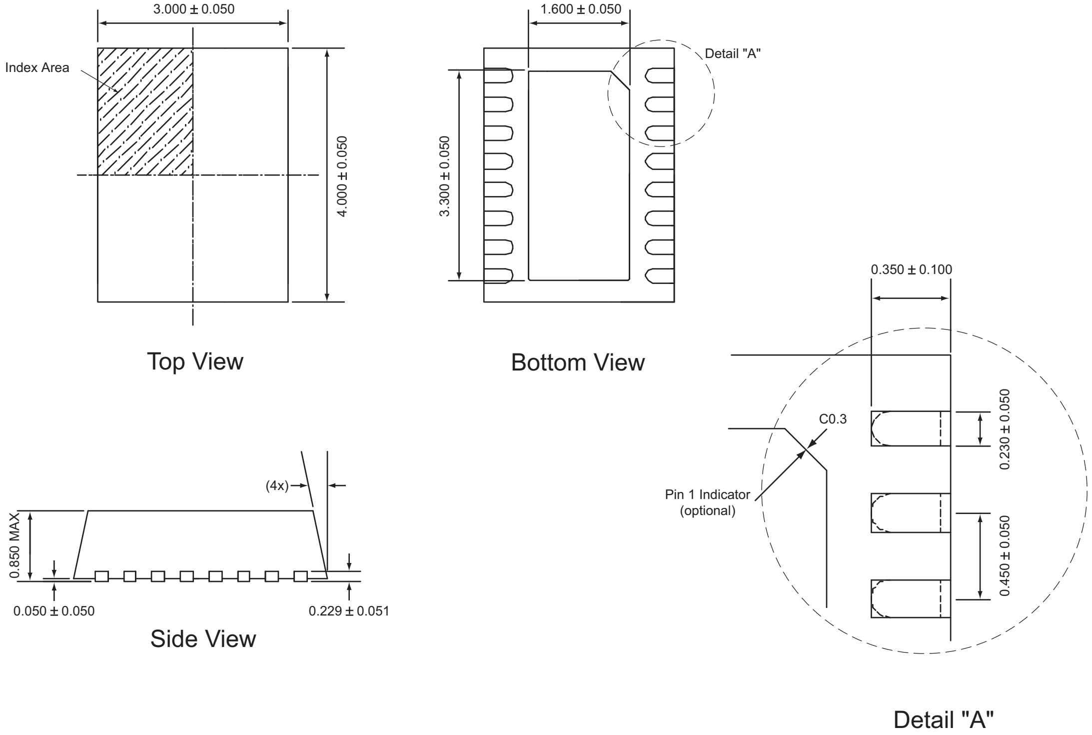
1. XYY = assembly and date code.
2. Sample stock is generally held on all part numbers listed in **BOLD**.

Package Information

TDFN34-16



Top View

Bottom View

Side View

Detail "A"

All dimensions in millimeters.

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1. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

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