

# 7-20GHz Medium Power Amplifier *preliminary*

## GaAs Monolithic Microwave IC in SMD package

### Description

The CHA3667aQDG is a wide band monolithic medium power amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The circuit is manufactured with a Power-HEMT process, 0.15 $\mu$ m gate length, via hole through the substrate.

It is ESD protected on RF ports thanks to DC specific filter circuits.

It is available in lead-free SMD package.

### Main Features

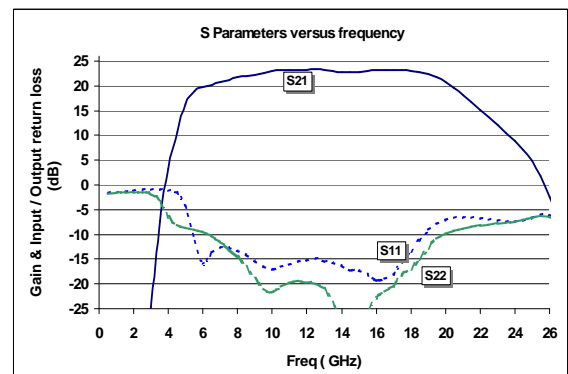
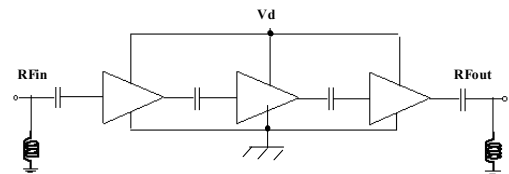
- Broadband performance 7-20GHz
- Self-biased
- 23dB gain @2.7dB noise figure
- 20dBm Output power@1dB compression
- DC power consumption, 175 mA @4.2V
- 24L-QFN4X4 SMD package
- ESD protected

### Main Characteristics

Tamb. = 25°C, Vd = 4.2V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Input frequency range	7		20	GHz
G	Small signal gain		23		dB
NF	Noise Figure		2.7		dB
P-1dB	Output power at 1dB gain compression		20		dBm
Id	Bias current		175		mA

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions



## Electrical Characteristics

Tamb. = 25°C, Vd = 4.2V

*preliminary*

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	7		20	GHz
G	Gain				dB
	(7-8GHz)		20		
	(8-19GHz)		23		
	(19-20GHz)		20		
NF	Noise figure (7-18 GHz)		2.7		dB
RLin	Input Return Loss		-10(1)		dB
RLout	Output Return Loss		-10		dB
IP3	Output IP3		28		dBm
P-1dB	Pout at 1dB gain compression:				
	( 7-13 GHz)		20		dBm
	(13-20 GHz)		21		dBm
Isol	Reverse isolation		40		dB
Vd	Drain bias voltage		4.2		V
Id	Drain bias current		175		mA

(1) Rlin<-6dB from 19.5GHz to 20 GHz

**Absolute Maximum Ratings (1)***preliminary*

Tamb = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5V	V
Id	Power supply quiescent current	240	mA
Pin	RF input power (2)	3	dBm
Top	Operating temperature range	-40 to +85	°C
Tj	Junction temperature (3)	175	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

(2) Duration<1s

(3) Thermal Resistance channel to ground paddle =101.1°C/W for Tamb. = +85°C Vd=4.2V & id=175mA

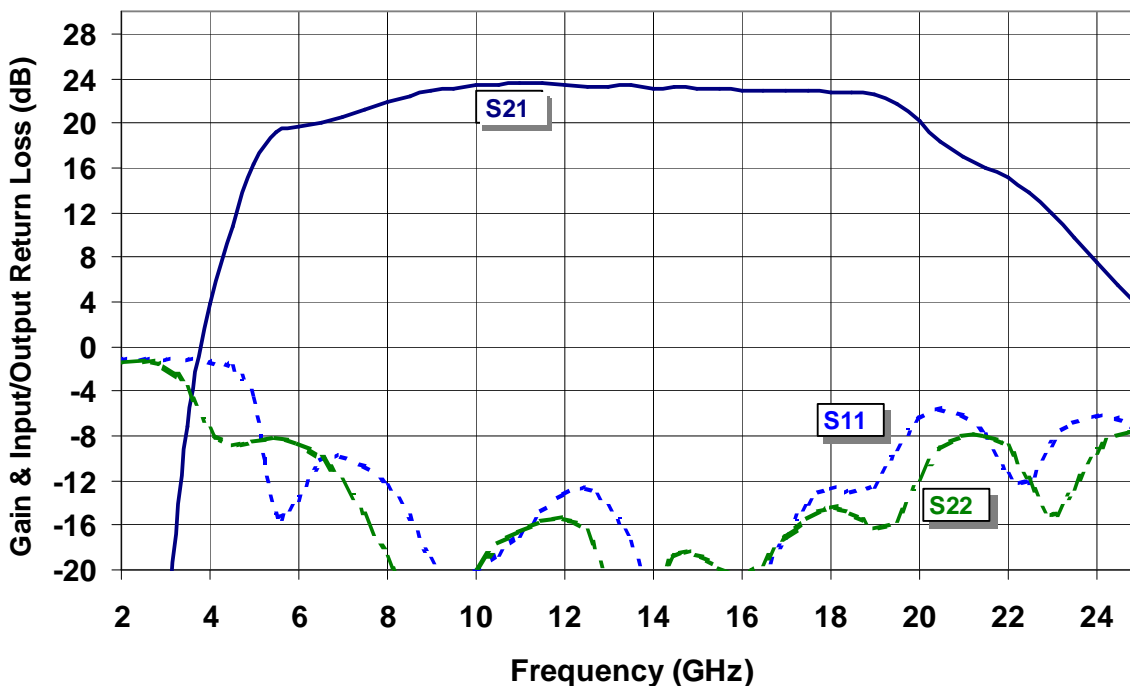
## Typical Measured Performance:

Tamb = +25°C, Vd= +4.2V Id = 175mA

*preliminary*

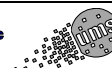
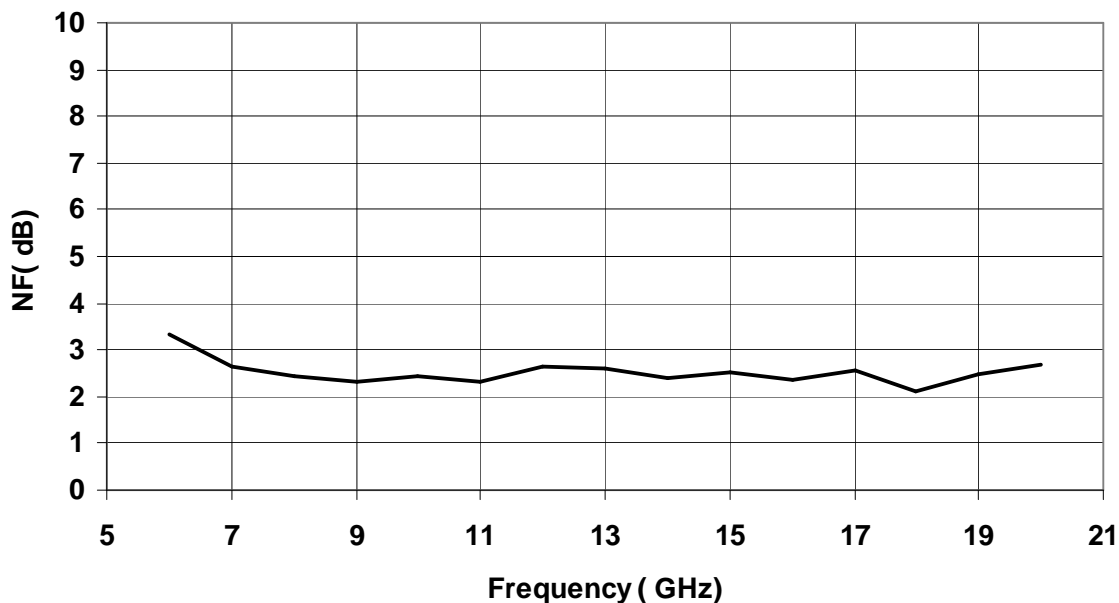
### S parameters versus Frequency

Measurements in the the plan of the connectors , using the proposed land pattern & board 96270\_B .



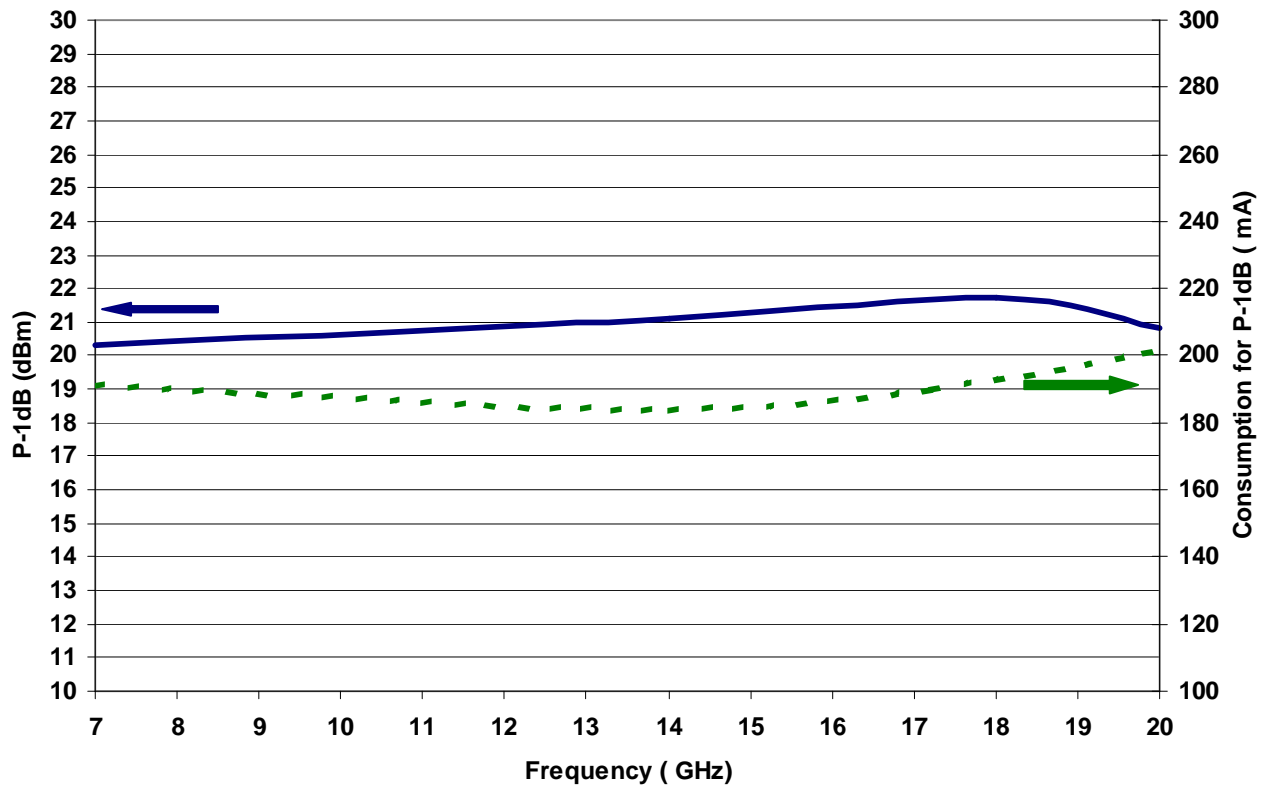
### Noise Figure versus Frequency

Result in the package access planes

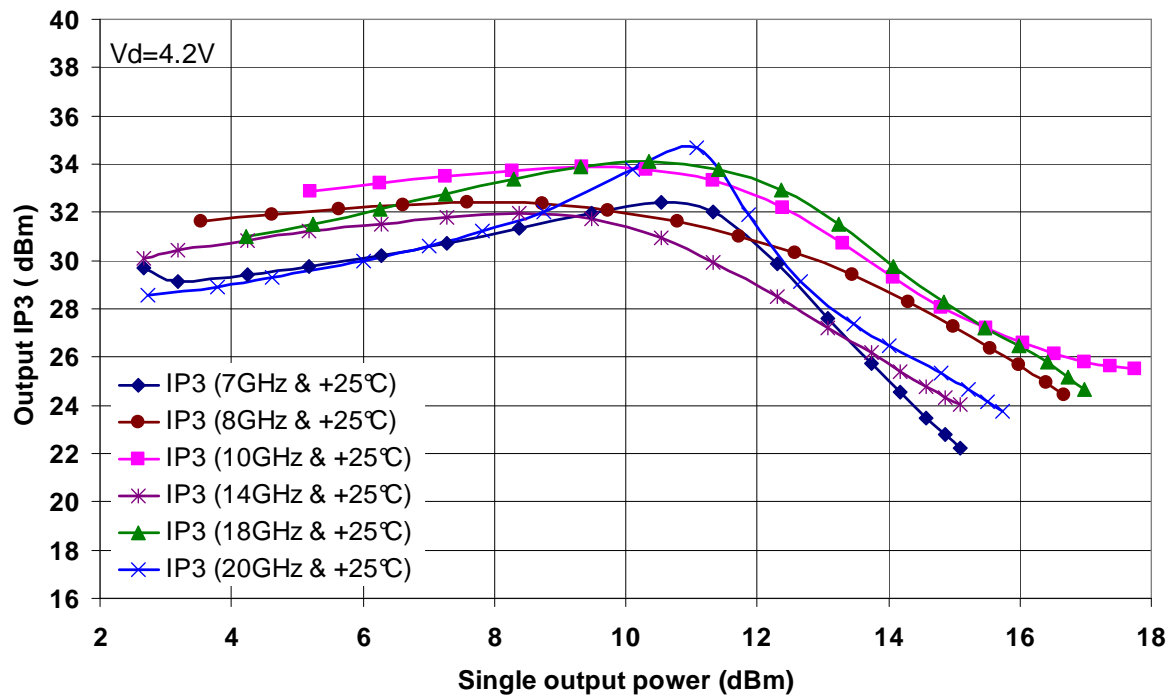


*preliminary*

**Output Power & associated Consumption Id @ 1dB compression**



**Output IP3 versus Single Output Power**

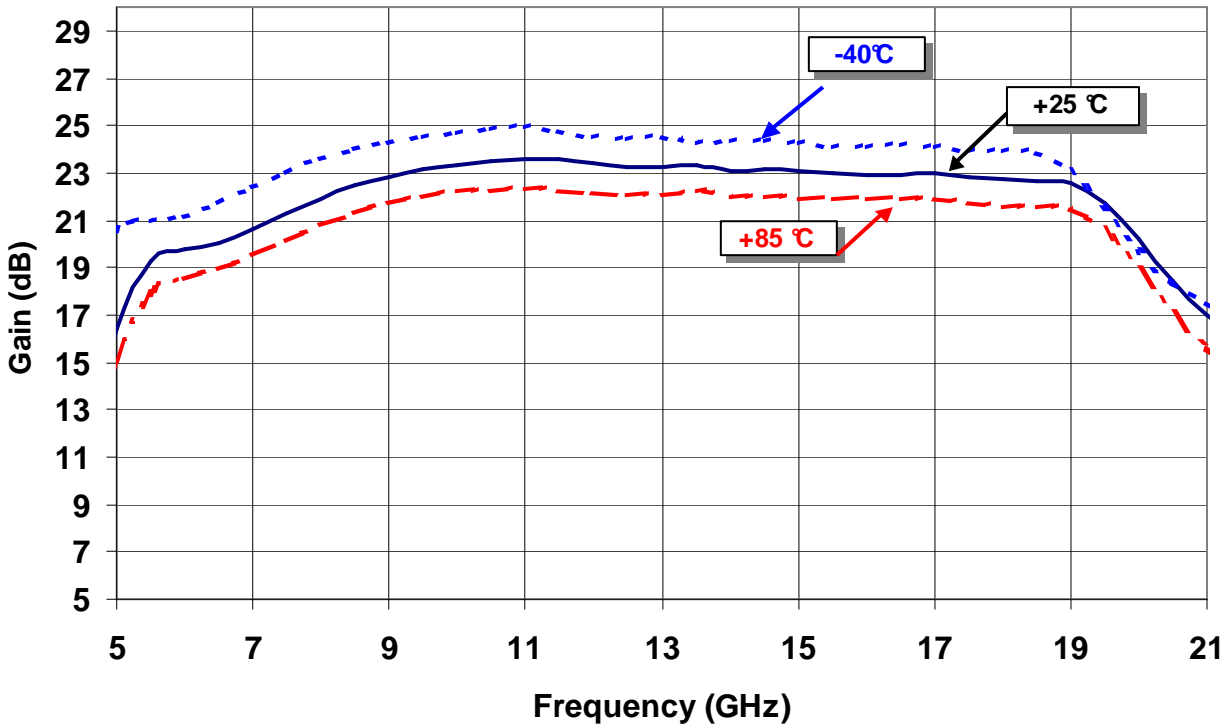


## Typical Measured Performance in temperature: ( -40°C to 85°C)

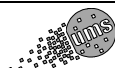
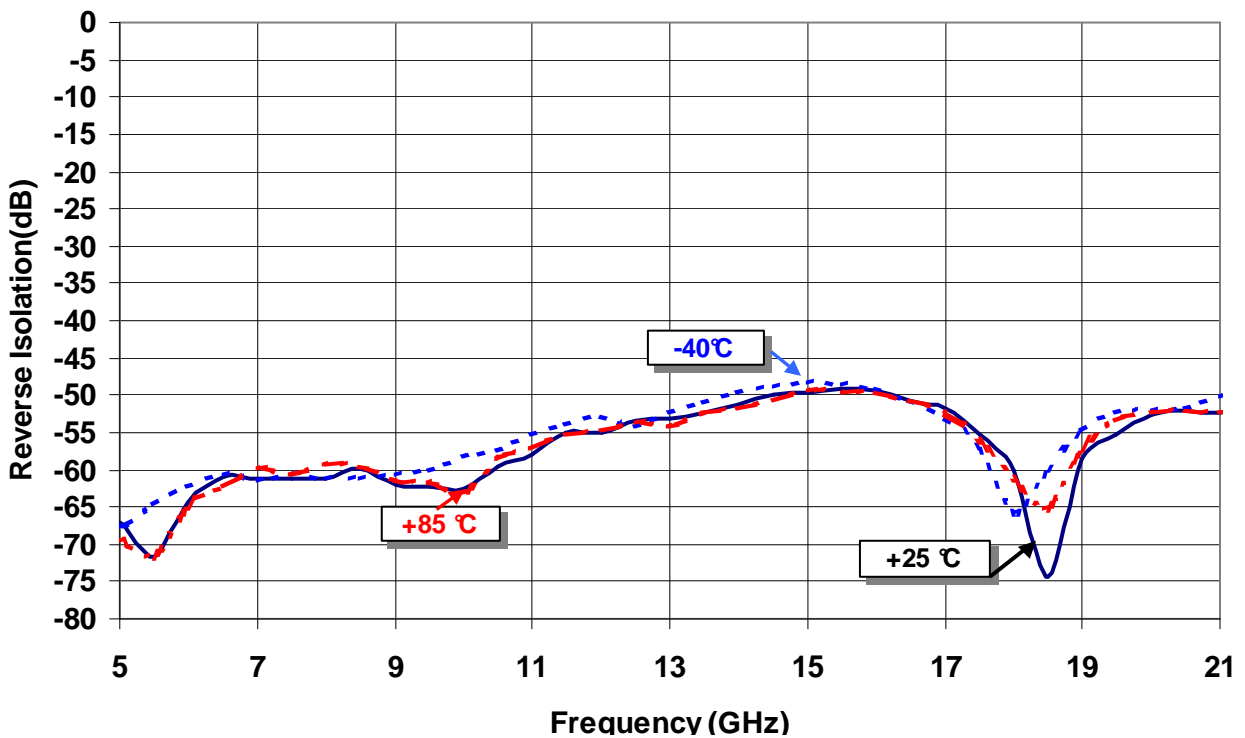
*preliminary*

Measurements in the the plan of the connectors , using the proposed land pattern & board 96270\_B .

*Linear Gain versus Frequency and Temperature*

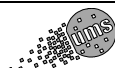
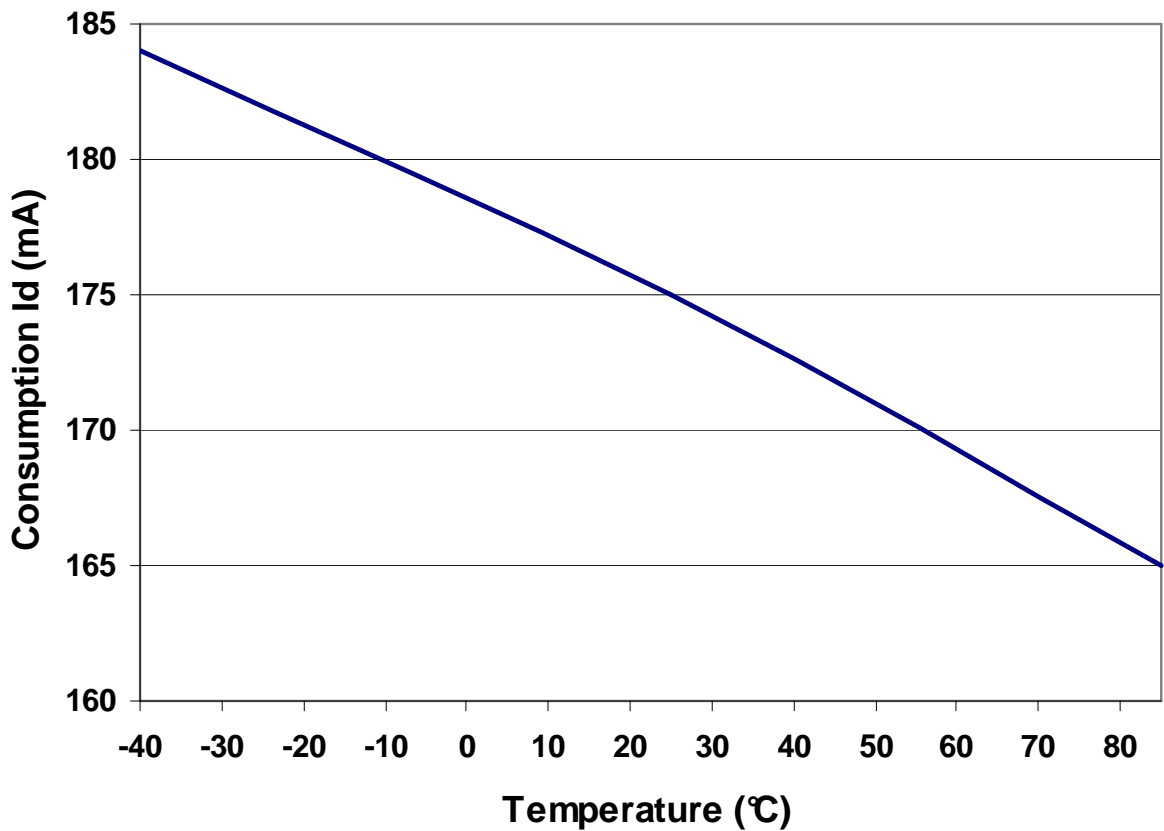
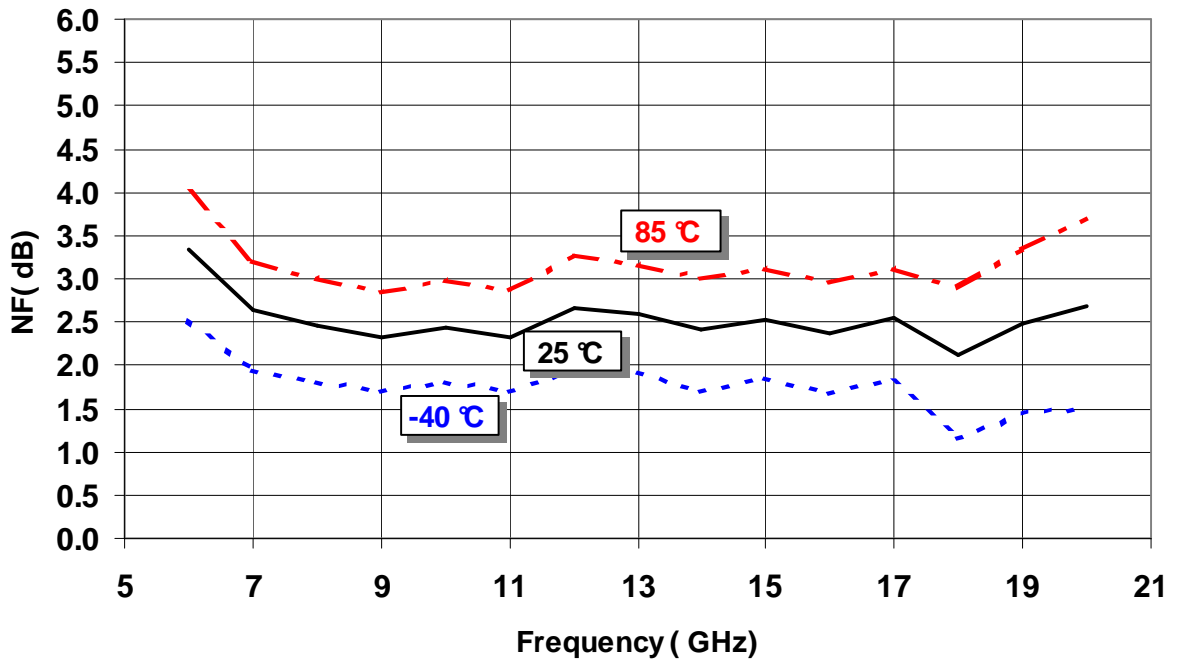


*Reverse isolation versus Frequency and Temperature*



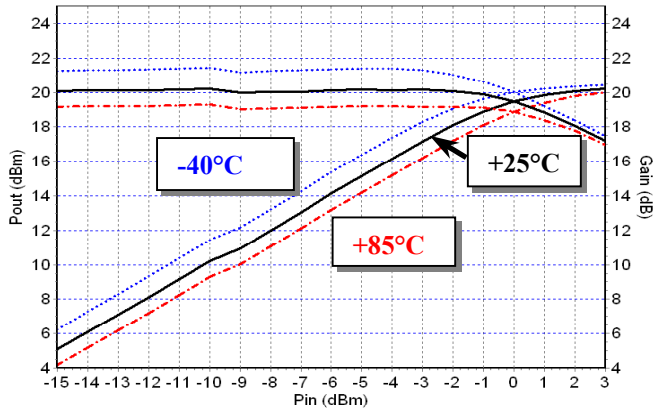
*preliminary*

Noise Figure versus Frequency and Temperature

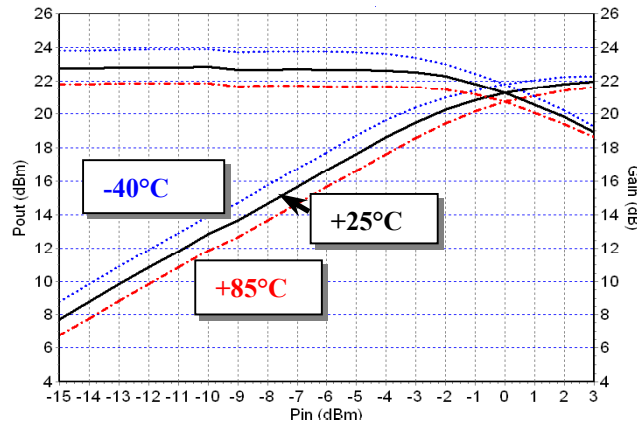


*preliminary*

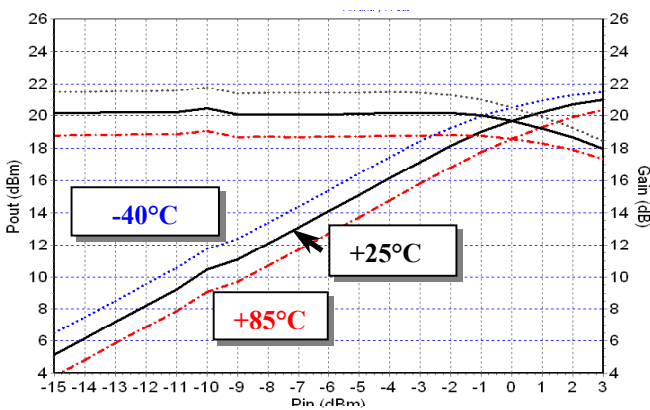
**Gain and Pout versus Frequency and Temperature @ 7 GHz**



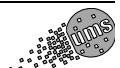
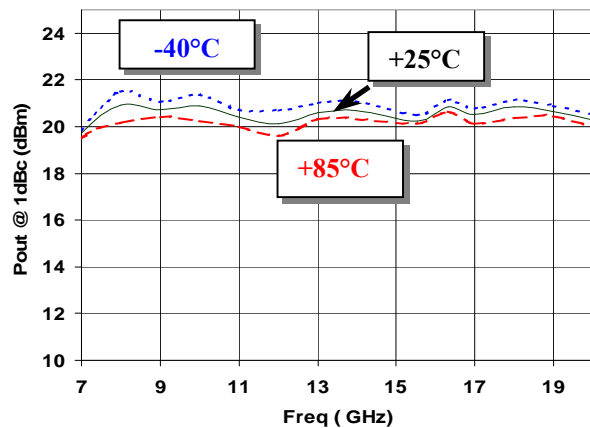
**Gain and Pout versus Frequency and Temperature @ 16 GHz**



**Gain and Pout versus Frequency and Temperature @ 20 GHz**



**Pout @ 1dBc versus Frequency and Temperature**

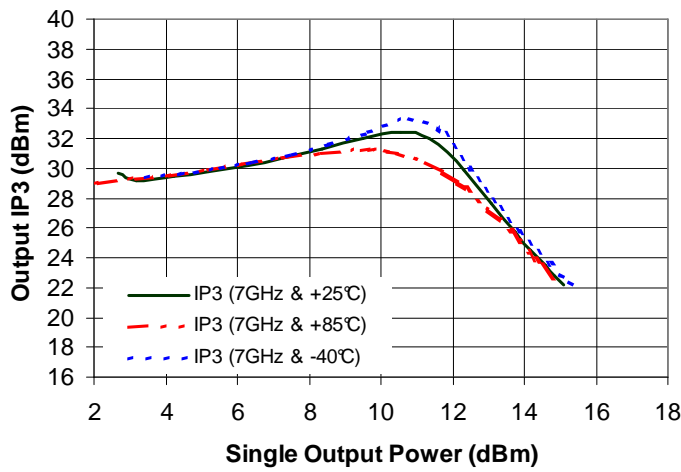




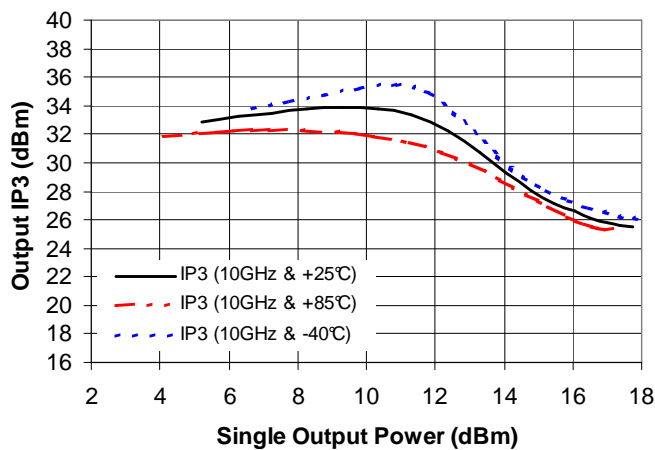
*preliminary*

Vd= +4.2V

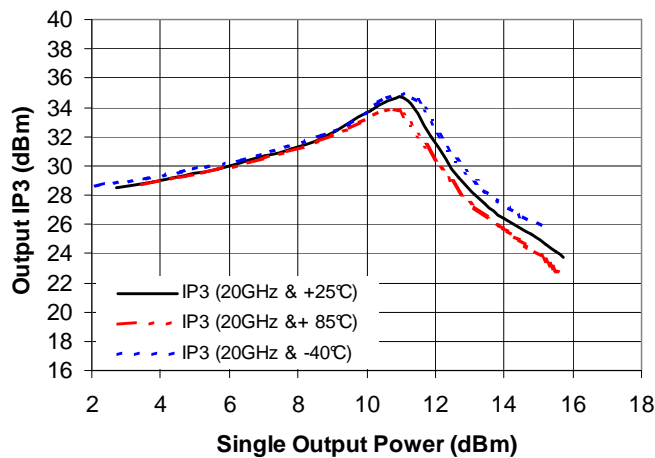
**Output IP3 versus Single Output Power and Temperature @ 7 GHz**



**Output IP3 versus Single Output Power and Temperature @ 10 GHz**



**Output IP3 versus Single Output Power and Temperature @ 20 GHz**



## Typical Package Sij parameters

*preliminary*

Tamb = +25°C, Vd= 4.2V, Typical Id=175mA

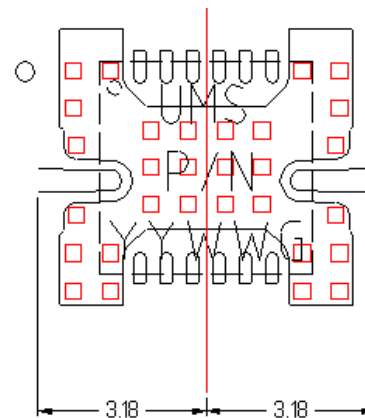
FREQ ( GHz)	S11 (dB)	Ph(S11) ( °)	S21 dB	Ph(S21) ( °)	S12 dB	Ph(S12) ( °)	S22 dB	Ph(S22) ( °)
1	-1.6	91.1	-64.6	-77.9	-74.9	-11.4	-1.7	95.7
2	-1.2	12.0	-43.4	-51.5	-80.6	-71.0	-1.6	16.6
3	-1.0	-57.5	-24.6	-99.2	-65.2	138.5	-1.8	-58.8
4	-1.1	-126.1	3.1	143.8	-65.6	11.7	-6.5	-120.6
5	-4.3	135.4	16.3	5.1	-67.4	59.6	-8.6	-144.5
6	-16.0	-42.1	19.8	-122.8	-70.3	4.7	-9.6	-173.4
7	-12.7	-135.1	20.7	147.2	-74.9	173.9	-11.5	157.3
8	-13.2	-172.1	21.7	70.9	-61.5	94.7	-14.6	133.6
9	-15.4	167.2	22.3	2.8	-63.6	55.3	-18.9	122.4
10	-17.1	162.1	23.0	-62.5	-61.1	-4.2	-21.7	137.8
11	-16.2	155.7	23.3	-125.7	-63.3	-15.4	-19.7	141.6
12	-15.3	140.5	23.3	174.7	-69.4	-84.6	-19.8	124.6
13	-15.4	116.5	23.2	116.2	-66.5	140.1	-20.9	95.1
14	-16.4	93.2	22.8	61.6	-69.7	138.0	-27.5	33.8
15	-17.4	63.7	22.8	7.5	-60.5	161.0	-29.4	-74.4
16	-19.3	15.4	23.1	-46.7	-53.7	109.5	-22.8	-112.8
17	-18.0	-55.1	23.1	-103.7	-57.1	54.6	-20.4	-122.7
18	-13.3	-122.2	23.0	-163.7	-51.1	90.9	-17.0	-134.8
19	-9.1	-176.6	22.5	133.0	-48.0	48.6	-12.7	-149.2
20	-7.0	130.0	20.7	67.8	-47.3	13.1	-9.8	178.1
21	-6.6	81.5	18.1	6.9	-55.3	-22.0	-8.8	144.9
22	-6.9	39.1	15.1	-50.4	-58.1	-24.0	-8.2	111.5
23	-7.3	0.9	12.1	-105.2	-47.8	92.8	-7.8	78.6
24	-7.6	-34.0	8.8	-161.0	-44.6	29.3	-7.4	48.1
25	-6.7	-68.1	4.8	140.6	-46.8	-7.3	-6.6	16.8
26	-6.0	-117.3	-2.4	86.8	-45.4	-8.8	-6.4	-19.3

Refer to the “definition of the Sij reference planes” section below

### Definition of the Sij reference planes

The reference planes are defined from the footprint of the recommended characterization board shown below under the number 96402.

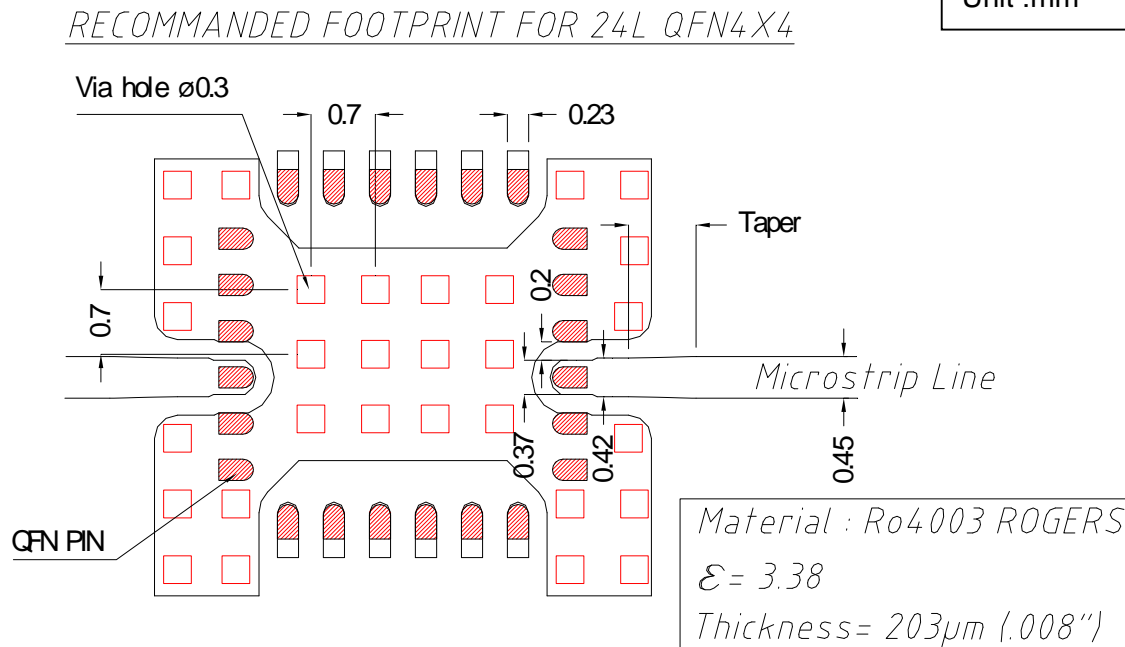
The reference is the symmetrical axis of the package. The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij incorporates this land pattern.



## Recommended footprint for 24L QFN4X4

**preliminary**

Unit :mm

**SMD mounting procedure**

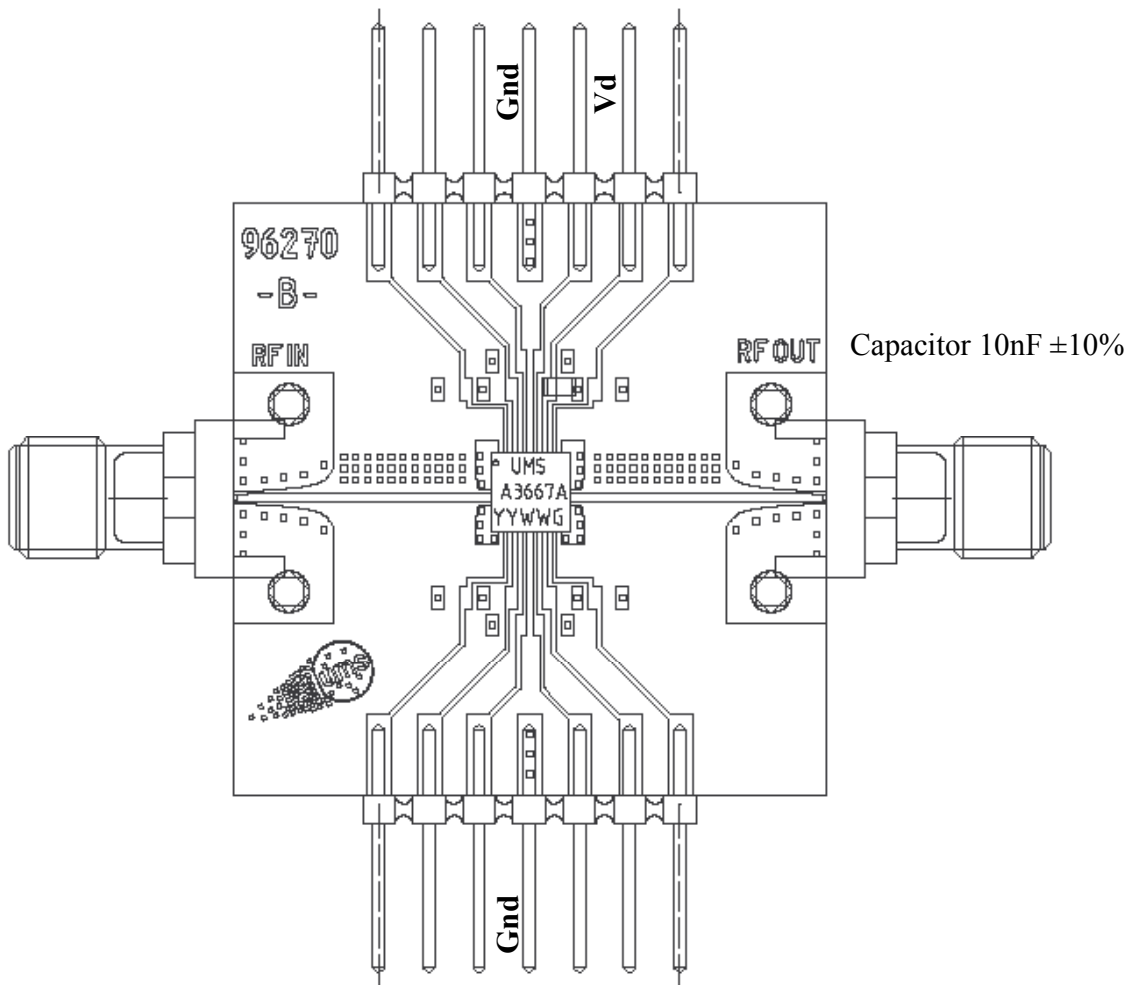
The SMD Leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB ( motherboard) are given in the drawing above.

For the mounting process standard techniques, involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

## Proposed Assembly board "96270" for the 24L-QFN4x4 products characterization.

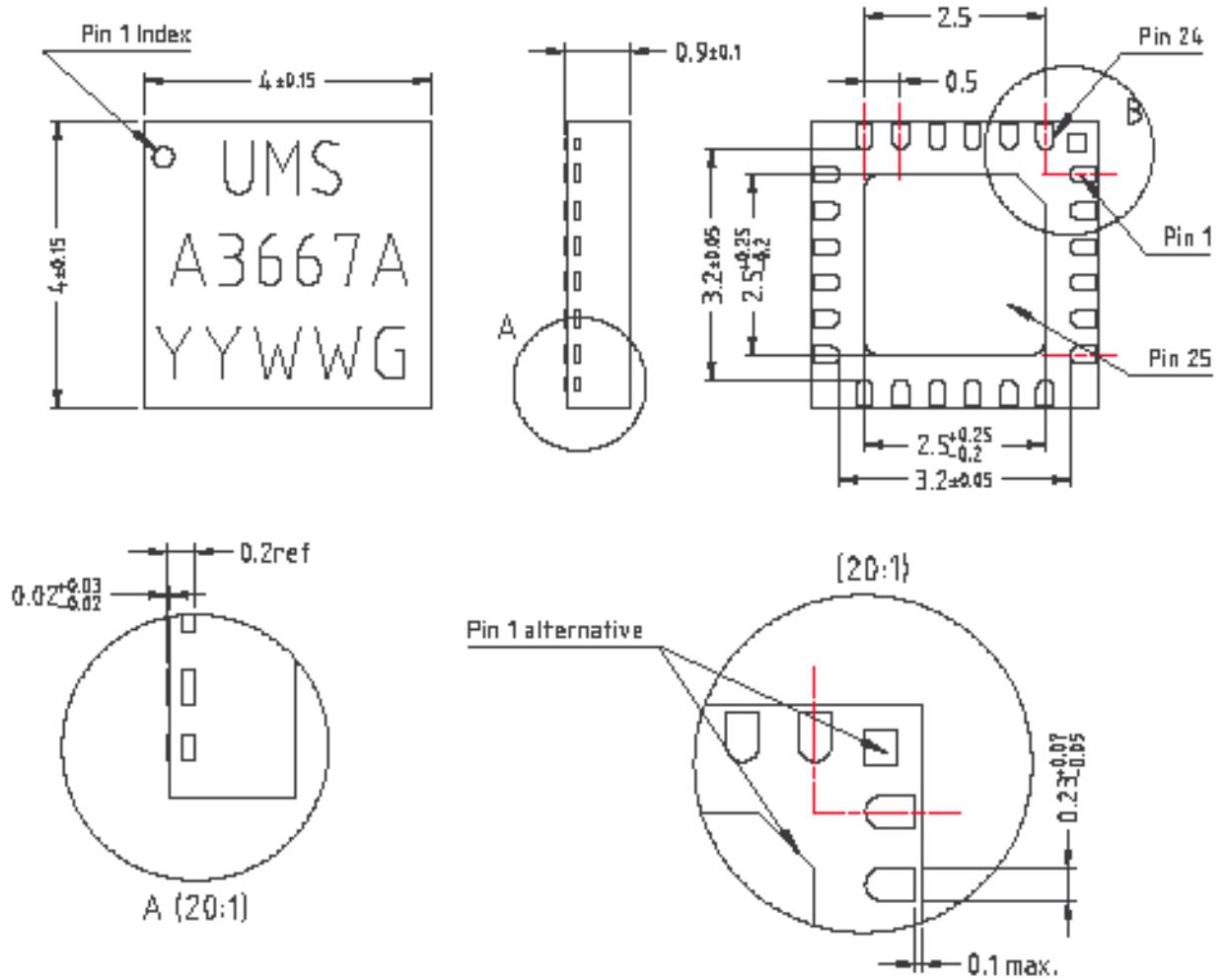
*preliminary*

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



Package outline:

*preliminary*



Units : mm

From the standard : JEDEC MO-220

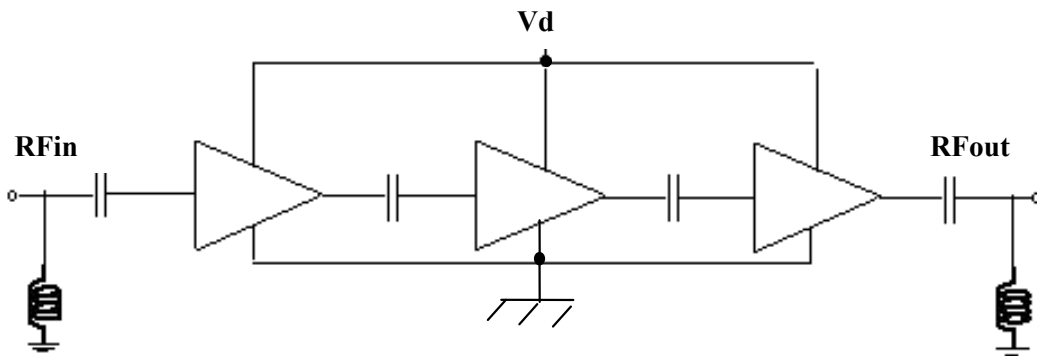
Matt tin, Lead free (Green)

1- Nc	11- Nc	21- Nc
2- Nc	12- Nc	22- Nc
3- Gnd	13- Nc	23- Nc
4- RF IN	14- Gnd	24- Nc
5- Gnd	15- RF OUT	25- Gnd
6- Nc	16- Gnd	
7- Nc	17- Nc	
8- Nc	18- Nc	
9- Nc	19- Nc	
10- Nc	20- VD	

## Note

*preliminary*

Due to ESD protection circuits, RFin and RFout are DC grounded and an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



## Ordering Information

QFN 4x4 RoHS compliant package: CHA3667aQDG/XY  
Stick: XY=20 Tape & reel: XY=21

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