# DMR01
# Low Power Digital Multichannel Receiver

## FEATURES

- LOW COST
- MICRO POWER
- DESIGNED FOR DBPSK CODED DATA
- ERROR CORRECTING DECODER
- DIFFERENT TRANSMIT FREQUENCIES
- UNLICENSED FREQUENCY BAND
- DIFFERENT DATA RATES
- SHORT RANGE APPLICATIONS (up to 3m/10ft)
- TSSOP20 PACKAGE

## APPLICATIONS

- BATTERY POWERED SYSTEMS
- WIRELESS DATA TRANSMISSION
- ACCESS CONTROL
- ALARM FUNCTIONS
- WIRELESS INTERFACE
- REMOTE CONTROL
- WIRELESS TRANSMISSIONS THROUGH CONDUCTING FLUIDS

## General Description

The DMR01 is a micro power receiver chip for low frequency data transmission systems. Based on a 32 kHz clock source, 8 different carrier frequencies from 8.192 kHz to 122.88 kHz are possible ($f_{cr}$ = (2n+1) x 8192 Hz, n = 0..7). Depending on the transmit distance and the transmit time, the DMR01 works with 4 different data rates from 1 to 8 kBaud. The DMR01 is able to receive coded data until with a maximum length of 128 bit for each transmit package. A frame detector gives the possibility to separate the data for different applications. The DMR01 uses a serial SPI register for a simple data exchange with external microcontrollers. Features like input amplifier gain, ADC sensitivity, data rate, selection of coded or uncoded data are programmable via the SPI interface.
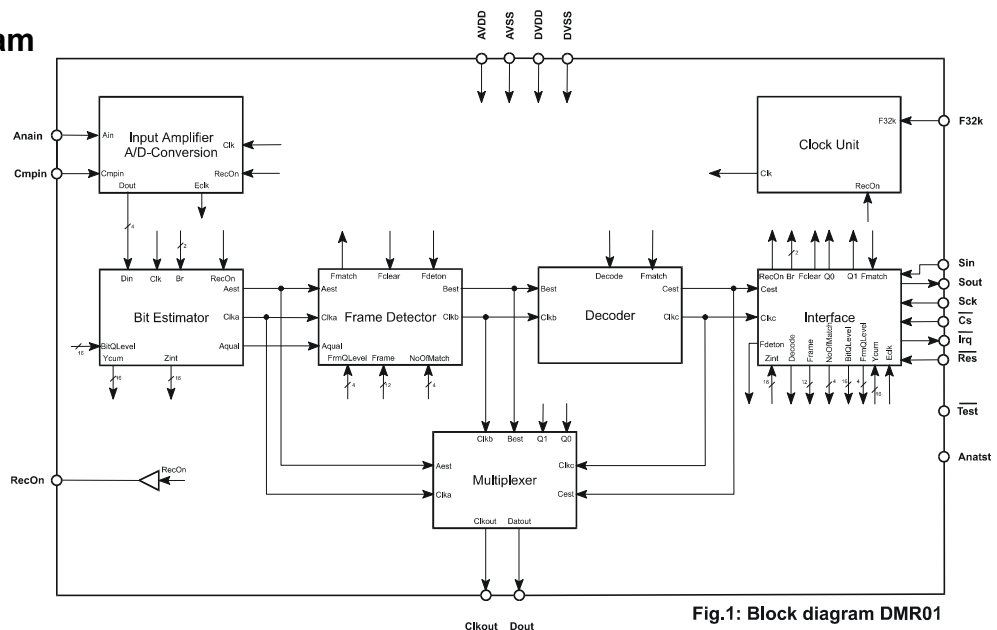
## Block Diagram



**Fig.1: Block diagram DMR01**

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# Electrical Specifications

## AC / DC Characteristics @ VDD = 3.3V ,$T_A$ = 25°C unless otherwise specified

| PARAMETER | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **INPUT RECEIVER BANDWIDTH** | | | | | |
| BW0 = 0 | | | 10 | | kHz |
| BW0 = 1 | | | 130 | | kHz |
| **DATA RATE** | | | | | |
| Br = 00 | | | 1024 | | Bit/s |
| Br = 01 | | | 2048 | | Bit/s |
| Br = 10 | | | 4096 | | Bit/s |
| Br = 11 | | | 8192 | | Bit/s |
| **INPUT @ BW0 = 1** | | | | | |
| Input Bias Voltage | | 0.95 | 1.35 | 1.90 | V |
| Input Impedance | small signal | 271 | 315 | 370 | kΩ |
| Voltage Gain (@ GA = 00) | | 55 | 67 | 70 | dB |
| Voltage Gain (@ GA = 01) | | 49 | 61 | 64 | dB |
| Voltage Gain (@ GA = 10) | | 43 | 55 | 58 | dB |
| Voltage Gain (@ GA = 11) | | 35 | 47 | 50 | dB |
| **INPUT @ BW0 = 0** | | | | | |
| Input Bias Voltage | | 0.95 | 1.28 | 1.75 | V |
| Input Impedance | small signal | 287 | 340 | 410 | kΩ |
| Voltage Gain (@GA = 00) | | 55 | 69 | 70 | dB |
| Voltage Gain (@GA = 01) | | 49 | 63 | 64 | dB |
| Voltage Gain (@GA = 10) | | 43 | 57 | 58 | dB |
| Voltage Gain (@GA = 11) | | 35 | 49 | 50 | dB |
| **PREAMPLIFIER NOISE @ BW0 = 1** | | | | | |
| Spectral Noise Voltage referred to Input (RMS) | @100kHz | | 77 | | nV/√ Hz |
| Broadband Output Noise | 1Hz – 1 MHz | | 165 | | mV |
| **PREAMPLIFIER NOISE @ BW0 = 0** | | | | | |
| Spectral Noise Voltage referred to Input (RMS) | @ 10kHz | | 213 | | nV /√ Hz |
| Broadband Output Noise | 1Hz – 1 MHz | | 193 | | mV |
| **POWERUP TIME** | | | | 100 | μs |
| **RECEIVER WAKE-UP TIME** | | | | 100 | μs |
| **SPI-INTERFACE (Sin, Sout, Sck)** | | | | | |
| Logical low level | | | | 0.3VDD | V |
| Logical high level | | 0.7VDD | | | V |
| Clock frequency | | | | 5 | MHz |
| Clock high time | | 80 | | | ns |
| Clock low time | | 80 | | | ns |
| Rise time (Clock) | | | | 10 | ns |
| Fall time (Clock) | | | | 10 | ns |
| Data input setup time | | | | 5 | ns |
| Data input hold time | | | | 5 | ns |
| Chip select setup time | | | | 10 | ns |
| Chip select hold time | | | | 10 | ns |
| **POWER SUPPLY @ BW0 = 1** | | | | | |
| Standby current (Rec on = 0) | No load, no clock | | 1 | 5 | μA |
| Operating current (Rec on = 1) | $f_{Clk}$ =32kHz | | 56 | 105 | μA |
| **POWER SUPPLY @ BW0 = 0** | | | | | |
| Standby current (Rec on = 0) | No load, no clock | | 1 | 5 | μA |
| Operating current (Rec on = 1) | $f_{Clk}$ =32kHz | | 43 | 90 | μA |
| **TEMPERATURE** | | | | | |
| Specified range | | -20 | 27 | 60 | °C |

## Absolute maximum ratings

| PARAMETER | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Supply Voltage | | 2.5 | 3.6 | 5.5 | V |
| Voltage @ all Inputs and Outputs Pins | | VSS-0.3 | | VDD+0.3 | V |
| ESD protection on all pins | | | 1 | | kV |
| Current @ all Input and Output Pins | | | | 10 | mA |
| Operating Temperature | | -20 | | 85 | °C |
| Storage Temperature | | -65 | | 150 | °C |
| Soldering Temperature | 10 seconds | | | 250 | °C |

# Pin Configuration

## TSSOP20 package

| ANAIN | 1 | | 20 | ANATST |
|---|---|---|---|---|
| CMPIN | 2 | | 19 | AVDD |
| AVSS | 3 | | 18 | NC |
| RECON | 4 | | 17 | TESTB |
| DVSS | 5 | DMR01 | 16 | CSB |
| RESB | 6 | | 15 | SOUT |
| F32K | 7 | | 14 | SIN |
| IRQB | 8 | | 13 | SCK |
| DVSS | 9 | | 12 | DVDD |
| CKOUT | 10 | | 11 | DOUT |

| Pin # | Name | Description |
|---|---|---|
| 1 | ANAIN | RF input signal |
| 2 | CMPIN | Level detect input |
| 3 | AVSS | Analog Ground |
| 4 | RECON | Power for external circuit |
| 5 | DVSS | Digital ground |
| 6 | RESB | Reset |
| 7 | F32K | Input for external clock |
| 8 | IRQB | Interrupt (valid data received) |
| 9 | DVSS | Digital ground |
| 10 | CLKOUT | Clock for uncoded data |
| 11 | DOUT | Uncoded data output |
| 12 | DVDD | Digital supply voltage |
| 13 | SCK | Serial data clock for SPI |
| 14 | SIN | Serial data input for SPI |
| 15 | SOUT | Serial output for SPI |
| 16 | CSB | Chip select |
| 17 | TESTB | Test pin |
| 18 | NC | Not connected |
| 19 | AVDD | Analog supply voltage |
| 20 | ANATST | Test pin (output) |

# Module Description

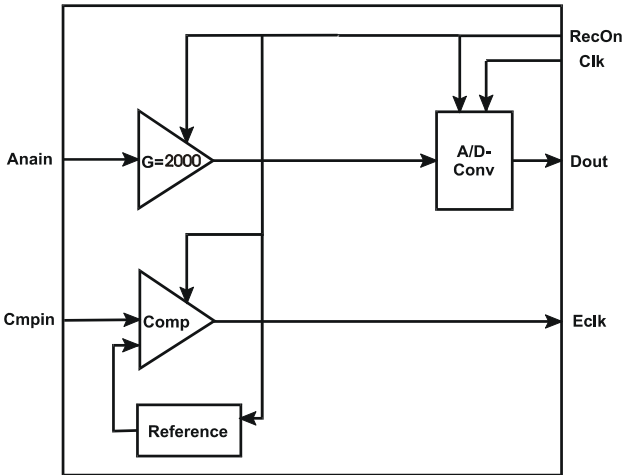## Input Amplifier and A/D Conversion



Fig.2: Analog Input stage

Fig. 2 shows a block diagram of the input stage. The input stage consists of an input amplifier, a flash A/D-converter and a comparator for high energy detection of the input signal. The input amplifier has a gain of about 2'000 which simplifies external circuitry. The A/D-converter has a resolution of 4 Bit and converts the input signal into a signed 4 bit word within less than $1\mu s$. Sampling frequency is 32'768 Hz. To save power in stand by mode the analog input stage can be switched of ('RecOn').

The comparator detects high level input signals on it's input Cmpin. This input is normally connected directly to the receiving antenna. Due to the modulation technique, there will always be a number of sinusoidal waves per transmitted bit. The output of the comparator enters therefore a counter (located in the interface part) which counts the number of waves with high energy. At the end of a transmission the value of this counter gives an information about the energy level of the received data stream. This feature is used to detect if a transmitter is located very close to the receiving antenna.
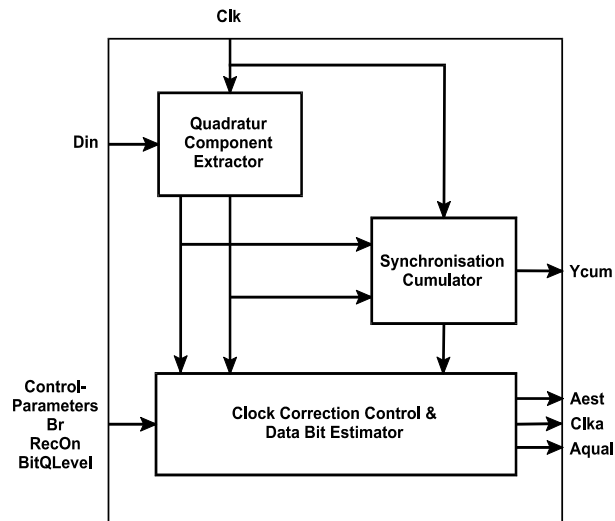
## Bit Estimator



Fig. 3: Bit Estimator

Fig. 3 shows a block diagram of the bit estimator. The bit estimator uses a very sophisticated and efficient algorithm to estimate incoming data out of the 4 bit information of the A/D-converter. It is designed to work with phase modulated input signals. More precisely, the modulation technique is differential binary phase shift keying (DBPSK). This means that there is a phase shift of 180° with every transmitted logic 1. Depending on the programmed baud rate the estimator expects 1, 2, 4 or 8 sinusoidal waves per bit for baud rates of 8'192, 4'096, 2'048 or 1'024 bit/s. The estimator is also able to detect the signal energy. 'Aqual' is high if the estimated bit 'Aest' has an energy level of more than programmed in 'BitQLevel'. 'Aest' and 'Aqual' are updated with the negative edge of 'Clka'. To save power in stand by mode the bit estimator can be switched off ('RecOn').
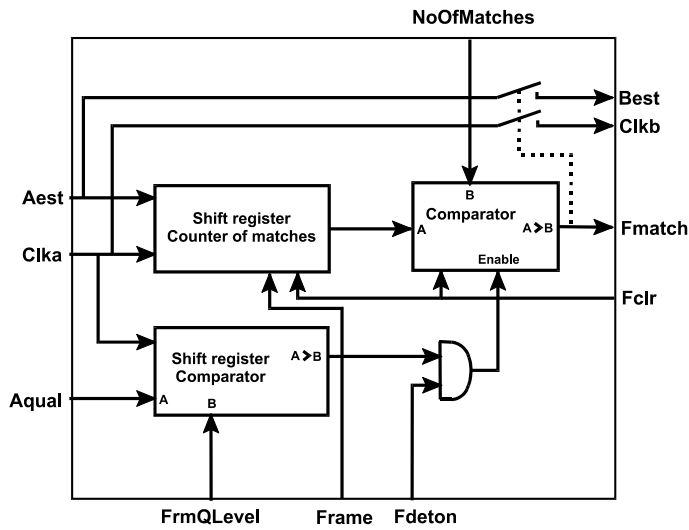
## Frame Detector



**Fig.4: Frame Detector**

Fig. 4 shows a block diagram of the frame detector. It's function is to detect a special string in the incoming data stream of 'Aest' / 'Clka'. The string which will be detected can be programmed with the 12 bit input word 'Frame'. The detector accepts an incoming string as start frame if a certain number of bits ('FrmQLevel') of the incoming frame word have a high energy level ('Aqual' = 1) and a certain number of bits ('NoOfMatch') match the frame word 'Frame'. In this case the signal 'FMatch' will be change from low to high and the following input bits ('Aest' / 'Clka') will be connected to 'Best' / 'Clkb'. 'Best' is updated with the negative edge of 'Clkb' and the detector will not recognize any other strings until the 'Fclr' input is set to '1'. 'Fclear' is controlled by the interface. It resets the detector if transmission is finished. The frame detection function can be disabled ('Fdeton' = 0). In this case the decoder will also not work and 'Best', 'Clkb' remains 0.
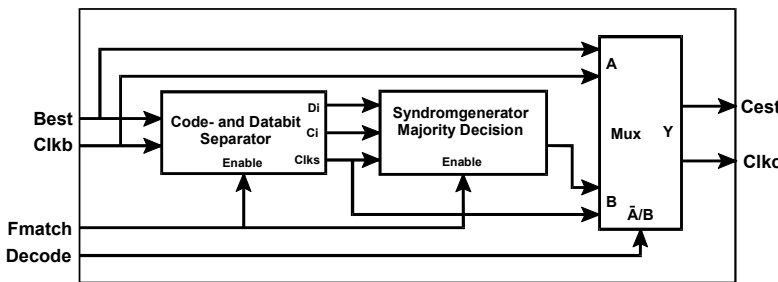
## Decoder



**Fig.5: Decoder**

Fig. 5 shows a block diagram of the decoder. It decodes a convolutional code with rate ½ using a polynomial function.

The incoming bits are grouped in pairs of 2 bits whereas the first one is the code bit and the second one is the original data bit. The threshold decoder decodes these set of pairs into a data stream appearing at 'Cest' / 'Clkc'. Data will be updated on the negative edge of 'Clkc'. The decoding procedure will be started with a high level at 'Fmatch'. It is also possible to disable the decoding function. If 'Decode' is low the decoder will map 'Best' / 'Clkb' to 'Cest' / 'Clkc' if Fmatch is high.

## Interface
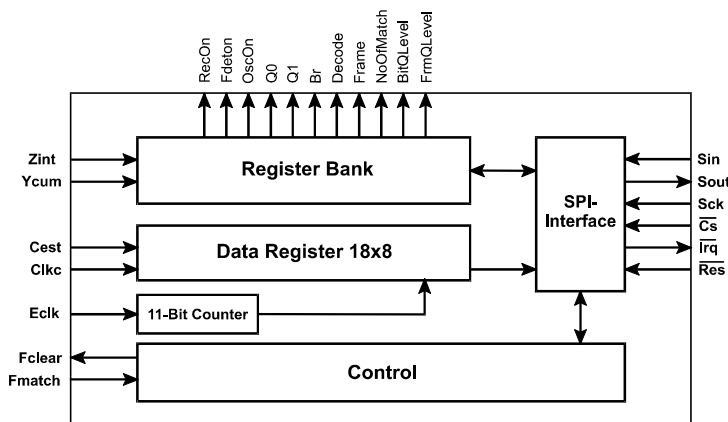


**Fig.7: Interface**

Fig. 7 shows the block diagram of the Interface. The interface has different functions:

- Communication with a microprocessor (SPI-interface)
- Saving all register values for programming
- Saving incoming data
- Interrupt function
- Counting pulses for high input energy detection

Additionally the interface also handles the end of a transmission. The first 4 incoming bits (MSB first) after the low to high transition of 'Fmatch' define the number of bytes the currently transmitted block will have. The interface resets the frame detector exactly after this number of bytes is stored. An interrupt will be generated after completion of transmission (IRQ changes to low) and a request flag is set in the interrupt register.

A counter counts the pulses from the comparator. The upper 8 bit of the 11bit counter can be read by the SPI-interface.

# Communication via SPI Interface

Each data transfer is initialized with a 8bit control word:

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Cmd2 | Cmd1 | Cmd0 | Adr4 | Adr3 | Adr2 | Adr1 | Adr0 |

Cmd2...Cmd0 represent the command word and define the action. Adr4..Adr0 is the address which will be accessed. The following commands are possible:

| Cmd2 | Cmd1 | Cmd0 | Action |
|------|------|------|--------|
| 0 | 0 | 0 | Not defined |
| 0 | 0 | 1 | Read register (address 00 to 07H) |
| 0 | 1 | 0 | Read YCUML (only for test) |
| 0 | 1 | 1 | Read YCUMH (only for test) |
| 1 | 0 | 0 | Read incoming data (address 00 to 11H) |
| 1 | 0 | 1 | Write register (address 00 to 07H) |
| 1 | 1 | 0 | Read ZINTL (only for test) |
| 1 | 1 | 1 | Read ZINTH (only for test) |

Each data transfer starts with a command and a corresponding address. Communication is initialized with the falling edge of CS. There is an auto increment function implemented for read and write operation. This means that the command word is necessary only once for consecutive addresses.
The MSB (most significant bit, bit7) has to be set first in write operation and will be present first in read operation. Data at 'Sin' is sampled with the positive edge of 'Sck' whereas Data at 'Sout' will be updated with the negative edge of 'Sck'.
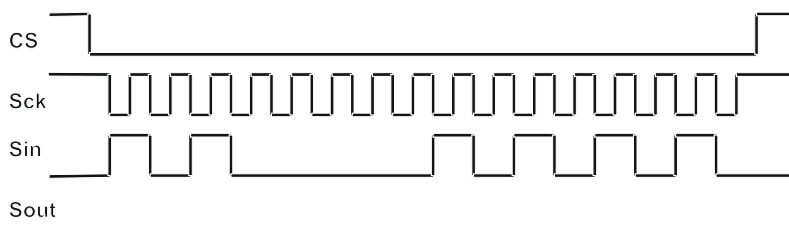
## Bus Timing

### Write Sequence



Fig.8 shows the write timing. In this case the command word is "write register (address 00H)". The value which is stored in this register is AAH.
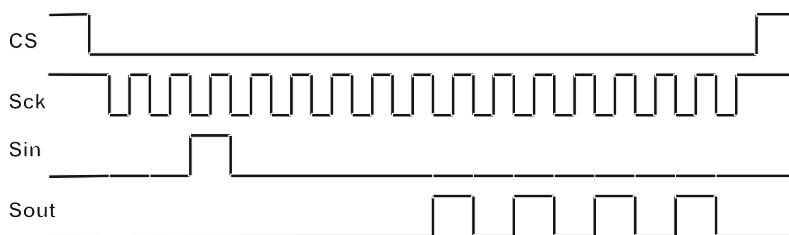
Fig. 8: Write Sequence

### Read Sequence



Fig.9 shows the read timing. In this case the command word is "read register (address 00H)". The value which is clocked at 'Sout' is AAH.

Fig. 9: Read Sequence

# Registers for DMR01 configuration

The system consists of several registers for programming the desired function. All registers will be reset to 0 with 'Res' = '0'.

## Control register

**Register name:** **CNT**
**Access:** R/W
**Description:** **Control register for programming the function of the DMR-01**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|--------|---------|--------|-------|---------|
| Out1 | Out0 | Br1 | Br0 | Dec on | Fdet on | Rec on | | 00H |

**Description:** **Out1,Out0 =** **00 : no internal signals available at Pin 'Datout' and Pin 'Clkout'**
01 : 'Aest' is mapped to 'Datout', 'Clka' is mapped to 'Clkout'
10 : 'Best' is mapped to 'Datout', 'Clkb' is mapped to 'Clkout'
11 : 'Cest' is mapped to 'Datout', 'Clkc' is mapped to 'Clkout'

Br1,Br0 = 00 : baud rate is set to 1'024 bit/s
01 : baud rate is set to 2'048 bit/s
10 : baud rate is set to 4'096 bit/s
11 : baud rate is set to 8'192 bit/s

Dec on = 0 : Decoder is not enabled
1 : Decoder is enabled

Fdet on = 0 : Frame detector is off
1 : Frame detector is on

Rec on = 0 : Receiver is off (including input amplifier)
**1 : Receiver is on**

In order to guarantee proper function 'Rec on' must be set to '0' before any of Bit2 to Bit5 is changed.

## Interrupt register

**Register name:** **INT**
**Access:** R/W   (write access is only possible for IE)
**Description:** **Interrupt status register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| IRQ | | | | IE | | | | 01H |

**Description:** **IE =** **0 : Interrupt capability disabled**
1 : Interrupt capability enabled

**IRQ =** **0 : Interrupt not requested**
1 : Interrupt request after received data

⚠ **An interrupt request will be reset by 'Res' = '0' or by reading any of the data registers. In this case the positive edge of 'CS' will trigger the clear function. This means that 'CS' must be high to start the receiver again.**

## Bit Quality level registers

**Register name:** **BITQLEVELH (high byte)**
**BITQLEVELL (low byte)**
Access: R/W
**Description:** **Bit quality level (energy level which represents good bit quality)**

High byte:

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| BQL15 | BQL14 | BQL13 | BQL12 | BQL11 | BQL10 | BQL9 | BQL8 | 02H |

**Low Byte:**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| BQL7 | BQL6 | BQL5 | BQL4 | BQL3 | BQL2 | BQL1 | BQL0 | 03H |

## Frame quality level Register

**Register name:** **FRMQLEVEL**
Access: R/W
**Description:** **Frame quality level (number of bits out of the 12 frame bits which must have an energy level which is higher than programmed in "Bit Quality level register" such that a frame is accepted) and number of matches (number of incoming bits which have to match the frame word) for acceptance.**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| NOM3 | NOM2 | NOM1 | NOM0 | FQL3 | FQL2 | FQL1 | FQL0 | 04H |

The numbers represented in FQL3..FQL0 and NOM3..NOM0 must be less or equal 12.

## Frame registers

**Register name:** **FRAMEH (high byte)**
**FRAMEL (low byte)**
Access: R/W
**Description:** **High Byte of the frame word**

High byte:

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| - | - | - | - | FRM11 | FRM10 | FRM9 | FRM8 | 05H |

**Low byte:**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| FRM7 | FRM6 | FRM5 | FRM4 | FRM3 | FRM2 | FRM1 | FRM0 | 06H |

## Controlregister for analog part

**Register name:**     **ANACNTRL**
Access:              R/W
**Description:**         **Setup of analog part**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| GA1 | GA0 | BW0 | ADR1 | ADR0 | CPS2 | CPS1 | CPS0 | 07H |

**Description: CPS2,CPS1,CPS0:**     **This 3 Bits define the reference level of the comparator.**
           **"000" is Vdd/2. "111" means Vdd*15/16.**

ADR1,ADR0:            00 : Input range for A/D-converter is about +/- 0.4 * Vdd
                                  01 : Input range for A/D-converter is about +/- 0.2 * Vdd
                                  10 : Input range for A/D-converter is about +/- 0.1 * Vdd
                                  11 : Input range for A/D-converter is about +/- 0.05 * Vdd

BW0 =                   0 : 8 kHz Input Receiver Bandwidth Mode
                                  1 : 122 kHz Input Receiver Bandwidth Mode

GA1,GA0:              00 : Input amplifier voltage gain is about 2'000
                                  01 : Input amplifier voltage gain is about 1'000
                                  10 : Input amplifier voltage gain is about 500
                                  11 : Input amplifier voltage gain is about 200

## Cumulator output registers

**Register name:**     **YCUMH (high byte)**
                                **YCUML (low byte)**
Access:              R
**Description:**         **Output of the cumulator (only for test purposes)**

High byte:

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| YCUM15 | YCUM14 | YCUM13 | YCUM12 | YCUM11 | YCUM10 | YCUM9 | YCUM8 | - |

**Low byte:**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| YCUM7 | YCUM6 | YCUM5 | YCUM4 | YCUM3 | YCUM2 | YCUM1 | YCUM0 | - |

**These 2 registers are read by direct commands (see 5.7).**

## Statistic output registers

**Register name:**     **ZINTH (high byte)**
                                  **ZINTL (low byte)**
Access:              R
**Description:**         **Statistic of the Bitestimator (only for test purposes)**

High byte:

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| ZINT15 | ZINT14 | ZINT13 | ZINT12 | ZINT11 | ZINT10 | ZINT9 | ZINT8 | - |

**Low byte:**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| ZINT7 | ZINT6 | ZINT5 | ZINT4 | ZINT3 | ZINT2 | ZINT1 | ZINT0 | - |

**These 2 registers are read by direct commands.**

# Registers for data receiving

All data registers will be reset to 0 with 'Res' = '0'.

## Number of received Bytes

**Register name:**     **NOB**
Access:     R
**Description:**     **Number of received bytes - 1 of the last reception.**
                     **If NOB is zero, then one byte of data was transmitted.**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| 0 | 0 | 0 | 0 | NOB3 | NOB2 | NOB1 | NOB0 | 00H |

## Data bytes

Access:     R
**Description:**     **Received data. The end address depends on the message length (max. 10H)**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| MSB | | | | | | | LSB | 01H to 10H |

## High energy detector

**Register name:**     **ECOUNTER**
Access:     R
**Description:**     **Number of signal waves at the comparator input with high energy.**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Address |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| EC10 | EC9 | EC8 | EC7 | EC6 | EC5 | EC4 | EC3 | * |

ECOUNTER represents the number of signal waves at the 'Cmpin' input with a level higher than the reference value. Only every 8th clock is counted (positive edge triggered).

*: The address of this register depends on the length of the received data stream. ECONTER is attached at the end of the message.

ECOUNTER will be reset after reading data.

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# Received data

## Dataformat and Coding

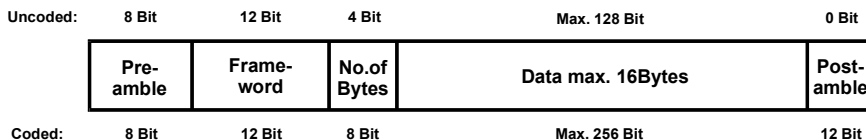| | | | | | | |
|---|---|---|---|---|---|---|
| **Uncoded:** | **8 Bit** | **12 Bit** | **4 Bit** | **Max. 128 Bit** | | **0 Bit** |
| | Pre-amble | Frame-word | No.of Bytes | Data max. 16Bytes | | Post-amble |
| **Coded:** | **8 Bit** | **12 Bit** | **8 Bit** | **Max. 256 Bit** | | **12 Bit** |

**Fig. 10: Dataformat**

For a proper function of the receiver, the transmitter has to do the correct function. First it is important to note the used dataformat as described in Fig. 8.
Each datastream consists of a 8 bit preamble, a 12 bit frameword, a 4 bit information for the number of transmitted bytes, the data (up to 16 Bytes) and a postamble. A '0000' for the number of bytes means that 1 byte is transmitted. A '1111' means that 16 bytes are transmitted.

For each bit, the transmitter must transmit a number of consecutive sinusoidal waves. This number is 8 for a baud rate of 1kbit/s, 4 for a baud rate of 2 kBit/s, 2 for a baud rate of 4 kbit/s and 1 for baud rate 8 kbit/s. The modulation technique is Differential Binary Phase Shift Keying (DBPSK). Therefore the phase of the sinusoidal waves has to be shifted by 180° if the bit (which actually should be transmitted) is logic high. The phase remains unchanged during transmission of this bit.

If the coding function is used, the information has to be encoded according to a special function (not disclosed at the moment). Note that in case of coded transmissions only the data after the frameword has to be encoded. The postamble is necessary to bring the decoder to it's default state. Preamble and postamble should use an all one sequence('11...11') In case of uncoded transmission the postamble is not necessary.

The encoder must be initialized with '000000' prior to every datastream.

# Package Information

**TSSOP20**

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|        | MIN   | NOM      | MAX  | NOTE  |
|--------|-------|----------|------|-------|
| A      |       |          | 1.10 |       |
| A1     | 0.05  |          | 0.15 |       |
| A2     | 0.85  | 0.90     | 0.95 |       |
| D      | 6.40  | 6.50     | 6.60 | 3, 8  |
| E1     | 4.30  | 4.40     | 4.50 | 4, 8  |
| E      |       | 6.4 BSC  |      |       |
| e      |       | 0.65 BSC |      |       |
| L      | 0.50  | 0.60     | 0.75 |       |
| R      | 0.09  |          |      |       |
| R1     | 0.09  |          |      |       |
| b      | 0.19  |          | 0.30 | 5     |
| b1     | 0.19  | 0.22     | 0.25 |       |
| c      | 0.09  |          | 0.20 |       |
| c1     | 0.09  |          | 0.16 |       |
| $\theta1$ | 0°  |          | 8°   |       |
| L1     |       | 1.0 REF  |      |       |
| aaa    |       | 0.10     |      |       |
| bbb    |       | 0.10     |      |       |
| ccc    |       | 0.05     |      |       |
| ddd    |       | 0.20     |      |       |
| e      |       | 0.65 BSC |      |       |
| $\theta2$ |    | 12° REF  |      |       |
| $\theta3$ |    | 12° REF  |      |       |

4.40 mm Body
0.65 mm Lead Pitch

Note : 1, 2        Issue : A        BSC = Basic ...

NOTES:

1.  ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2.  DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.

3.  DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

4.  DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5.  DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM FOR 0.5 MM PITCH PACKAGES.

6.  TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7.  DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

8.  DIMENSIONS 'D' ANO 'E1' ARE TO BE DETERMINED AT DATUM PLANE -H-

9.  THIS DIMENSION APPLIES ONLY TO VARIATIONS WITH AN EVEN NUMBER OF LEADS PER SIDE. FOR VARIATION WITH AN ODD NUMBER OF LEADS PER SIDE, THE "CENTER" LEAD MUST BE COINCIDENT WITH THE PACKAGE CENTERLINE,. DATUM A.

10. ACROSS SECTION A – A TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEADTIP.

11. THIS VARIATION IS NOT REGISTERED WITH JEDEC.