Integrated Circuit Systems, Inc.

ICS873990

LOW VOLTAGE, LVCMOS/ CRYSTAL-TO-LVPECL/ECL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS873990 is a low voltage, low skew, 3.3V LVPECL/ECL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS873990 has two selectable clock inputs. The XTAL1 and XTAL2 are used to interface to a crystal and the TEST_CLK pin can accept a LVCMOS or LVTTL input. This device has a fully integrated PLL along with frequency configurable outputs. An external feedback input and output regenerates clocks with "zero delay".

The four independent banks of outputs each have their own output dividers, which allow the device to generate a multitude of different bank frequency ratios and output-to-input frequency ratios. The output frequency range is 25MHz to 400MHz and the input frequency range is 6.25MHz to 125MHz. The PLL_SEL input can be used to bypass the PLL for test and system debug purposes. In bypass mode, the input clock is routed around the PLL and into the internal output dividers.

The ICS873990 also has a SYNC output which can be used for system synchronization purposes. It monitors Bank A and Bank C outputs for coincident rising edges and signals a pulse per the timing diagrams in this data sheet. This feature is used primarily in applications where Bank A and Bank C are running at different frequencies, and is particularly useful when they are running at non-integer multiples of each other.

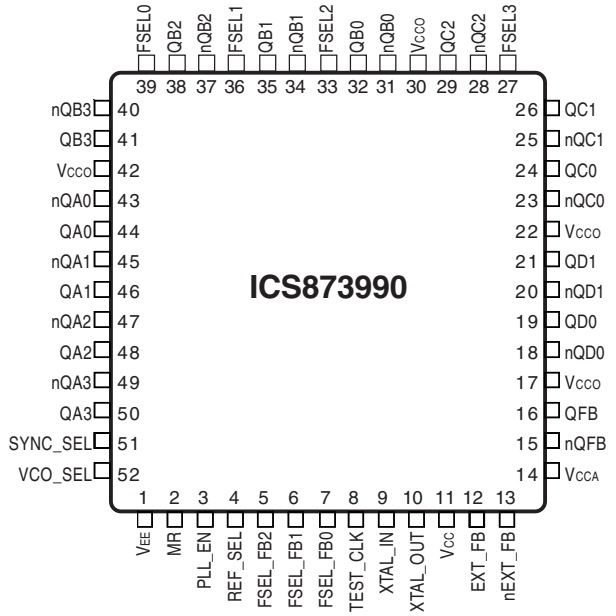
Example Applications:

1. Line Card Multiplier: Multiply 19.44MHz from a back-plane to 77.76MHz on the line card ASIC and Serdes.
2. Zero Delay Buffer: Fan out up to thirteen 100MHz copies from a reference clock to multiple processing units on an embedded system.

FEATURES

- 14 differential LVPECL outputs
- Selectable crystal oscillator interface or TEST_CLK inputs
- TEST_CLK accepts the following input levels: LVCMOS, LVTTL
- Output frequency: 400MHz (maximum)
- Crystal input frequency range: 10MHz to 25MHz
- VCO range: 200MHz to 800MHz
- Output skew: 250ps (maximum)
- Cycle-to-cyle jitter: ±50ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 3.135V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.465V to -3.135V
- 0°C to 70°C ambient operating temperature
- Industrial temperature available upon request
- Lead-Free package fully RoHS compliant

PIN ASSIGNMENT



52-Lead LQFP
10mm x 10mm x 1.4mm package body
Y package
Top View

BLOCK DIAGRAM

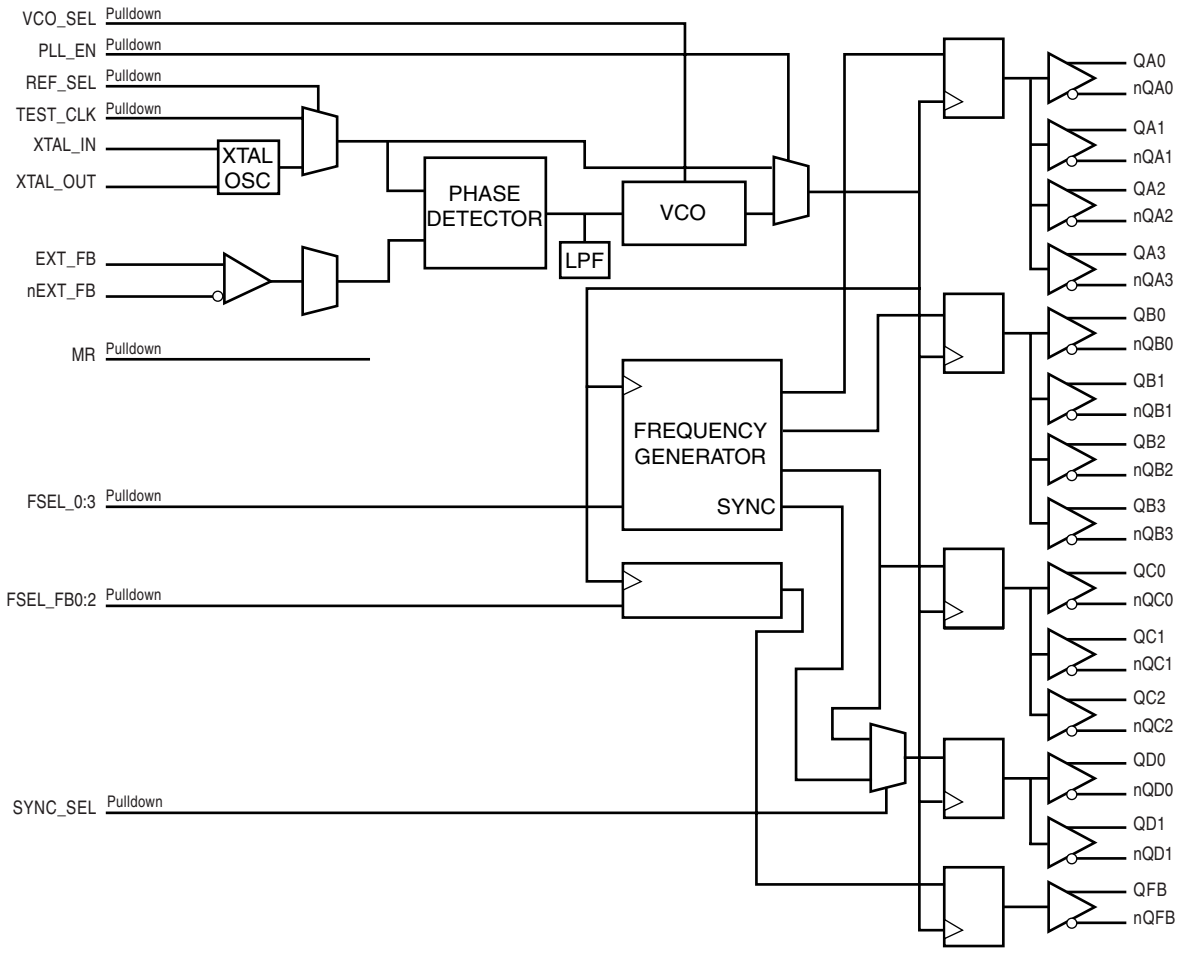


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{EE}	Power		Negative supply pin.
2	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx) to go low and the inverted outputs (nQx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
3	PLL_EN	Input	Pulldown	PLL enable pin. When logic LOW, PLL is enabled. When logic HIGH, PLL is in bypass mode. LVCMOS/LVTTL interface levels.
4	REF_SEL	Input	Pulldown	Selects between the different reference inputs as the PLL reference source. When logic LOW, selects crystal inputs. When logic HIGH, selects TEST_CLK. LVCMOS/LVTTL interface levels.
5 6 7	FSEL_FB2 FSEL_FB1 FSEL_FB0	Input	Pulldown	Feedback frequency select pins. LVCMOS/LVTTL interface levels.
8	TEST_CLK	Input	Pulldown	LVCMOS/LVTTL test clock input.
9, 10	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
11	V_{CC}	Power		Core supply pin.
12	EXT_FB	Input	Pulldown	External feedback input.
13	nEXT_FB	Input	Pullup/ Pulldown	External feedback input. V_{CC}/2 default when left floating.
14	V_{CCA}	Power		Analog supply pin.
15, 16	nQFB, QFB	Output		Differential feedback output pair. LVPECL interface levels.
17, 22, 30, 42	V_{CCO}	Power		Output supply pins.
18, 19	nQD0, QD0	Output		Differential output pair. LVPECL interface levels.
20, 21	nQD1, QD1	Output		Differential output pair. LVPECL interface levels.
23, 24	nQC0, QC0	Output		Differential output pair. LVPECL interface levels.
25, 26	nQC1, QC1	Output		Differential output pair. LVPECL interface levels.
27 33 36 39	FSEL3 FSEL2 FSEL1 FSEL0	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
28, 29	nQC2, QC2	Output		Differential output pair. LVPECL interface levels.
31, 32	nQB0, QB0	Output		Differential output pair. LVPECL interface levels.
34, 35	nQB1, QB1	Output		Differential output pair. LVPECL interface levels.
37, 38	nQB2, QB2	Output		Differential output pair. LVPECL interface levels.
40, 41	nQB3, QB3	Output		Differential output pair. LVPECL interface levels.
43, 44	nQA0, QA0	Output		Differential output pair. LVPECL interface levels.
45, 46	nQA1, QA1	Output		Differential output pair. LVPECL interface levels.
47, 48	nQA2, QA2	Output		Differential output pair. LVPECL interface levels.
49, 50	nQA3, QA3	Output		Differential output pair. LVPECL interface levels.
51	SYNC_SEL	Input	Pulldown	Sync output select pin. When LOW, the SYNC output follows the timing diagram (page 5). When HIGH, QD output follows QC output.
52	VCO_SEL	Input	Pulldown	Selects VCO range. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLup}	Input Pullup Resistor			51		kΩ

TABLE 3A. SELECT PIN FUNCTION TABLE

Inputs				Outputs		
FSEL3	FSEL2	FSEL1	FSEL0	QAx	QBx	QCx
0	0	0	0	÷ 2	÷ 2	÷ 2
0	0	0	1	÷ 2	÷ 2	÷ 4
0	0	1	0	÷ 2	÷ 4	÷ 4
0	0	1	1	÷ 2	÷ 2	÷ 6
0	1	0	0	÷ 2	÷ 6	÷ 6
0	1	0	1	÷ 2	÷ 4	÷ 6
0	1	1	0	÷ 2	÷ 4	÷ 8
0	1	1	1	÷ 2	÷ 6	÷ 8
1	0	0	0	÷ 2	÷ 2	÷ 8
1	0	0	1	÷ 2	÷ 8	÷ 8
1	0	1	0	÷ 4	÷ 4	÷ 6
1	0	1	1	÷ 4	÷ 6	÷ 6
1	1	0	0	÷ 4	÷ 6	÷ 8
1	1	0	1	÷ 6	÷ 6	÷ 8
1	1	1	0	÷ 6	÷ 8	÷ 8
1	1	1	1	÷ 8	÷ 8	÷ 8

TABLE 3B. FEEDBACK CONTROL FUNCTION TABLE

Inputs			Outputs
FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	÷2
0	0	1	÷4
0	1	0	÷6
0	1	1	÷8
1	0	0	÷8
1	0	1	÷16
1	1	0	÷24
1	1	1	÷32

TABLE 3C. INPUT CONTROL FUNCTION TABLE

Control Input Pin	Logic 0	Logic 1
PLL_EN	Enables PLL	Bypasses PLL
VCO_SEL	fVCO	fVCO/2
REF_SEL	Selects XTAL	Selects TEST_CLK
MR	---	Resets outputs
SYNC_SEL	Selects outputs	Match QC Outputs

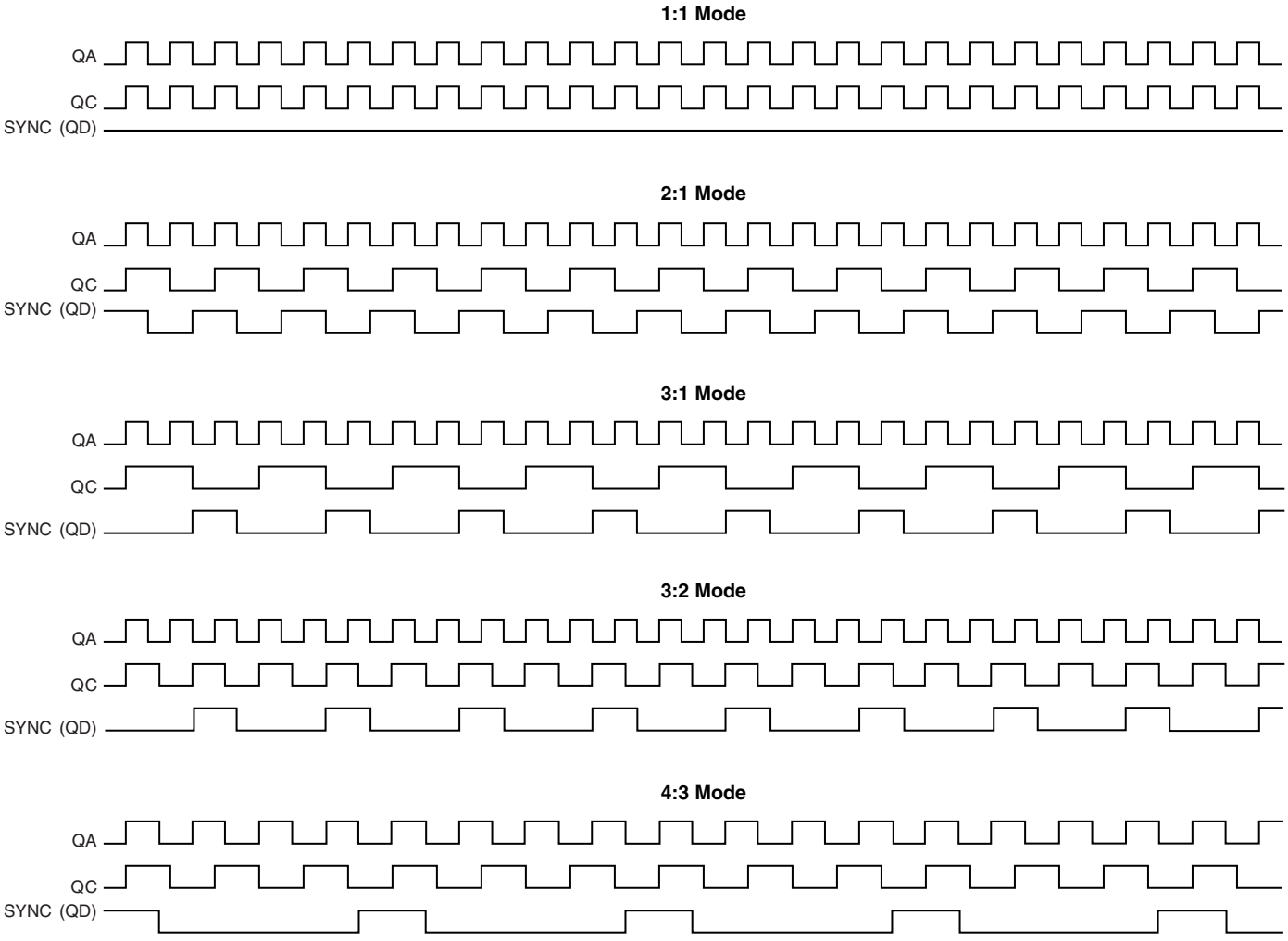


FIGURE 1. TIMING DIAGRAMS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	42.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maxi-mum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current				150	mA
I_{CCA}	Analog Supply Current				15	mA
I_{CCO}	Output Supply Current				95	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	REF_SEL, SYNC_SEL, FSEL_FB0:FB2, PLL_EN, FSEL0:3, MR, VCO_SEL		2		V_{CC} + 0.3	V
		TEST_CLK		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	REF_SEL, SYNC_SEL, FSEL_FB0:FB2, PLL_EN, FSEL0:3, MR, VCO_SEL		-0.3		0.8	V
		TEST_CLK		-0.3		1.3	V
I_{IH}	Input High Current		$V_{CC} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current		$V_{IN} = 0V$, $V_{CC} = 3.465V$	-5			µA

TABLE 4B. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage, NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage, NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 6. PLL INPUT REFERENCE CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
t_R / t_R	Input Rise/Fall Time	TEST_CLK				3	ns
f_{REF}	Reference Frequency VCO_SEL = 0		Feedback ÷ 6	66.66		133.33	MHz
			Feedback ÷ 8	50		100	MHz
			Feedback ÷ 16	25		50	MHz
			Feedback ÷ 24	16.66		33.33	MHz
			Feedback ÷ 32	12.5		25	MHz
	Reference Frequency VCO_SEL = 1		Feedback ÷ 4	50		100	MHz
			Feedback ÷ 6	33.33		66.66	MHz
			Feedback ÷ 8	25		50	MHz
			Feedback ÷ 16	12.5		25	MHz
			Feedback ÷ 24	8.33		16.66	MHz
			Feedback ÷ 32	6.25		12.5	MHz
f_{REFDC}	Reference Input Duty Cycle			25		75	%

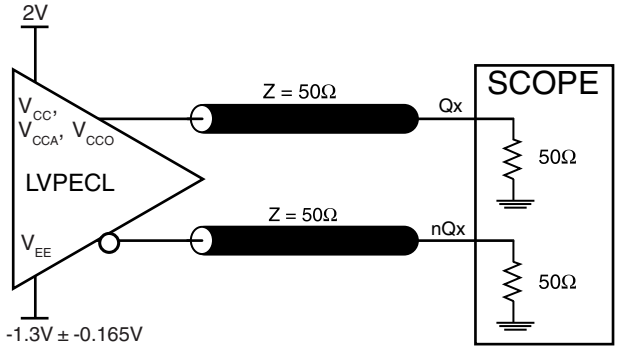
NOTE: These parameters are guaranteed by design, but not tested in production.

TABLE 7. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

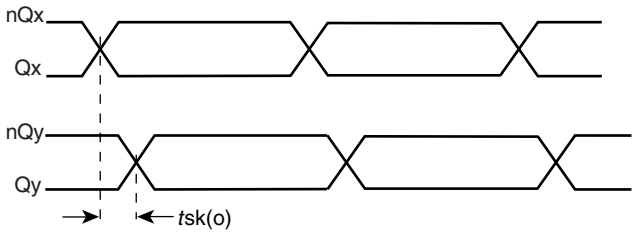
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					400	MHz
t(Ø)	Static Phase Offset; NOTE 1, 5	TEST_CLK		-240	120	0	ps
*t*sk(o)	Output Skew; NOTE 2, 3					250	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 3, 6					350	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 3				±50		ps
f_{VCO}	PLL VCO Lock Range; NOTE 4		VCO_SEL = 0	400		800	MHz
			VCO_SEL = 1	200		400	MHz
t_{LOCK}	PLL Lock Time					10	ms
t_R / t_F	Output Rise/Fall Time		20% to 80%	0.2		1	ns
odc	Output Duty Cycle			45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 2:Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: When VCO_SEL = 0, the PLL will be unstable with feedback configurations of ÷2, ÷4 and some ÷6. When VCO_SEL = 1, the PLL will be unstable with a feedback configuration of ÷2.
NOTE 5: Static phase offset is specified for an input frequency of 50MHz with feedback in ÷8.
NOTE 6: Defined as skew across banks of outputs switching in the same direction operating at different frequencies with the same supply voltages and equal load conditions. Measured at V_{CCO}/2.

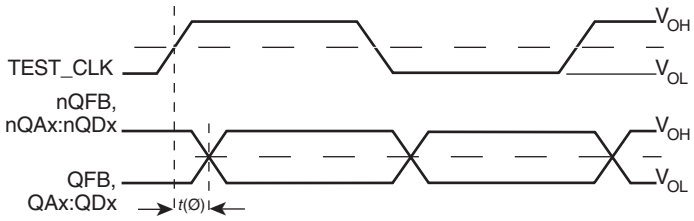
PARAMETER MEASUREMENT INFORMATION



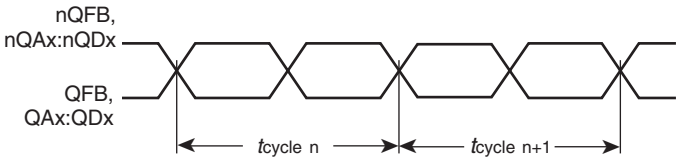
OUTPUT LOAD AC TEST CIRCUIT



OUTPUT SKEW

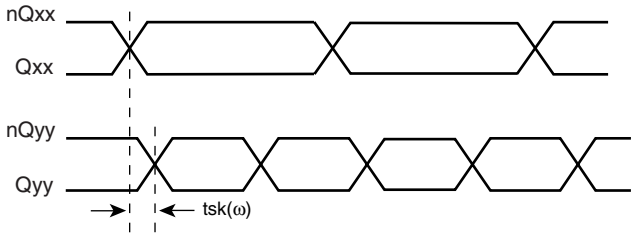


STATIC PHASE OFFSET

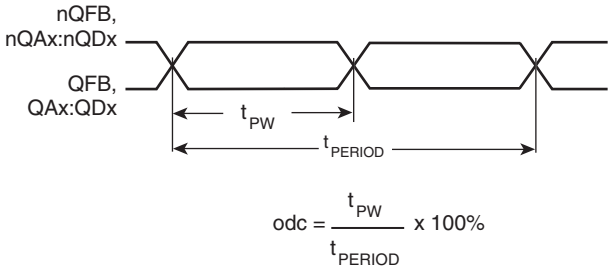


$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$
1000 Cycles

CYCLE-TO-CYCLE JITTER

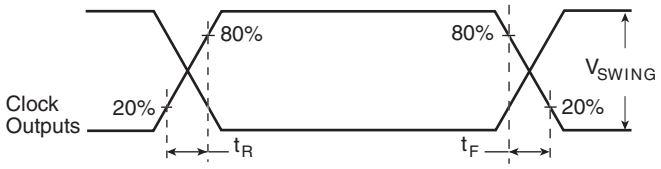


MULTIPLE FREQUENCY SKEW



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS873990 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each V_{CCA} pin.

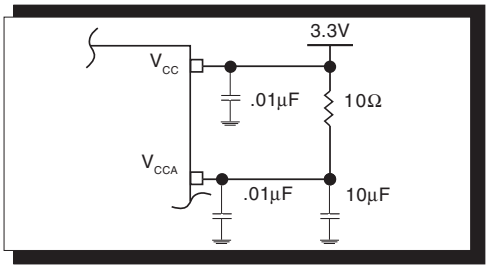


FIGURE 2. POWER SUPPLY FILTERING

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

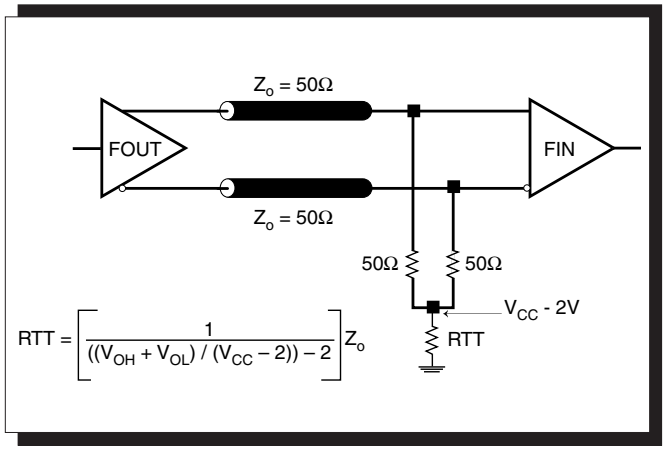


FIGURE 3A. LVPECL OUTPUT TERMINATION

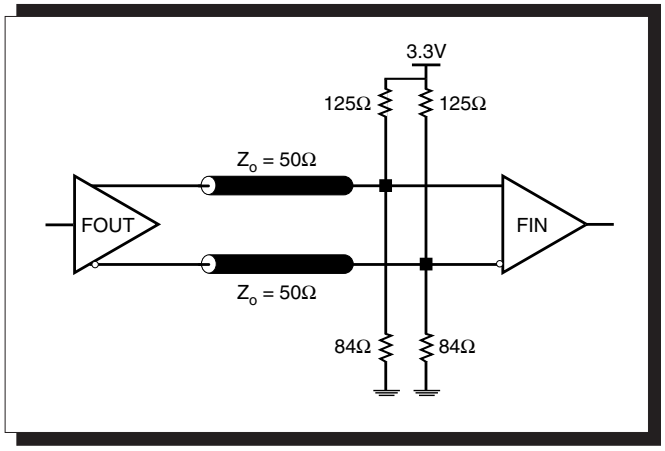


FIGURE 3B. LVPECL OUTPUT TERMINATION

CRYSTAL INPUT INTERFACE

The ICS873990 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 4* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

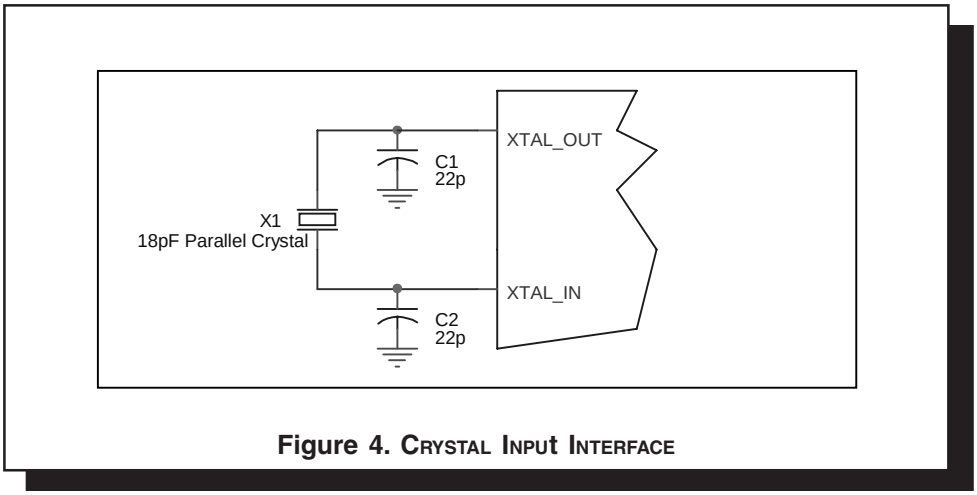


Figure 4. CRYSTAL INPUT INTERFACE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS873990.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS873990 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 165mA = **571.7mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 14 * 30mW = **420mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 571.7mW + 420mW = **991.7mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 47.1°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.992W * 47.1°C/W = 116.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 8. THERMAL RESISTANCE θ_{JA} FOR 52-PIN LQFP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

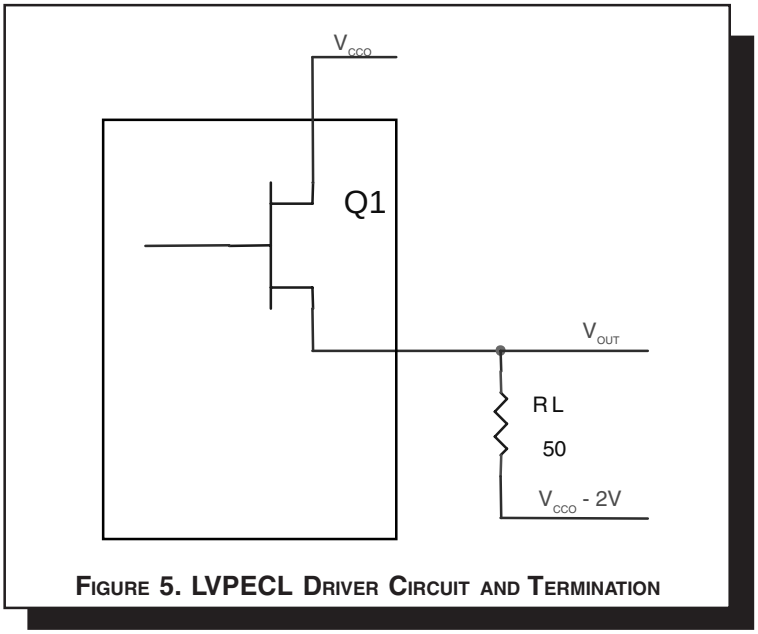


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} – 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 9. θ_{JA} VS. AIR FLOW TABLE FOR 52 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS873990 is: 5788

Pin compatible with the MPC990

PACKAGE OUTLINE - Y SUFFIX FOR 52 LEAD LQFP

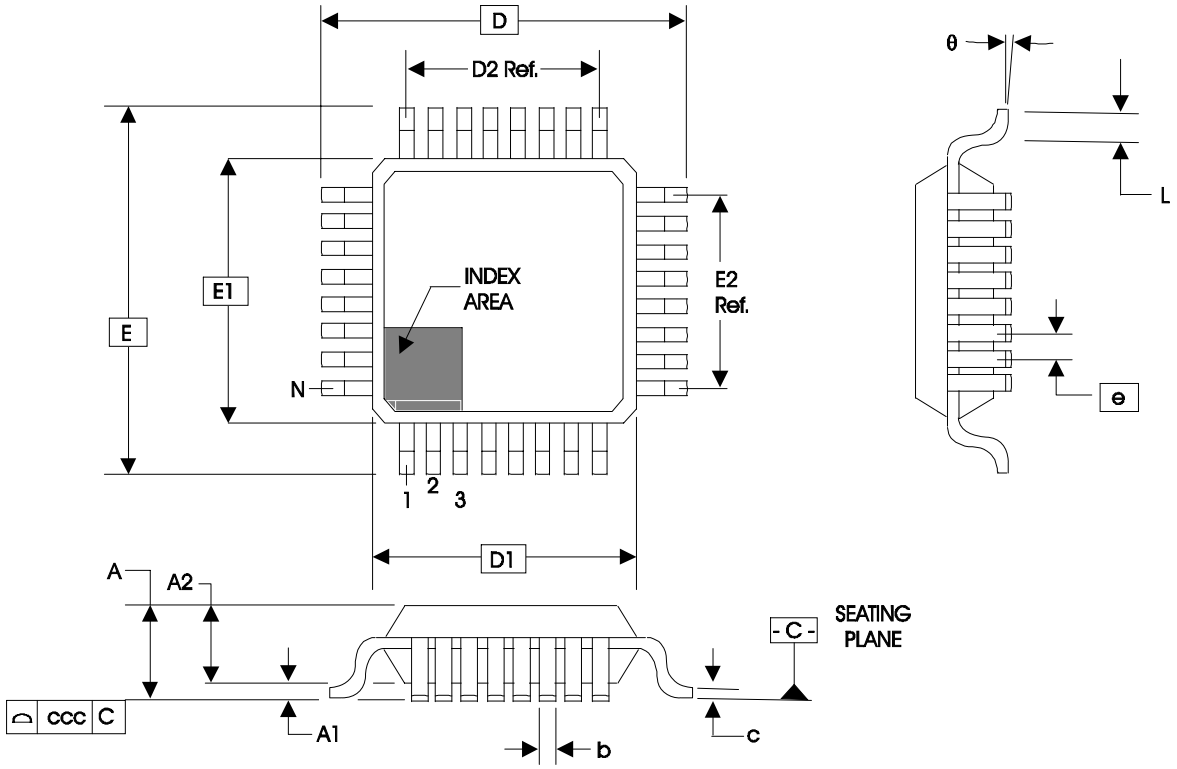


TABLE 10. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N		52	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
c	0.09	--	0.20
D		12.00 BASIC	
D1		10.00 BASIC	
E		12.00 BASIC	
E1		10.00 BASIC	
e		0.65 BASIC	
L	0.45	--	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 11. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS873990AY	ICS873990AY	52 Lead LQFP	tray	0°C to 70°C
ICS873990AYT	ICS873990AY	52 Lead LQFP	500 tape & reel	0°C to 70°C
ICS873990AYLF	TBD	52 Lead "Lead-Free" LQFP	tray	0°C to 70°C
ICS873990AYLFT	TBD	52 Lead "Lead-Free" LQFP	500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T5 T11	1 6 15	Features Section - added Lead-Free bullet. Crystal Characteristics - added Drive Level. Ordering Information Table - added Lead-Free part number and note.	6/13/05