

# IRF2907ZS-7PPbF

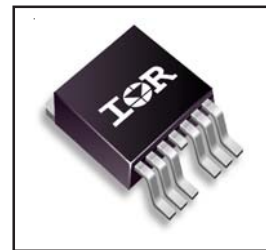
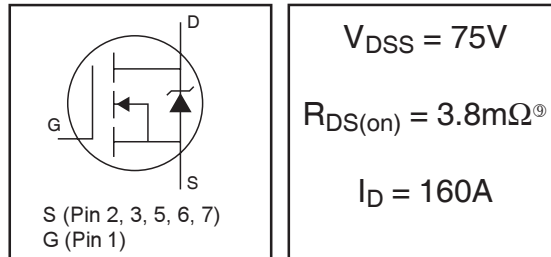
## Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to  $T_{jmax}$

## Description

Specifically designed for high current, high reliability applications, this HEXFET® Power MOSFET utilizes the latest processing techniques and advanced packaging technology to achieve extremely low on-resistance and world-class current ratings. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Server & Telecom OR'ing, Automotive and low voltage Motor Drive Applications.

## HEXFET® Power MOSFET



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	180	A
$I_D @ T_C = 100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$ (See Fig. 9)	120	
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	160	
$I_{DM}$	Pulsed Drain Current ①	700	
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	160	mJ
$E_{AS}$ (tested)	Single Pulse Avalanche Energy Tested Value ③	410	
$I_{AR}$	Avalanche Current ①	See Fig.12a,12b,15,16	A
$E_{AR}$	Repetitive Avalanche Energy ⑤		mJ
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

## Thermal Resistance

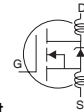
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	0.50	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑧	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑦⑧	—	40	

HEXFET® is a registered trademark of International Rectifier.

www.irf.com

### Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.066	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)SMD}$	Static Drain-to-Source On-Resistance	—	3.0	3.8	m $\Omega$	$V_{GS} = 10V, I_D = 110A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	94	—	—	S	$V_{DS} = 25V, I_D = 110A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 75V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 75V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	170	260	nC	$I_D = 110A$
$Q_{gs}$	Gate-to-Source Charge	—	55	—		$V_{DS} = 60V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	66	—		$V_{GS} = 10V$ ③
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	$V_{DD} = 38V$
$t_r$	Rise Time	—	90	—		$I_D = 110A$
$t_{d(off)}$	Turn-Off Delay Time	—	92	—		$R_G = 2.6\Omega$
$t_f$	Fall Time	—	44	—		$V_{GS} = 10V$ ②
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	7580	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	970	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	540	—		$f = 1.0MHz$ , See Fig. 5
$C_{oss}$	Output Capacitance	—	3750	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
$C_{oss}$	Output Capacitance	—	650	—		$V_{GS} = 0V, V_{DS} = 60V, f = 1.0MHz$
$C_{oss\ eff.}$	Effective Output Capacitance	—	1110	—		$V_{GS} = 0V, V_{DS} = 0V$ to 60V

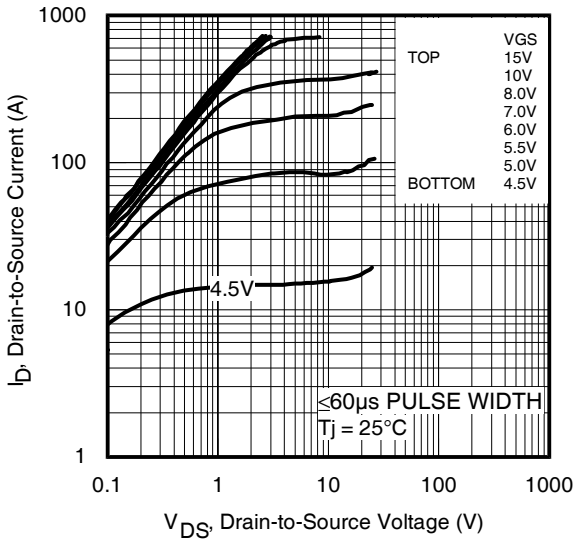


### Diode Characteristics

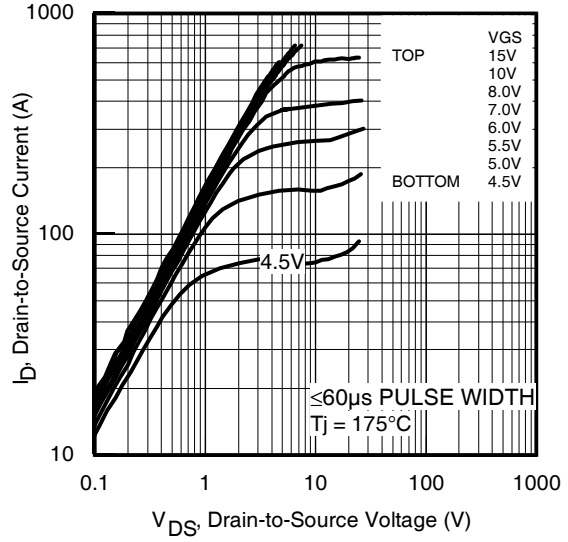
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	160	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	700		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 110A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	35	53	ns	$T_J = 25^\circ\text{C}, I_F = 110A, V_{DD} = 38V$
$Q_{rr}$	Reverse Recovery Charge	—	40	60	nC	$di/dt = 100A/\mu s$ ③

#### Notes:

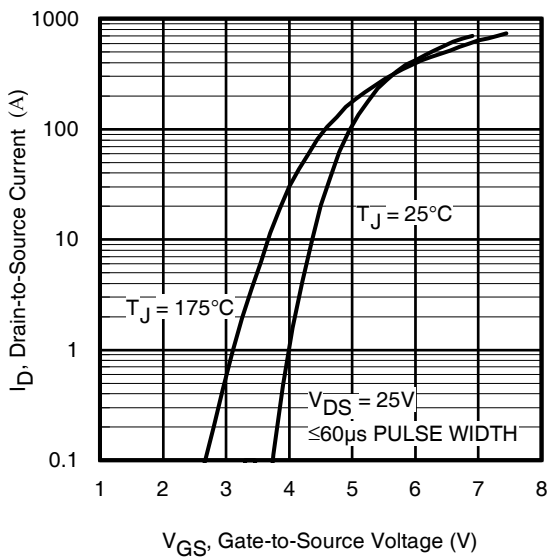
- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.026mH, R_G = 25\Omega, I_{AS} = 110A, V_{GS} = 10V$ . Part not recommended for use above this value.
- ③ Pulse width  $\leq 1.0ms$ ; duty cycle  $\leq 2\%$ .
- ④  $C_{oss\ eff.}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑤ Limited by  $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑨ Solder mounted on IMS substrate.



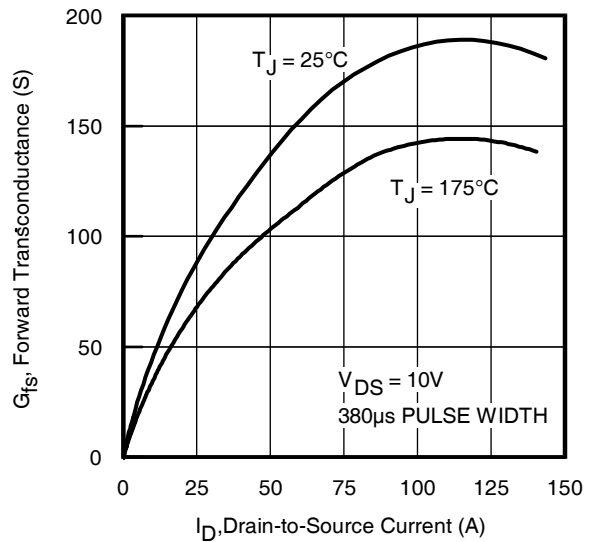
**Fig 1.** Typical Output Characteristics



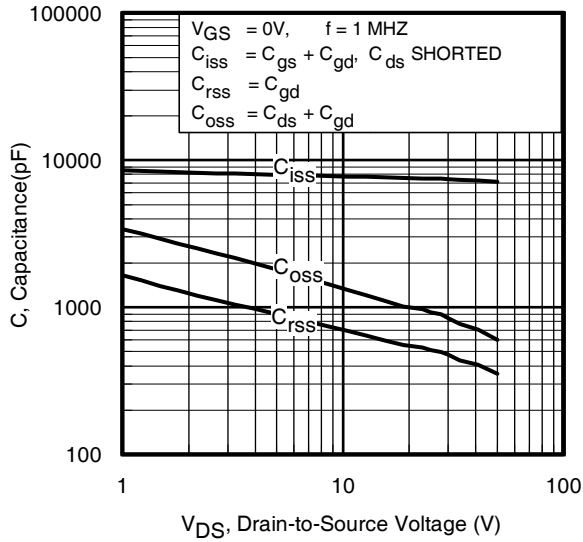
**Fig 2.** Typical Output Characteristics



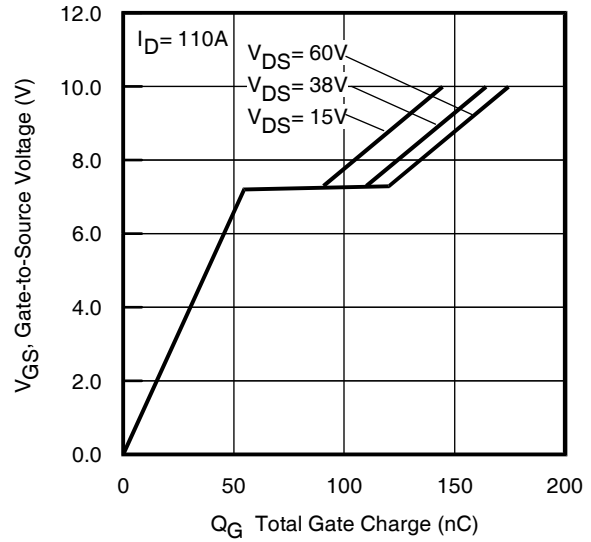
**Fig 3.** Typical Transfer Characteristics



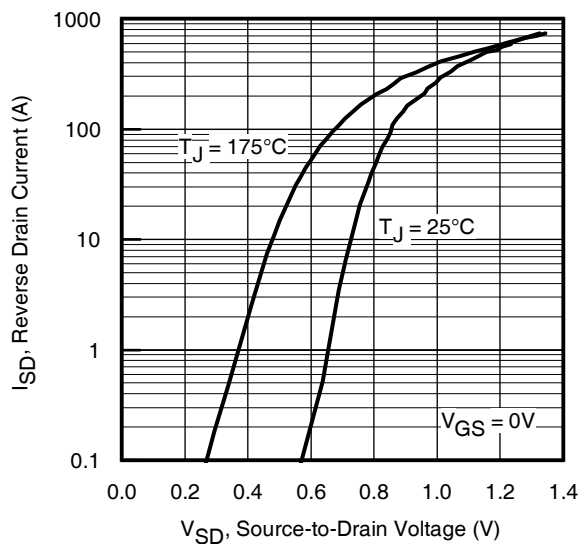
**Fig 4.** Typical Forward Transconductance vs. Drain Current



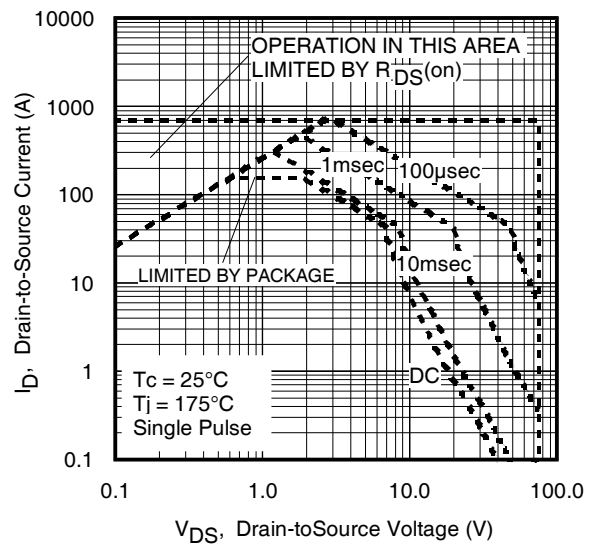
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

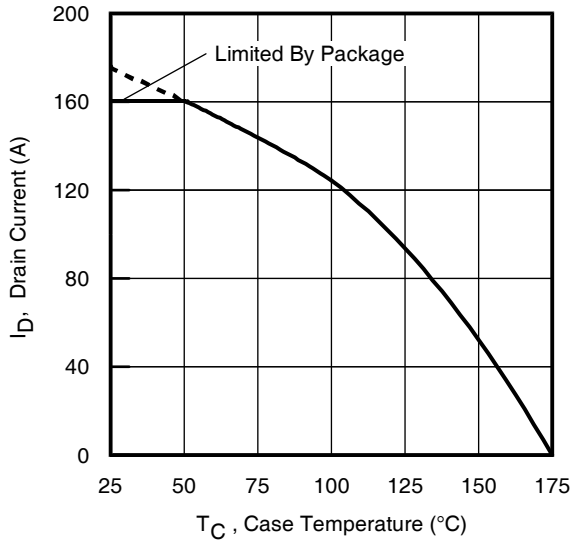


Fig 9. Maximum Drain Current vs. Case Temperature

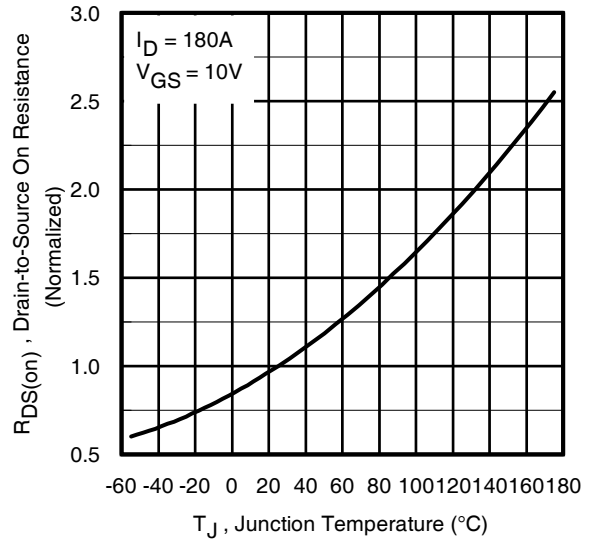


Fig 10. Normalized On-Resistance vs. Temperature

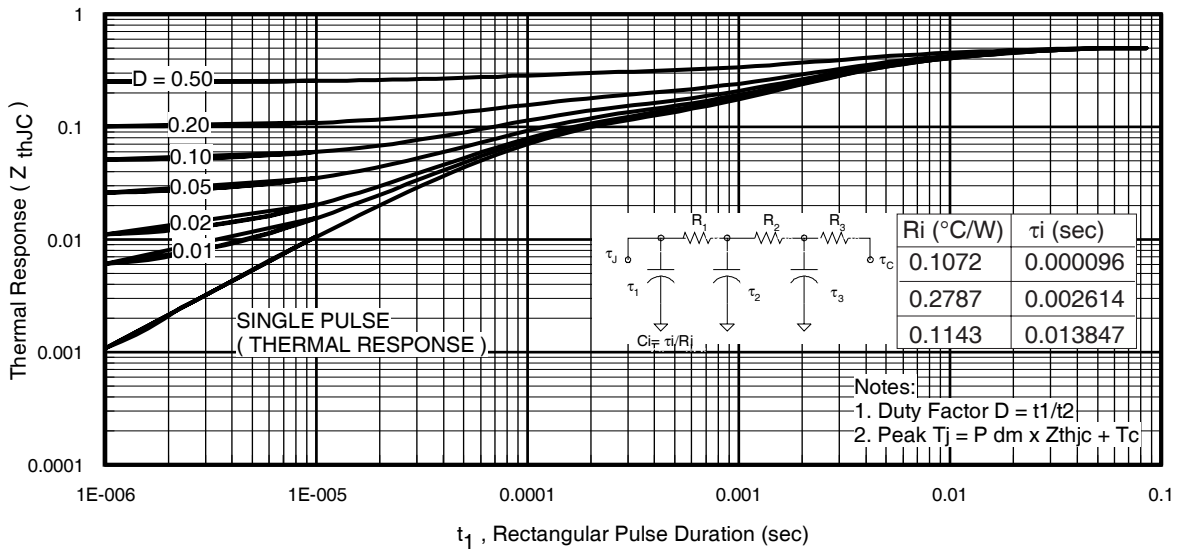


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



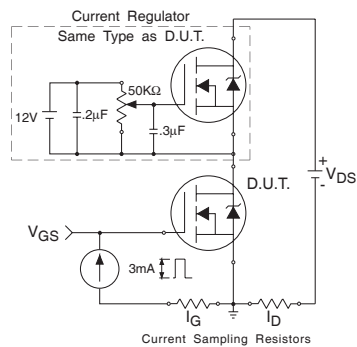
**Fig 12a.** Unclamped Inductive Test Circuit



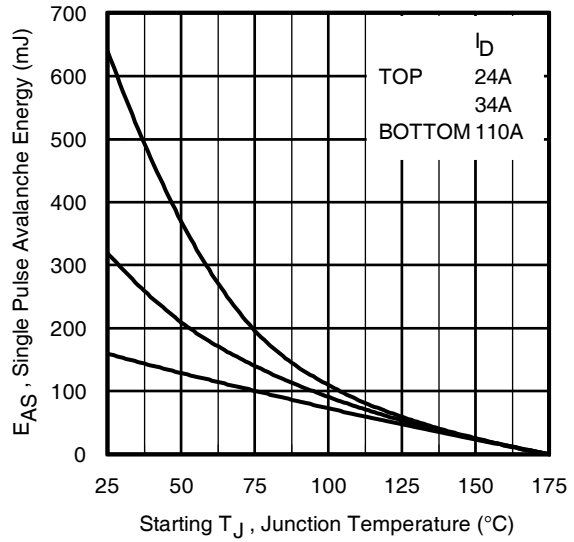
**Fig 12b.** Unclamped Inductive Waveforms



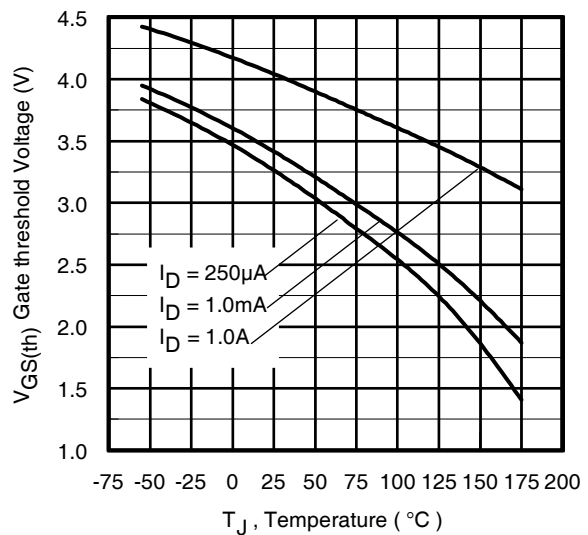
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy vs. Drain Current



**Fig 14.** Threshold Voltage vs. Temperature

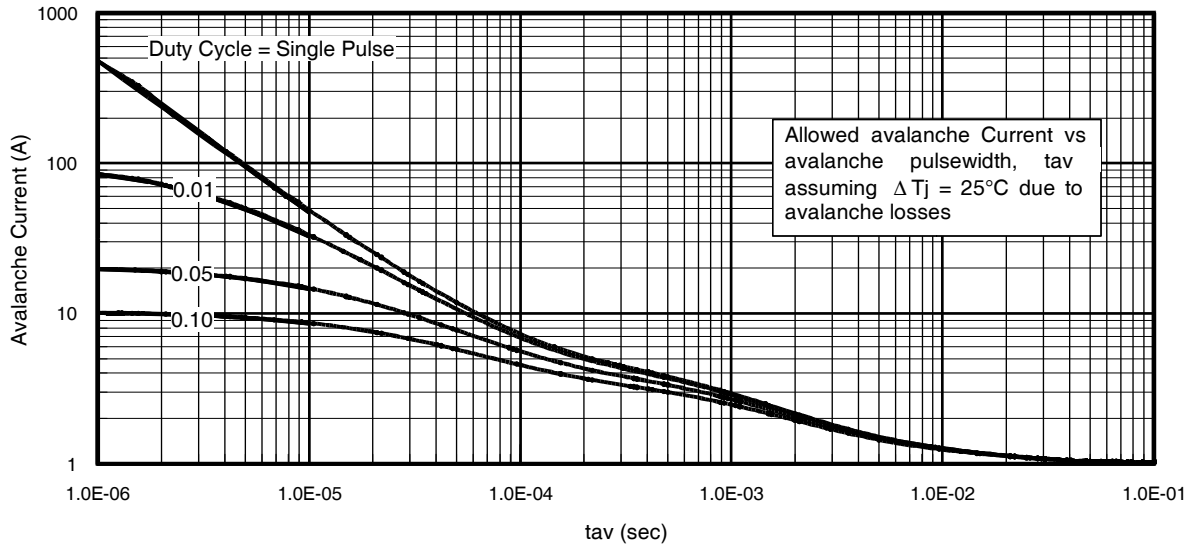


Fig 15. Typical Avalanche Current vs.Pulsewidth

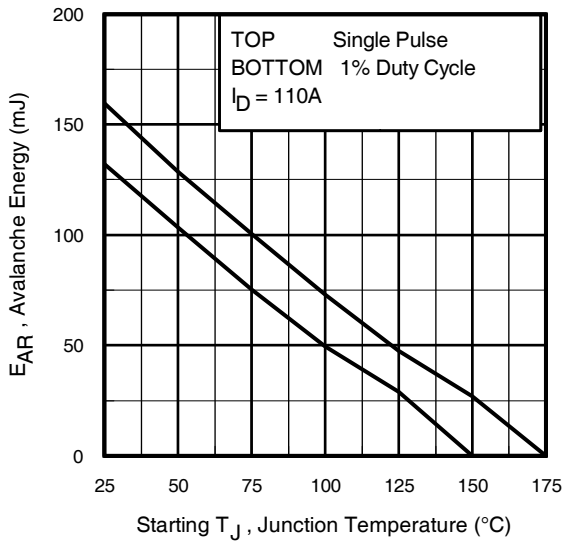


Fig 16. Maximum Avalanche Energy vs. Temperature

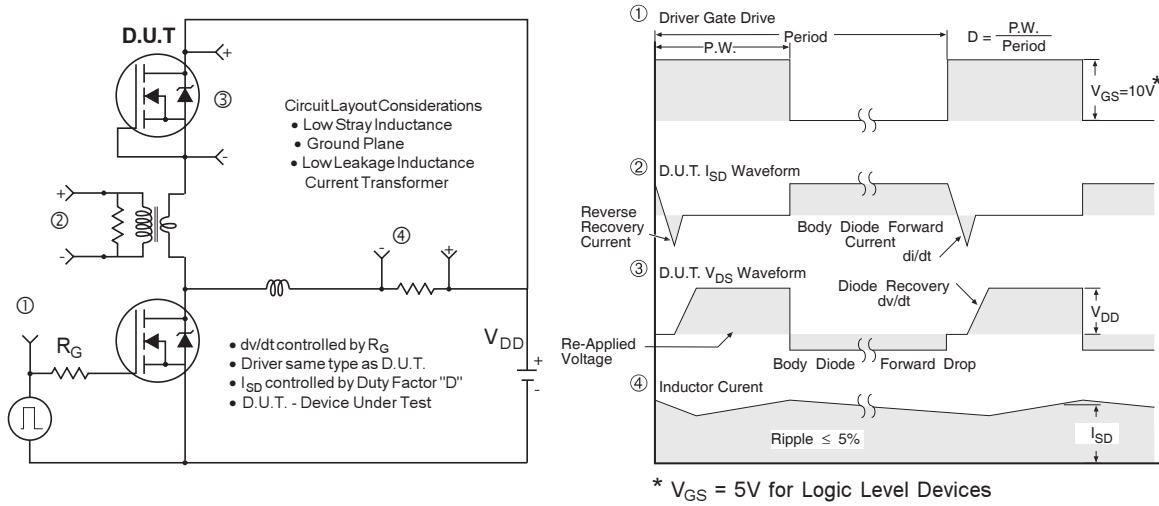
**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

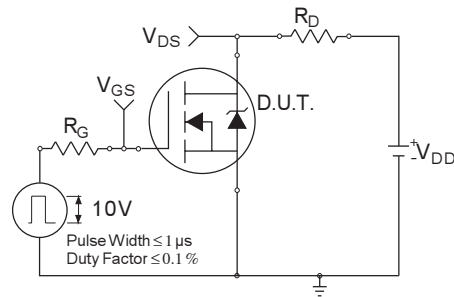
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



**Fig 18a.** Switching Time Test Circuit

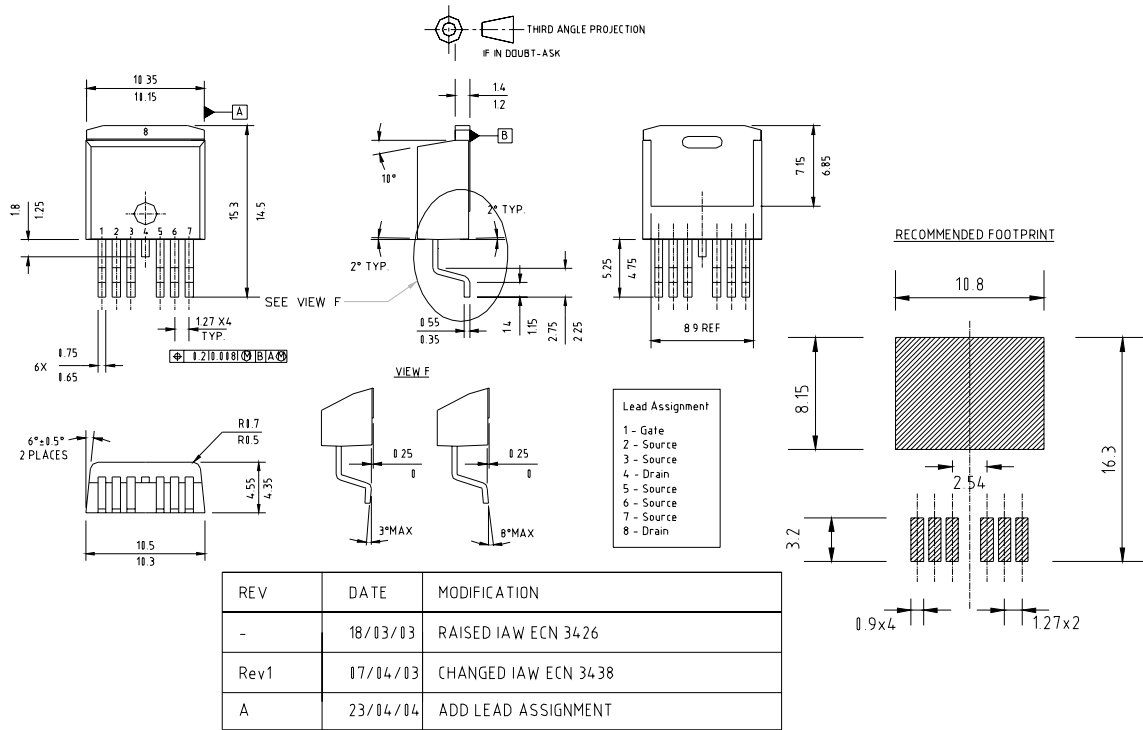


**Fig 18b.** Switching Time Waveforms



## D<sup>2</sup>Pak - 7 Pin Package Outline

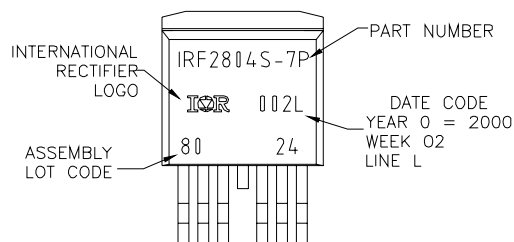
Dimensions are shown in millimeters (inches)



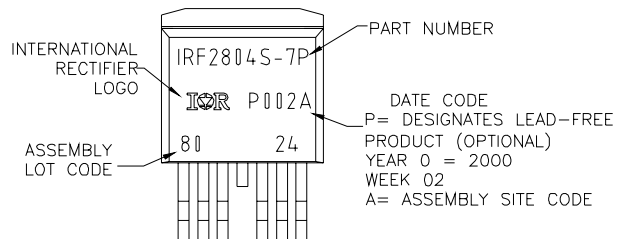
## D<sup>2</sup>Pak - 7 Pin Part Marking Information

EXAMPLE: THIS IS AN IRF2804S-7P WITH LOT CODE 8024 ASSEMBLED ON WW02,2000 IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead Free"



OR

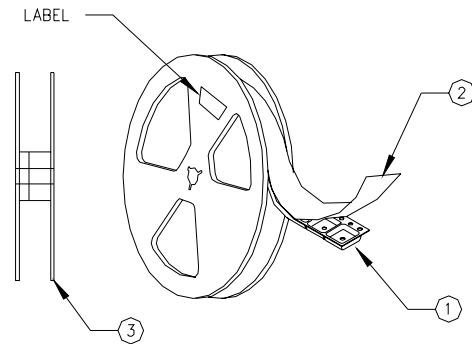
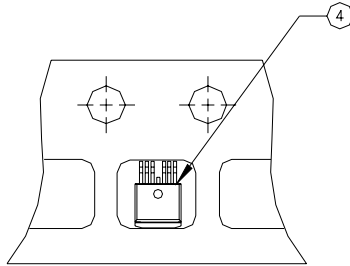


# IRF2907ZS-7PPbF

## D<sup>2</sup>Pak - 7 Pin Tape and Reel

### NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.
  - 1.1 REEL SIZE 13 INCH DIAMETER.
  - 1.2 EACH REEL CONTAINING 800 DEVICES.
  - 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
  - 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
  - 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
  - 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.
2. LABELLING (REEL AND SHIPPING BAG).
  - 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
  - 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
  - 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
  - 2.4 QUANTITY:
  - 2.5 VENDOR CODE: IR
  - 2.6 LOT CODE:
  - 2.7 DATE CODE:



Data and specifications subject to change without notice.  
This product has been designed and qualified for the Automotive [Q101] market.  
Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>