FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12532-2E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89660R Series

MB89663R/665R/P665/W665

■ OUTLINE

The MB89660R series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a great variety of peripheral functions such as timers, a UART, a serial interface, an 8-bit A/D converter, an input capture, an output compare, and an external interrupt. The MB89660R series is applicable to a wide range of applications from consumer products to industrial equipment.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- Packages
  QFP-64
  SH-DIP-64
- F²MC-8L family CPU core

Instruction set optimized for controllers
- Multiplication and division instructions
- 16-bit arithmetic operations
- Test and branch instructions
- Bit manipulation instructions, etc.

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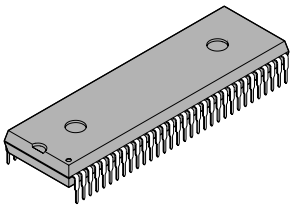
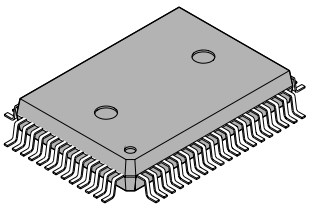
■ PACKAGE

64-pin Plastic SH-DIP



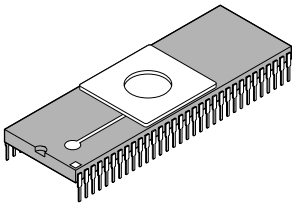
(DIP-64P-M01)

64-pin Plastic QFP



(FPT-64P-M06)

64-pin Ceramic SH-DIP



(DIP-64C-A06)

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- Four types of timers
  8-bit PWM timer
  8/16-bit timer/counter
  20-bit timebase timer
- Functions that permit communications with a variety of devices
  UART which permits selection of synchronous/asynchronous communications
  A serial interface that permits selection of the transfer direction
- 8-bit A/D converter: 8 channels
  Sense function capable of performing voltage compare operation in 5 μs at 10 MHz
  Started by external input possible
- Real-time control
  Input capture: 2 channels
  Output compare: 2 channels
- External interrupt: 4 channels
  Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low power consumption (standby modes)
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
  Hardware standby mode (Wake-up from this mode and activation by pin input only.)

■ PRODUCT LINEUP

Item \ Part number	MB89663R	MB89665R	MB89W665	MB89P665
Classification	Mass-produced products (mask ROM products)		EPROM product	One-time PROM product, also used for evaluation
ROM size	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal PROM, to be programmed with general-purpose EPROM programmer)	
RAM size	256 × 8 bits	512 × 8 bits		
CPU functions	The number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1,8, 16 bits Minimum execution time: 0.4 μs at 10 MHz Interrupt processing time: 3.6 μs at 10 MHz			
Ports	Output ports (CMOS): 8 Output ports (N-ch open-drain): 8 (All also serve as peripherals.) General-purpose I/O ports (CMOS): 36 (19 ports also serve as peripherals.) Total: 52			
8-bit PWM timer	8-bit interval timer operation (square wave output capable, operating clock cycle: 0.4 μs to 25.6 μs) 8-bit resolution PWM operation (conversion cycle: 102 μs to 6.6 ms)			
8/16-bit timer/ counter	2-channel 8-bit timer/counter operation (timer 1 and timer 2, each operating clock independence, square wave output capable), or 16-bit timer/counter operation (operating clock cycle: 0.8 μs to 12.8 μs) In timer 1 or 16-bit timer/counter operation, event counter operation by external clock input			
UART	Variable data length (6-, 7-, 8-bit length), built-in baud rate generator, error detection function, built-in full-duplex double buffer NRZ type transfer format, CLK synchronous/asynchronous data transfer capable Transfer rate setting by dedicated band rate generator, external clock, 8-bit PWM timer			
8-bit serial I/O	8 bits LSB/MSB first selectable One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 0.8 μs, 3.2 μs, 12.8 μs)			
8-bit A/D converter	8-bit resolution × 8 channels A/D conversion function (conversion time: 18 μs at 10 MHz) Sense function (conversion time: 5 μs at 10 MHz) Capable of continuous activation by an external clock or an internal clock Reference voltage input			
Real-time I/O	16-bit timer: operating clock cycle (0.4 μs, 0.8 μs, 1.6 μs, 3.2 μs) overflow interrupt Input capture: 16 bits × 2 channels (External trigger edge selectable) Output capture: 16 bits × 2 channels			

(Continued)

(Continued)

Item \ Part number	MB89663R	MB89665R	MB89W665	MB89P665
External interrupt	4 channels (source flag, enable flag independently) Rising edge/falling edge/both edges selectable Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.) (Wake-up from hardware standby mode is not possible)			
Low-power consumption (standby modes)	Sleep mode, stop mode, and hardware standby mode			
Process	CMOS			
Operating voltage* (when using A/D converter)	2.2 V to 6.0 V (3.5 V to 6.0 V)		2.7 V to 6.0 V (3.5 V to 6.0 V)	

* : Varies with conditions such as the operating frequency. (See section “■ Electrical Characteristics.”)

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89663R MB89665R MB89P665	MB89W665
DIP-64P-M01	○	×
FPT-64P-M06	○	×
DIP-64C-A06	×	○

○ : Available × : Not available

Note: For more information about each package, see section “■ Package Dimensions.”

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the OTPROM (one-time PROM) product (also used for evaluation), verify its differences from the product that will actually be used: Take particular care on the following points:

- On the MB89663R, register bank from 16 to 32 cannot be used.
- On the MB89P665, address $BFF0_H$ to $BFF6_H$ comprise the option setting area, option settings can be read by reading these addresses.
- The stack area, etc., is used.

2. Current Consumption

- When operated at low speed, the product with an OTPROM or an EPROM will consume more current than the product with a mask ROM.
- However, the same is the current comsumption in sleep/stop modes. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics."

3. Mask Options

Functions that can be selected as options and how to designate these options vary with product.

Before using options, check section "■ Mask Options."

Take particular care on the following points:

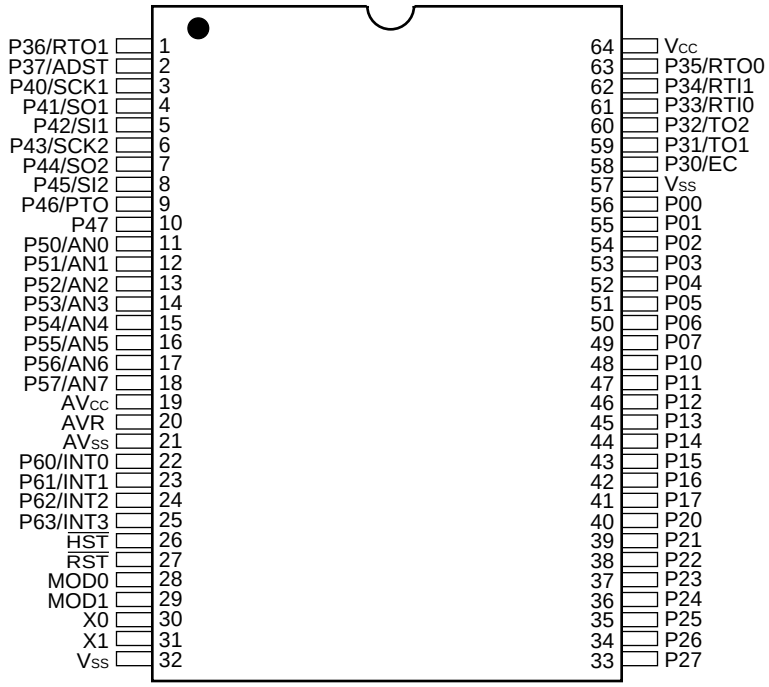
- On the MB89P665, a pull-up resistor must be selected in a group of four pins for P54 to P57.
- For all products, P50 to P57 must be set for no pull-up resistor optional when an A/D converter is used.

4. Differences between the MB89660 and MB89660R Series

- Memory access area
  Memory access area of both the MB89660R and MB89660 series is the same.
- Other Specifications
  For MB89660R series, input level at P00 to P07 and P10 to P17 is fixed when the hardware is standing-by. And for MB89660 series, input level at P00 to P07 and P10 to P17 is not fixed. Therefore, when the medium voltage is input there such as input open, the standby current will increase.
- Electrical specifications/electrical characteristics
  There are differences at pull down resistances of MOD0 and MOD1 between MB89660R series and MB89660 series. For more information, see "3. DC characteristics" in section "■ Electrical Characteristics".
  Electrical specification of the other items of MB89660R series and MB89660 series are equivalent.
  However, it is possible that the valid characteristic will be modified. See the corresponding characteristic respectively for detail.

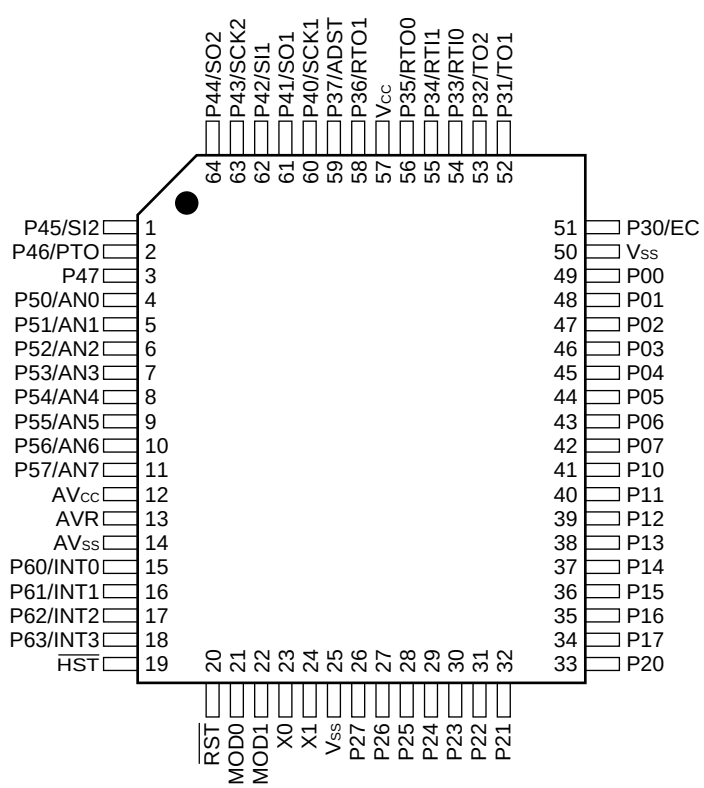
■ PIN ASSIGNMENT

(Top view)



(DIP-64P-M01)
(DIP-64C-A06)

(Top view)



(FPT-64P-M06)

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
SH-DIP*1	QFP*2			
30	23	X0	A	Crystal oscillator pins
31	24	X1		
28	21	MOD0	B	Operation mode select pins Connect directly to V_{CC} or V_{SS}. A pull-down resistor is selectable as an option for mask ROM products.
29	22	MOD1		
27	20	$\overline{RST}$	C	Reset I/O pin This port is an N-ch open-drain output type with pull-up resistor and of hysteresis input type. “L” is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”.
26	19	$\overline{HST}$	G	Hardware standby input pin Connect directly to V_{CC} when hardware standby is not used.
56 to 49	49 to 42	P00 to P07	D	General-purpose I/O ports
48 to 41	41 to 34	P10 to P17		
40 to 33	33 to 26	P20 to P27	F	General-purpose output ports
58	51	P30/EC	E	General-purpose I/O port Also serves as an external clock input for an 8/16-bit timer/counter. This pin is of hysteresis input type and with a noise canceller.
59	52	P31/TO1	E	General-purpose high-current I/O port Also serves as an 8/16-bit timer/counter output. This pin is of hysteresis input type and with a noise canceller.
60	53	P32/TO2	E	General-purpose I/O port Also serves as an 8/16-bit timer/counter output. This pin is of hysteresis input type and with a noise canceller.
61	54	P33/RTI0	E	General-purpose I/O ports Also serve as the data input for the input capture. This pin is of hysteresis input type and with a noise canceller.
62	55	P34/RTI1		
63	56	P35/RTO0	E	General-purpose I/O ports Also serve as the data output for the output compare. This pin is of hysteresis input type and with a noise canceller.
1	58	P36/RTO1		
2	59	P37/ADST	E	General-purpose high-current I/O port Also serves as the external starting input for the A/D converter. This pin is of hysteresis input type and with a noise canceller.

*1: DIP-64P-M01, DIP-64C-A06

*2: FPT-64P-M06

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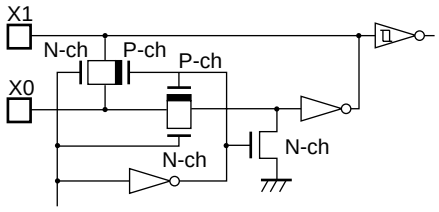
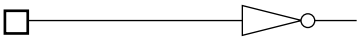
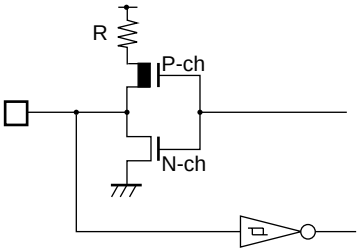
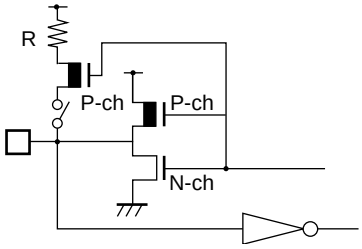
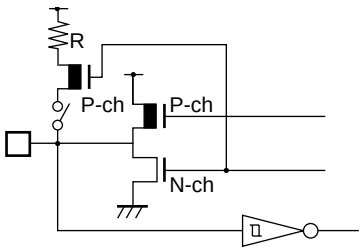
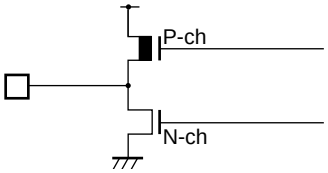
Pin no.		Pin name	Circuit type	Function
SH-DIP*1	QFP*2			
3	60	P40/SCK1	E	General-purpose I/O port Also serves as the clock I/O for the UART. This pin is of hysteresis input type and with a noise canceller.
4	61	P41/SO1	E	General-purpose I/O port Also serves as the data output for the UART. This pin is of hysteresis input type and with a noise canceller.
5	62	P42/SI1	E	General-purpose I/O port Also serves as the data input for the UART. This pin is of hysteresis input type and with a noise canceller.
6	63	P43/SCK2	E	General-purpose I/O port Also serves as the clock I/O for the 8-bit serial I/O interface. This pin is of hysteresis input type and with a noise canceller.
7	64	P44/SO2	E	General-purpose I/O port Also serves as the data output for the 8-bit serial I/O interface. This pin is of hysteresis input type and with a noise canceller.
8	1	P45/SI2	E	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O interface. This pin is of hysteresis input type and with a noise canceller.
9	2	P46/PTO	E	General-purpose I/O port Also serves as a toggle output for an 8-bit PWM timer. This pin is of hysteresis input type and with a noise canceller.
10	3	P47	E	General-purpose I/O port This pin is of hysteresis input type and with a noise canceller.
11 to 18	4 to 11	P50/AN0 to P57/AN7	H	N-ch open-drain output ports Also serve as the analog input for the A/D converter.
22 to 25	15 to 18	P60/INT0 to P63/INT3	E	General-purpose I/O ports These pins also serve as an external interrupt input. These pins are of hysteresis input type and with a noise canceller.
64	57	V_{CC}	—	Power supply pin
32 57	25 50	V_{SS}	—	Power supply (GND) pins
19	12	AV_{CC}	—	A/D converter power supply pin
20	13	AVR	—	A/D converter reference voltage input pin
21	14	AV_{SS}	—	A/D converter power supply pin Use this pin at the same voltage as V_{SS}.

*1: DIP-64P-M01, DIP-64C-A06

*2: FPT-64P-M06

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistor of approximately 1 MΩ at 5.0 V
B		• CMOS input • Built-in pull-down resistor (mask ROM products only)
C		• Output pull-up resistor (P-ch) of approximately 50 kΩ at 5.0 V • Hysteresis input
D		• CMOS output • CMOS input • Pull-up resistor option of approximately 50 kΩ at 5.0 V
E		• CMOS output • Hysteresis input • Pull-up resistor option of approximately 50 kΩ at 5.0 V
F		• CMOS output

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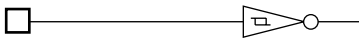
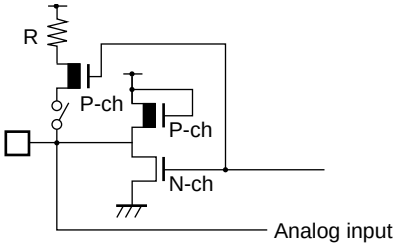
Type	Circuit	Remarks
G		• Hysteresis input
H		• N-ch open-drain output • Analog input • Pull-up resistor option of approximately 50 kΩ at 5.0 V

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “ ■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D Converters

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ if the A/D converters are not in use.

4. Power Supply Voltage Fluctuations

Although operation is assured within the rated range of V_{CC} power supply voltage, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency(50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

5. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P665

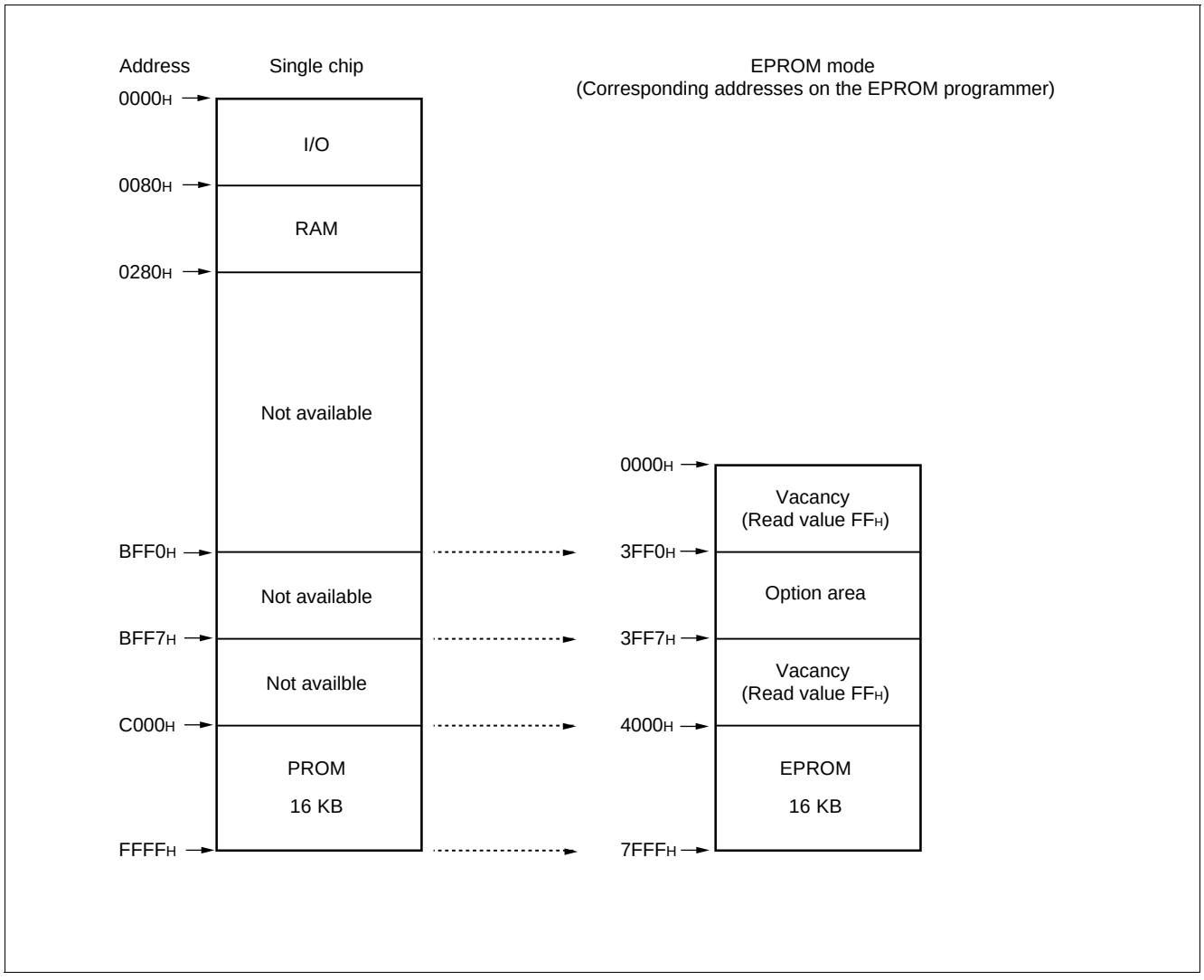
The MB89P665 is an OTPROM version of the MB89660R series.

1. Features

- 16-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in each mode such as 16-Kbyte PROM, option area is diagrammed below.



3. Programming to the PROM

In EPROM mode, the MB89P665A functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

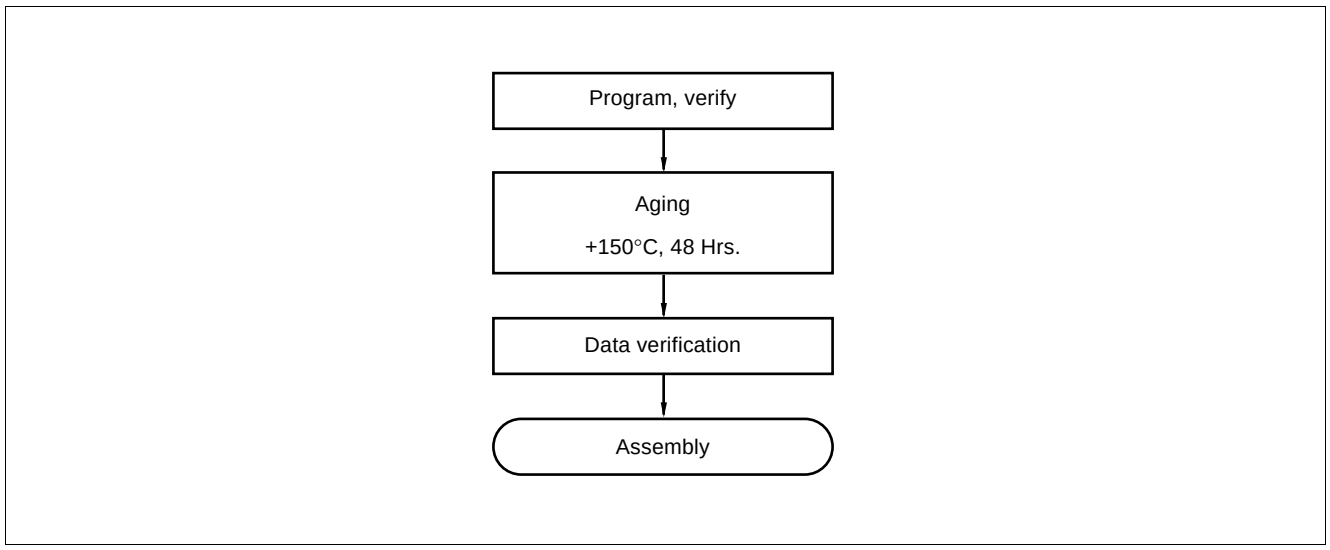
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 4000_H to $7FFF_H$ (note that addresses $C000_H$ to $FFFF_H$ while operating as a single chip correspond to 4000_H to $7FFF_H$ in EPROM mode).
Load option data into addresses $3FF0_H$ to $3FF6_H$ of the EPROM programmer. (For information about each corresponding option, see “8. Setting OTPROM Options.”)

(3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

Due to its nature, bit programming test can't be conducted as Fujitsu delivery test. For this reason, a programming yield of 100% cannot be assured at all times.

6. Erasure Procedure

In order to clear all locations of their programmed contents, it is necessary to expose the internal EPROM to an ultraviolet light source. A dosage of 10 W-seconds/cm^2 is required to completely erase an internal EPROM. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000 μW/cm^2 for 15 to 21 minuites. The internal EPROM should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the internal EPROM and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure time will be much longer than with UV source at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the internal EPROM, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

7. EPROM Programmer Socket Adapter and Recommended Programmer Manufacturer

Part number	Package	Compatible socket adapter Sun Hayato Co., Ltd.	Recommended programmer manufacturer and programmer name			
			Minato Electronics Inc.			Data I/O Co., Ltd.
			1890A	1891	1930	R4945A
MB89W665	SH-DIP-64	ROM-64QF-28DP-8L5	—			—
MB89P665PF	QFP-64	ROM-64QF-28DP-8L	Recommended			Recommended
MB89P665	SH-DIP-64	ROM-64SD-28DP-8L	—			—

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106
Minato Electronics Inc.: TEL: USA (1)-916-348-6066
JAPAN (81)-45-591-5611
Data I/O Co., Ltd.:TEL: USA/ASIA (1)-206-881-6444
EUROPE (49)-8-985-8580

Note: Connect the adapter jumper pin to V_{SS} when using.

8. Setting OTPROM Options

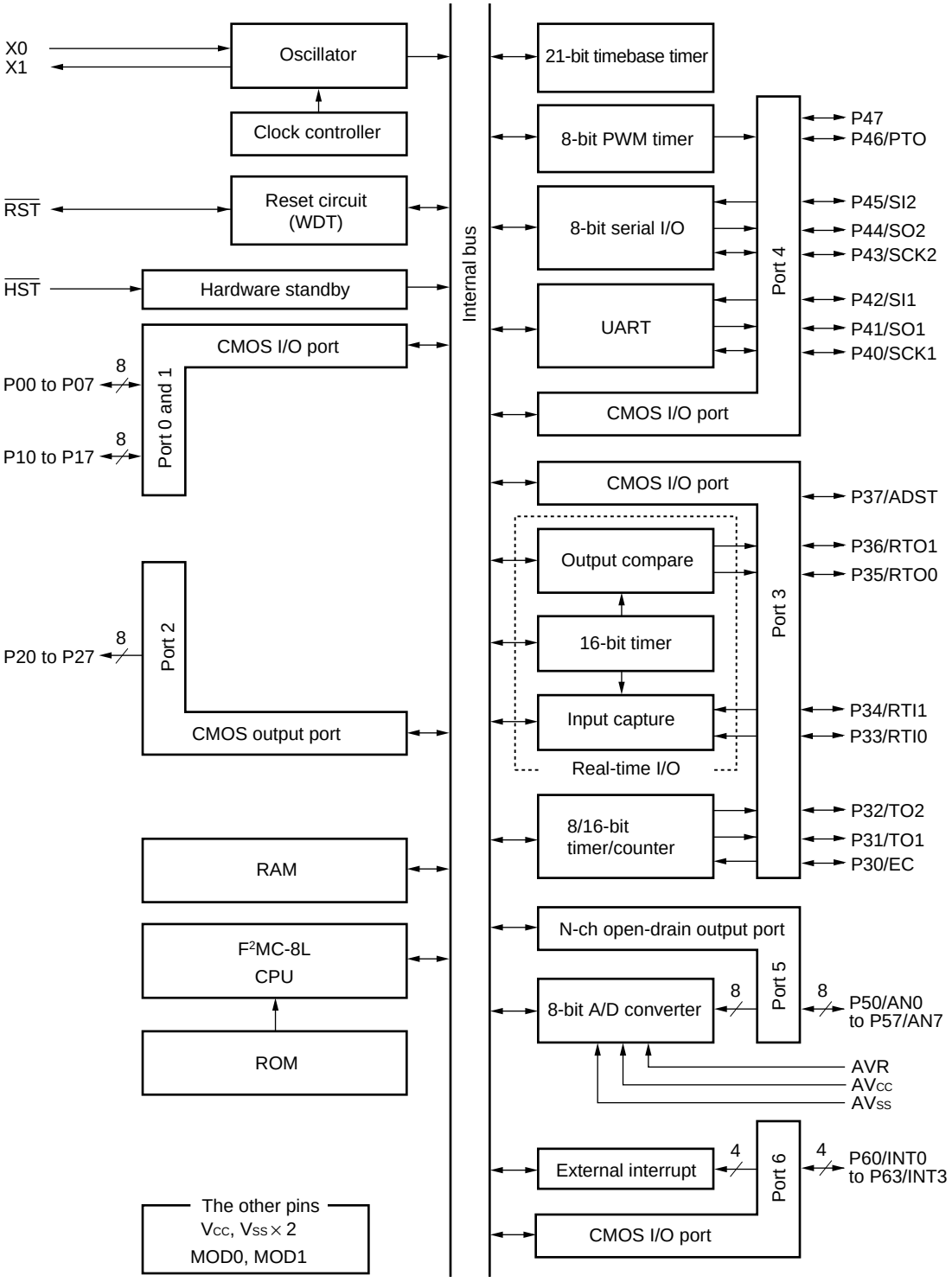
The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

- **OTPROM option bit map**

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FF0H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Oscillation stabilization time 1: Crystal 0: Ceramic	Reset pin output 1: Yes 0: No	Power-on reset 1: Yes 0: No	Vacancy Readable and writable	Vacancy Readable and writable
3FF1H	P07 Pull-up 1: No 1: Yes	P06 Pull-up 1: No 1: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
3FF2H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
3FF3H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
3FF4H	P47 Pull-up 1: No 0: Yes	P46 Pull-up 1: No 0: Yes	P45 Pull-up 1: No 0: Yes	P44 Pull-up 1: No 0: Yes	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes
3FF5H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P57 to P54 Pull-up 1: No 0: Yes	P53 Pull-up 1: No 0: Yes	P52 Pull-up 1: No 0: Yes	P51 Pull-up 1: No 0: Yes	P50 Pull-up 1: No 0: Yes
3FF6H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P63 Pull-up 1: No 0: Yes	P62 Pull-up 1: No 0: Yes	P61 Pull-up 1: No 0: Yes	P60 Pull-up 1: No 0: Yes

Note: • Each bit is set to '1' as the initialized value, therefore the pull-up option is not selected.
• Do not write 0 to the vacant bit.
The read value of the vacant bit is 1, unless 0 is written to it.

■ BLOCK DIAGRAM

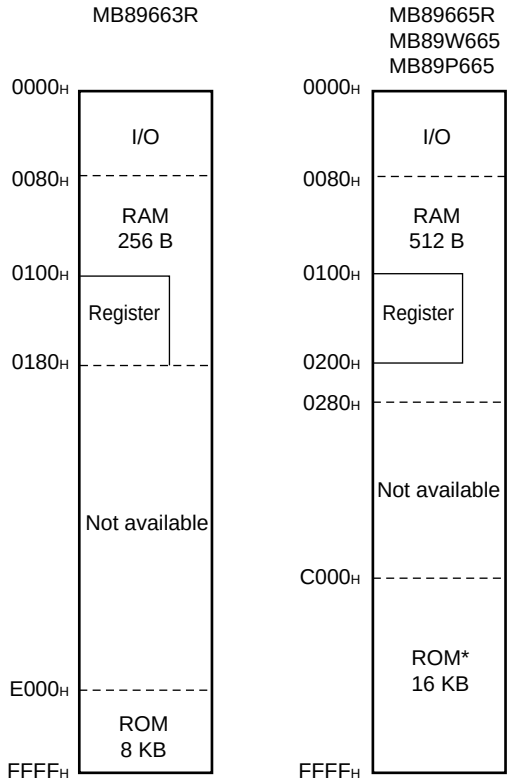


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89660R series offer 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is allocated from the lowest address. The data area is allocated immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is allocated from exactly the opposite end, that is, near the highest address. The tables of interrupt reset vectors and vector call instructions are allocated from the highest address within the program area. The memory space of the MB89660R series is structured as illustrated below.

Memory Space

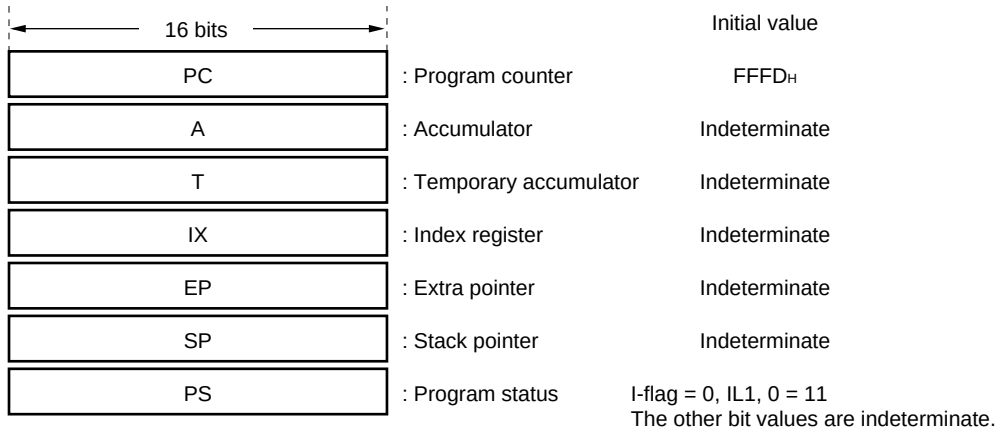


*: When the MB89P665 is used for evaluation, the internal ROM cannot be used.

2. Registers

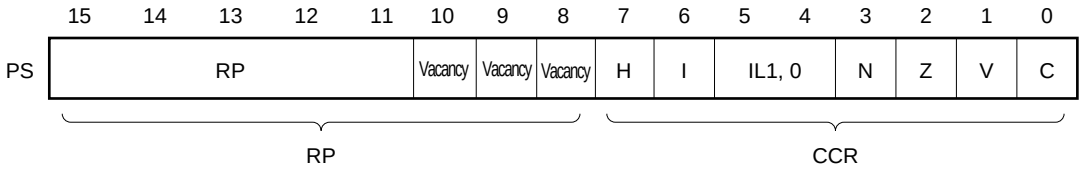
The F²MC-8L family has two types of registers; dedicated hardware registers in the CPU and general-purpose memory registers. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating the instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which is used for arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit pointer for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



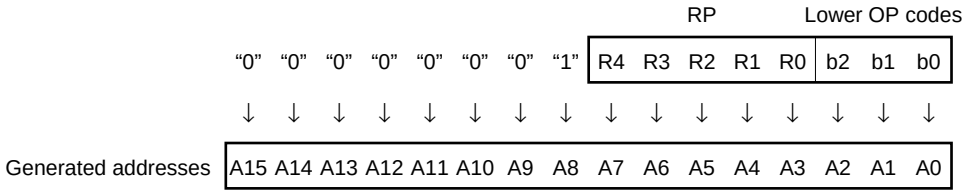
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

• Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

- **Rule for Conversion of Actual Addresses of the General-purpose Register Area**



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data, and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low

N-flag: Set to '1' if the MSB becomes '1' as the result of an arithmetic operation. Cleared to '0' otherwise.

Z-flag: Set to '1' when an arithmetic operation results in 0. Cleared to '0' otherwise.

V-flag: Set to '1' if the complement on '2' overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. Set to the shift-out value in the case of a shift instruction.

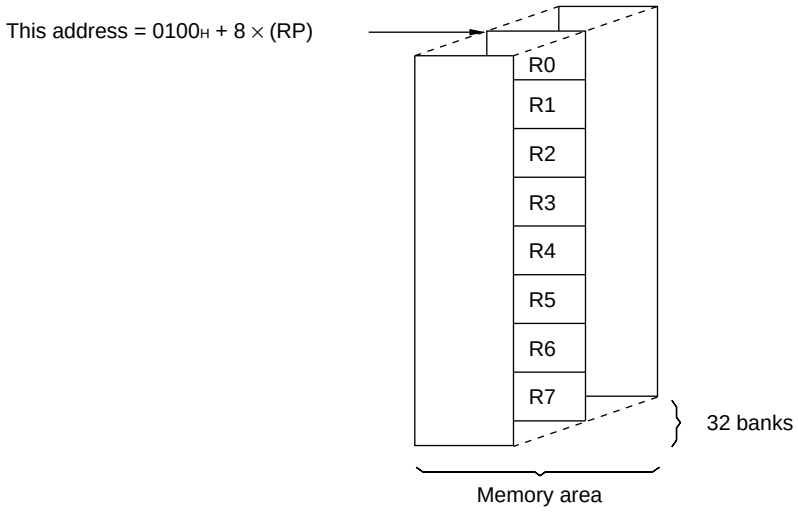
The following general-purpose registers are provided:

General-purpose registers: an 8-bit register for storing data

The general-purpose registers are of 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 16 banks can be used on the MB89663R and a total of 32 banks can be used on the MB89665R/P665/W665. The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size.

- **Register Bank Configuration**



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H			Vacancy
06H			Vacancy
07H			Vacancy
08H	(R/W)	STBC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBTC	Timebase timer control register
0BH			Vacancy
0CH	(R/W)	PDR3	Port 3 data register
0DH	(W)	DDR3	Port 3 data direction register
0EH	(R/W)	PDR4	Port 4 data register
0FH	(W)	DDR4	Port 4 data direction register
10H	(R/W)	PDR5	Port 5 data register
11H			Vacancy
12H	(R/W)	PDR6	Port 6 data register
13H	(W)	DDR6	Port 6 data direction register
14H			Vacancy
15H	(R/W)	ADC1	A/D converter control register 1
16H	(R/W)	ADC2	A/D converter control register 2
17H	(R/W)	ADCD	A/D converter data register
18H	(R/W)	T2CR	Timer 2 control register
19H	(R/W)	T1CR	Timer 1 control register
1AH	(R/W)	T2DR	Timer 2 data register
1BH	(R/W)	T1DR	Timer 1 data register
1CH	(R/W)	CNTR	PWM control register
1DH	(W)	COMR	PWM compare register
1EH			Vacancy
1FH			Vacancy

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20H	(R/W)	SMC	UART serial mode control register
21H	(R/W)	SRC	UART serial rate control register
22H	(R/W)	SSD	UART serial status/data register
23H	(R/W)	SIDR/SODR	UART serial data register
24H	(R/W)	SMR	Serial mode register
25H	(R/W)	SDR	Serial data register
26H	(R/W)	EIC1	External interrupt control register 1
27H	(R/W)	EIC2	External interrupt control register 2
28H	(R/W)	TMCR	Timer control register
29H	(R)	TCHR	Timer count register (H)
2AH	(R)	TCLR	Timer count register (L)
2BH	(R/W)	OPCR	Output control register
2CH	(R/W)	CPR0H	Output compare register 0 (H)
2DH	(R/W)	CPR0L	Output compare register 0 (L)
2EH	(R/W)	CPR1H	Output compare register 1 (H)
2FH	(R/W)	CPR1L	Output compare register 1 (L)
30H	(R/W)	ICCR	Input capture control register
31H	(R/W)	ICIC	Input capture interrupt control register
32H	(R)	ICR0H	Input capture register 0 (H)
33H	(R)	ICR0L	Input capture register 0 (L)
34H	(R)	ICR1H	Input capture register 1 (H)
35H	(R)	ICR1L	Input capture register 1 (L)
36H			Vacancy
37H			Vacancy
38H			Vacancy
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH			Vacancy

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	*
	AVR	V_{SS} – 0.3	V_{SS} + 7.0	V	AVR must not exceed "AV_{CC} + 0.3 V"
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
"L" level maximum output current	I_{OL}	—	20	mA	
"L" level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	40	mA	Average value (operating current × operating rate)
"H" level maximum output current	I_{OH}	—	–20	mA	
"H" level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
"H" level total maximum output current	ΣI_{OH}	—	–50	mA	
"H" level total average output current	ΣI_{OHAV}	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : Use AV_{CC} and V_{CC} set to the same voltage.
Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

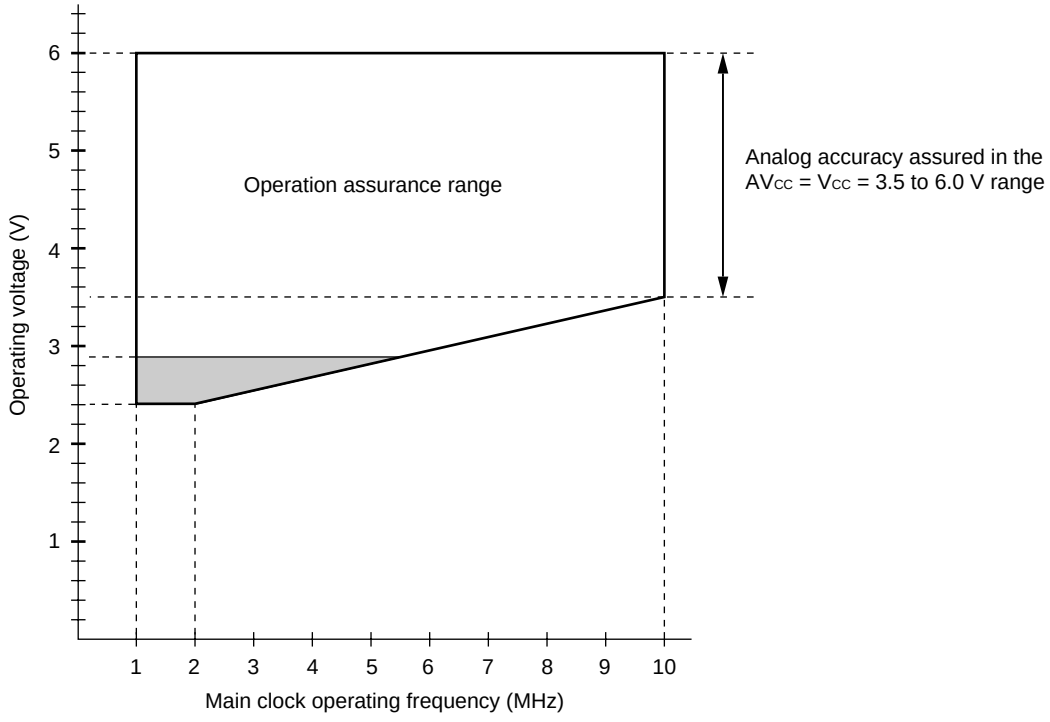
2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	2.2*	6.0*	V	Normal operation assurance range* MB89663R/665R
		2.7*	6.0*	V	Normal operation assurance range* MB89P665
		1.5	6.0	V	Retains the RAM state in the stop mode
	AVR	0.0	AV_{CC}	V	
Operating temperature	T_A	–40	+85	°C	

* : These values vary with the operating frequency and analog assurance range. See Figure. 1 and “5. A/D Converter Electrical Characteristics.”

• **Figure 1 Operating Voltage vs. Main Clock Operating Frequency (MHz)**



Note: The shaded area is assured only for the MB89663R/665R.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC characteristics

(AV_{CC} = V_{CC} = +5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, $\overline{HST}$ P30 to P37, P40 to P47, P60 to P63	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage[*1]	V_{IL}	P00 to P07, P10 to P17	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, $\overline{HST}$ P30 to P37, P40 to P47, P60 to P63	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin applied voltage	V_D	P50 to P57	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
"H" level output voltage	V_{OH1}	P00 to P07, P10 to P17, P20 to P27, P30, P32 to P36, P40 to P47, P60 to P63	I_{OH} = –2.0 mA	2.4	—	—	V	
	V_{OH2}	P31, P37	I_{OH} = –15 mA	2.4	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P27, P30, P32 to P36, P40 to P47, P50 to P57, P60 to P63	I_{OL} = +1.8 mA	—	—	0.4	V	
	V_{OL2}	P31, P37	I_{OL} = +12 mA	—	—	0.4	V	
	V_{OL3}	$\overline{RST}$	I_{OL} = +4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P63	0.45 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULU}	$\overline{RST}$, option select pin	V_I = 0.0 V	25	50	100	kΩ	

(Continued)

(Continued)

(AV_{CC} = V_{CC} = +5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Pull-down resistance	R_{PULD}	MOD0, MOD1	V_I = +5.0 mA	25	50	100	kΩ	Mask ROM products only
Power supply current	I_{CC}	V_{CC}	F_C = 10 MHz t_{inst}*3 = 0.4 µs in the Normal mode	—	15	18	mA	MB89663R/ 665R
				—	17	20	mA	MB89P665/ W665
	I_{CCS}		F_C = 10 MHz t_{inst}*3 = 0.4 µs in the Sleep mode	—	6	8	mA	
	I_{CCH}		T_A = +25°C t_{inst}*3 = 0.4 µs in the Stop mode	—	—	10	µA	
	I_A	AV_{CC}	F_C = 10 MHz, when A/D conversion is operating	—	2.5	4.5	mA	
	I_{AH}		F_C = 10 MHz, T_A = +25°C, when A/D conversion is not operating	—	—	5	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: Fix MOD0 and MOD1 to V_{SS}.

*2: The power supply current is measured on the external clock at "V_{CC} = 5.0 V".

*3: For information on t_{inst}, see "(4) Instruction Cycle" in "4. AC Characteristics."

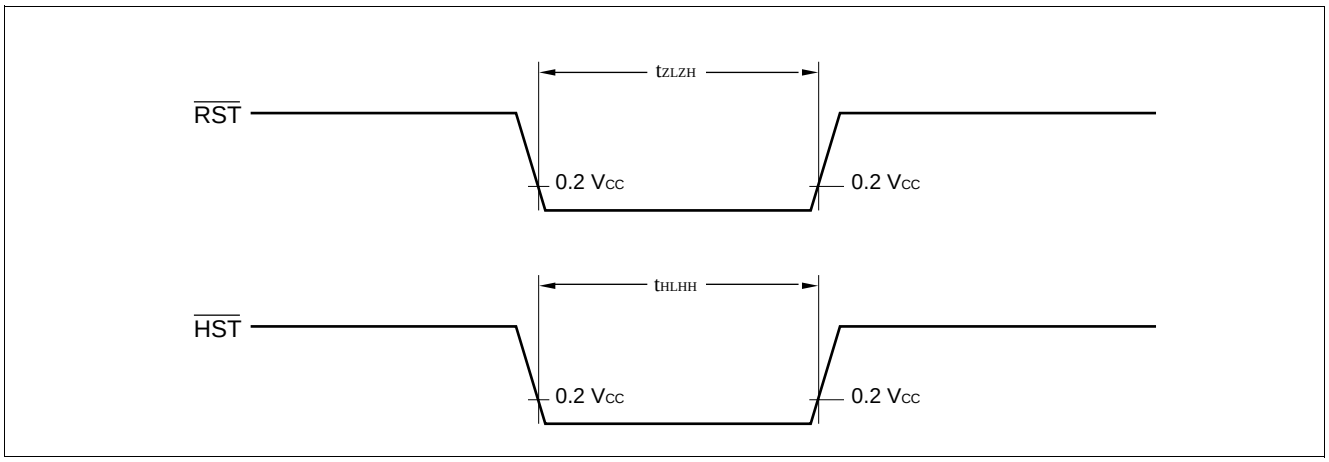
4. AC Characteristics

(1) Reset Timing, Hardware Standby Timing

(V_{CC} = +5.0 V±10%, AV_{SS} =V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	16 t_{XCYL}	—	ns	
$\overline{HST}$ "L" pulse width	t_{HLHH}		16 t_{XCYL}	—	ns	

* : t_{XCYL} is the oscillation cycle (1/F_C) to input to the X0 pin.

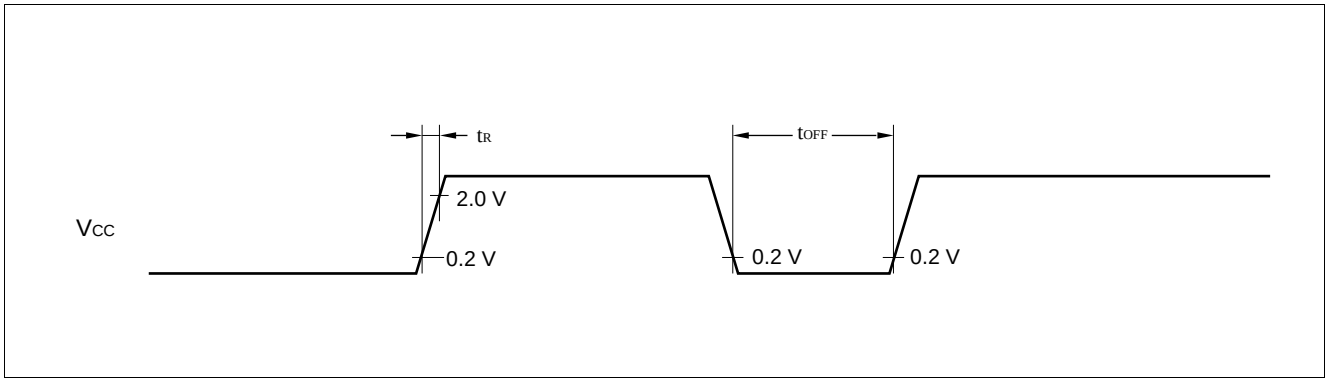


(2) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Values		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the oscillation stabilization time selected.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

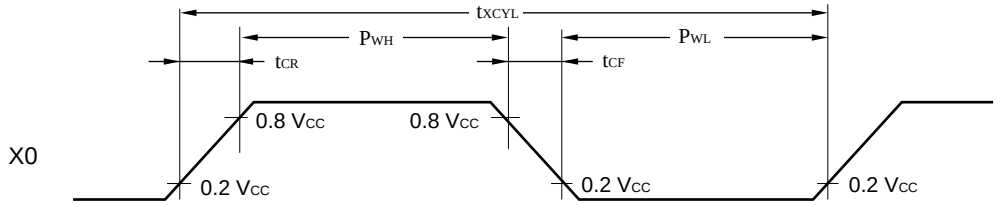


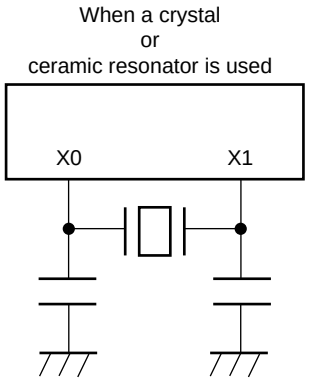
(3) Clock Timing

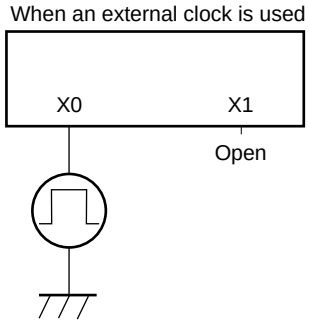
(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_C	X0, X1	—	1	—	10	MHz	
Clock cycle time	t_{XCYL}	X0, X1	—	100	—	1000	ns	
Input clock pulse width	P_{WH} P_{WL}	X0	—	20	—	—	ns	External clock
Input clock rising/ falling time	t_{CR} t_{CF}	X0	—	—	—	10	ns	External clock

X0 and X1 Timing and Conditions of Applied Voltage







(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_C$	µs	When operating at "F_C = 10 MHz"

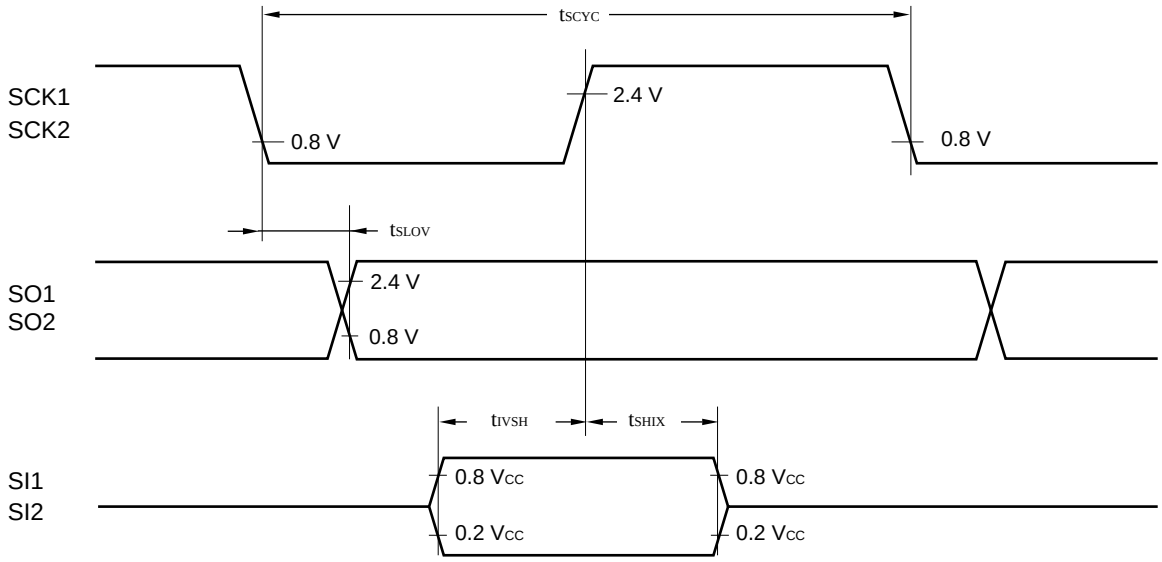
(5) Serial I/O Timing and UART Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

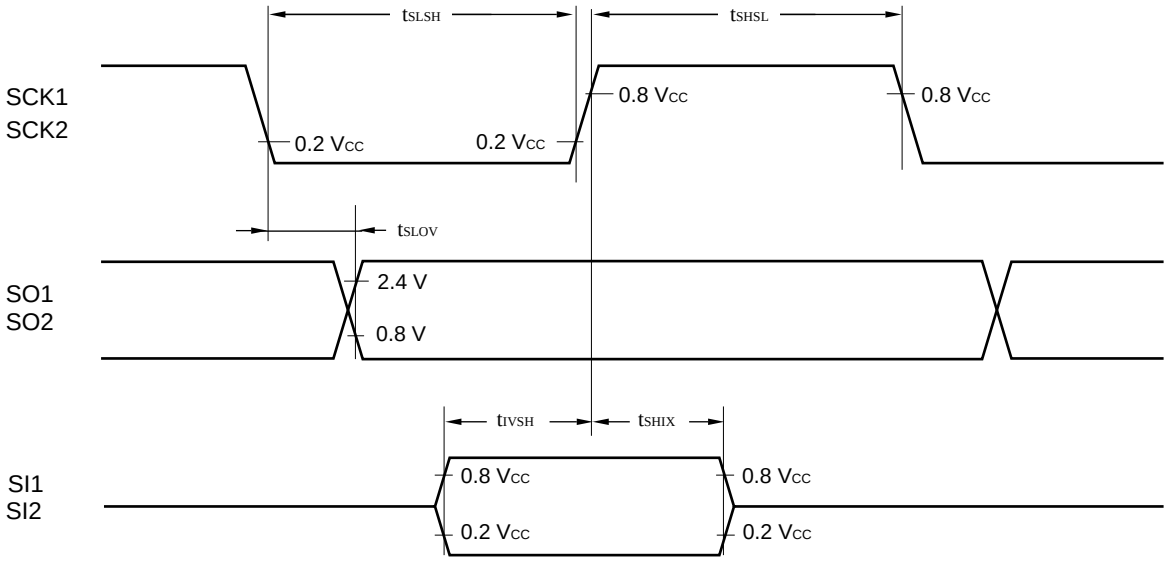
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK1, SCK2	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time SCK2 ↓ → SO2 time	t_{SLOV}	SCK1, SO1 SCK2, SO2		–200	200	ns	
Valid SI1 → SCK1 ↑ Valid SI1 → SCK1 ↑	t_{IVSH}	SI1, SCK1 SI2, SCK2		1/2 t_{inst}*	—	µs	
SCK1 ↑ → valid SI1 hold time SCK2 ↑ → valid SI2 hold time	t_{SHIX}	SCK1, SI1 SCK2, SI2		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK1, SCK2	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK1, SCK2		1 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time SCK2 ↓ → SO2 time	t_{SLOV}	SCK1, SO1 SCK2, SO2		0	200	ns	
Valid SI1 → SCK1 ↑ Valid SI2 → SCK2 ↑	t_{IVSH}	SI1, SCK1 SI2, SCK2		1/2 t_{inst}*	—	µs	
SCK1 ↑ → valid SI1 hold time SCK2 ↑ → valid SI2 hold time	t_{SHIX}	SCK1, SI1 SCK2, SI2		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

• **Serial I/O Timing and UART Timing (Internal Shift Clock Mode)**



• **Serial I/O Timing and UART Timing (External Shift Clock Mode)**

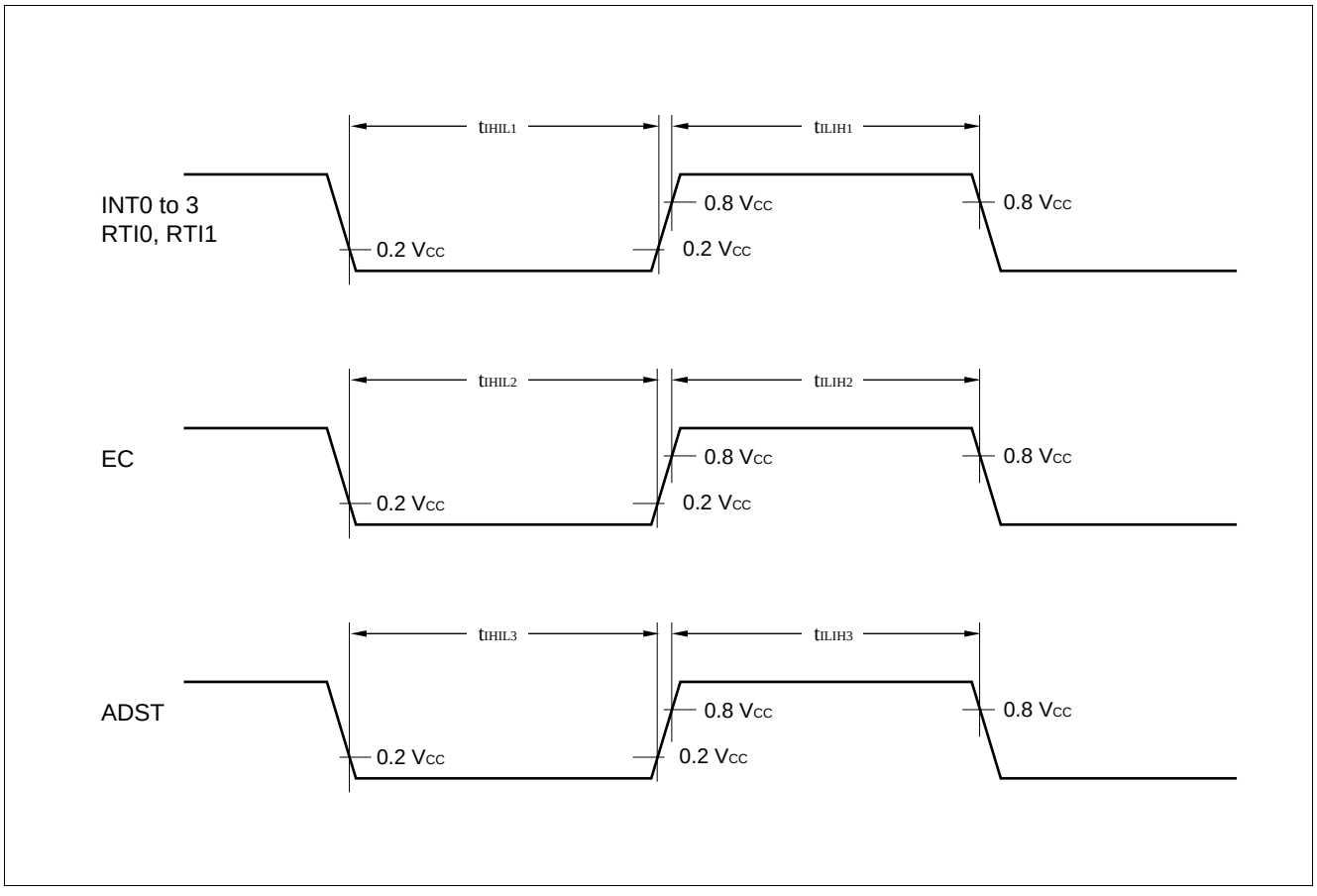


(6) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” level pulse width 1	t_{ILIH1}	RTI0, RTI1 INT0 to INT3	—	2 t_{inst}*	—	µs	
Peripheral input “L” level pulse width 1	t_{IHIL1}		—		—	µs	
Peripheral input “H” level pulse width 2	t_{ILIH2}	EC	—	1 t_{inst}*	—	µs	
Peripheral input “L” level pulse width 2	t_{IHIL2}		—		—	µs	
Peripheral input “H” level pulse width 3	t_{ILIH3}	ADST	A/D mode	32 t_{inst}*	—	µs	
Peripheral input “L” level pulse width 3	t_{IHIL3}				—	µs	
Peripheral input “H” level pulse width 3	t_{ILIH3}		Sense mode	8 t_{inst}*	—	µs	
Peripheral input “L” level pulse width 3	t_{IHIL3}				—	µs	

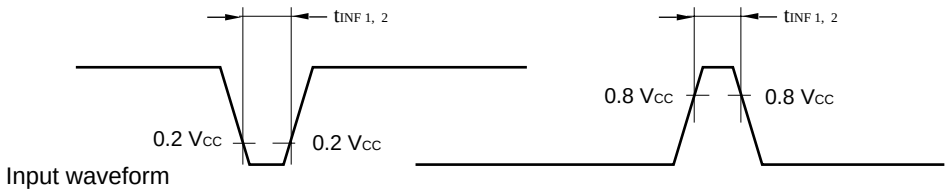
* : For information on t_{inst}, see “(4) Instruction cycle.”



(7) Noise Filter

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Noise filter width 1	t_{INF1}	P30 to P37, P40 to P47, P60 to P63	During port operation	15	—	ns	
Noise filter width 2	t_{INF2}	P60 to P63	During external interrupt	60	—	ns	



Input waveform

5. A/D Converter Electrical Characteristics

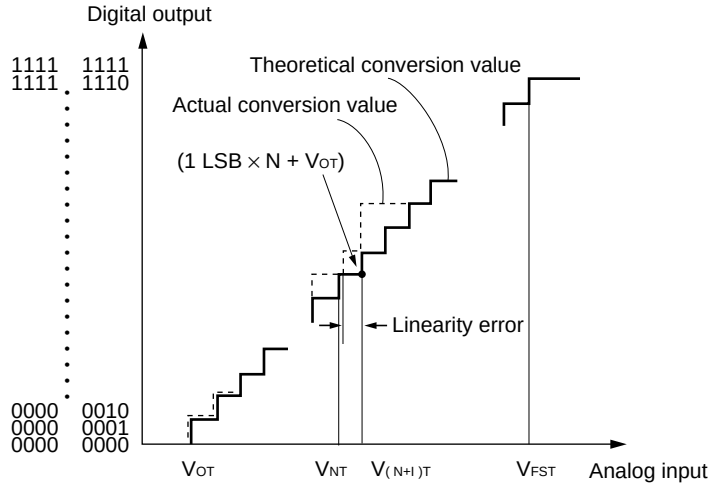
(AV_{CC} = V_{CC} = +3.5 V to 6.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	8	bit	
Total error			AVR = AV_{CC}	—	—	±2.0	LSB	
Linearity error				—	—	±1.0	LSB	
Differential linearity error				—	—	±0.9	LSB	
Zero transition voltage	V_{OT}			AV_{SS} – 1.5 LSB	AV_{SS}+ 0.5 LSB	AV_{SS}+ 2.5 LSB	mV	
Full-scale transition voltage	V_{FST}			AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 0.5 LSB	mV	
Interchannel disparity	—			—	—	1	LSB	
A/D mode conversion time			—	—	44 t_{isnt}*	—	µs	
Sense mode conversion time				—	12 t_{inst}*	—	µs	
Analog port input circuit	I_{AIN}	AN0 to AN7		—	—	10	µA	
Analog input voltage	—			0	—	AVR	V	
Reference voltage		AVR		0	—	AV_{CC}	V	
Reference voltage supply current	I_R		AVR = 5.0 V when A/D conversion is operating	—	150	—	µA	
	I_{RH}		AVR = 5.0 V when A/D conversion is not operating	—	—	5	µA	

* : For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

6. A/D Glossary

- Resolution
  Analog changes that are identifiable by the A/D converter
  When the number of bits is 8, analog voltage can be divided into 2^8 = 256.
- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point (“0000 0000” ↔ “0000 0001”) with the full-scale transition point (“1111 1111” ↔ “1111 1110”) from actual conversion characteristics
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values



$$1\ \text{LSB} = \frac{\text{AVR}}{256}$$

$$\text{Linearity error} = \frac{V_{NT} - (1\ \text{LSB} \times N + V_{OT})}{1\ \text{LSB}}$$

$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

$$\text{Total error} = \frac{V_{NT} - (1\ \text{LSB} \times N + 1\ \text{LSB})}{1\ \text{LSB}}$$

7. A/D Converter

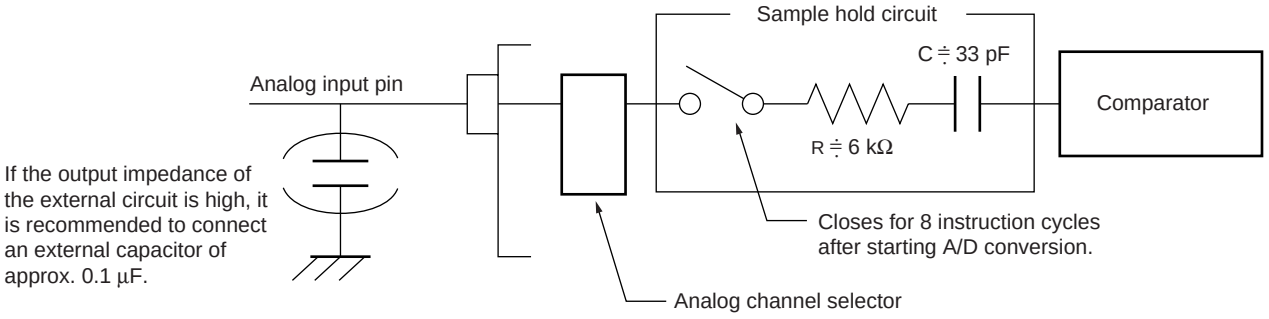
- **Input impedance of analog input pins**

  The A/D converter used for the MB89660R series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after starting A/D conversion.

  For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 2 kΩ).

  Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of approx. 0.1 µF for the analog input pin.

Analog Input Equivalent Circuit

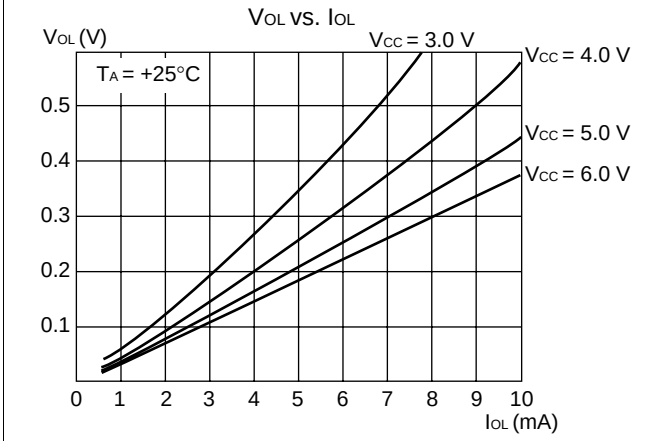


- **Error**

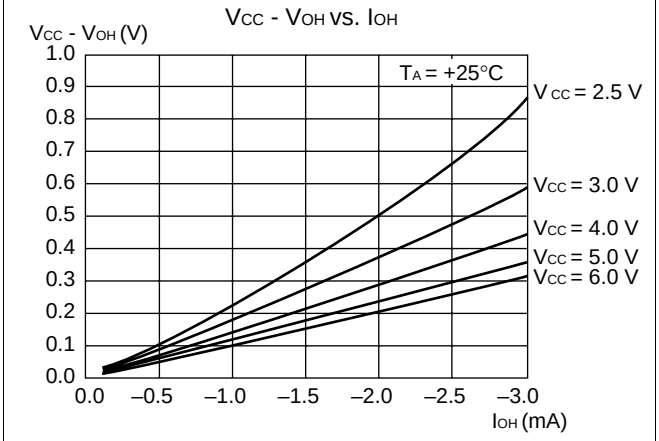
  The smaller the | AVR – AVSS |, the greater the error would become relatively.

■ EXAMPLES CHARACTERISTICS

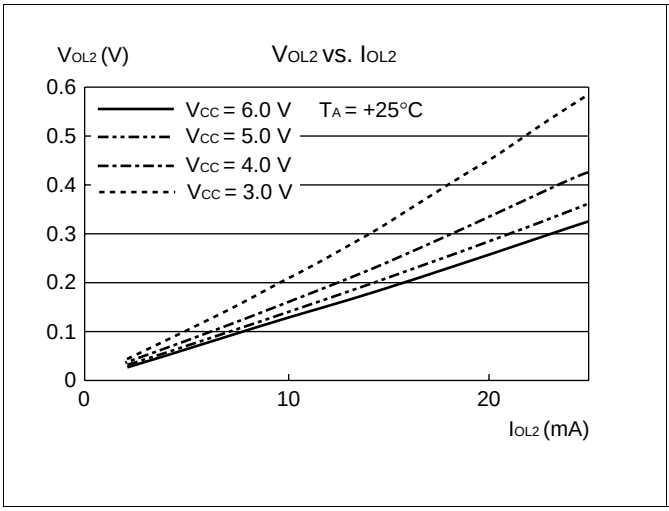
(1) "L" Level Output Voltage
P00 to P07, P10 to P17,P20 to P27, P30, P32 to P36, P40 to P47, P50 to P57, P60 to P63



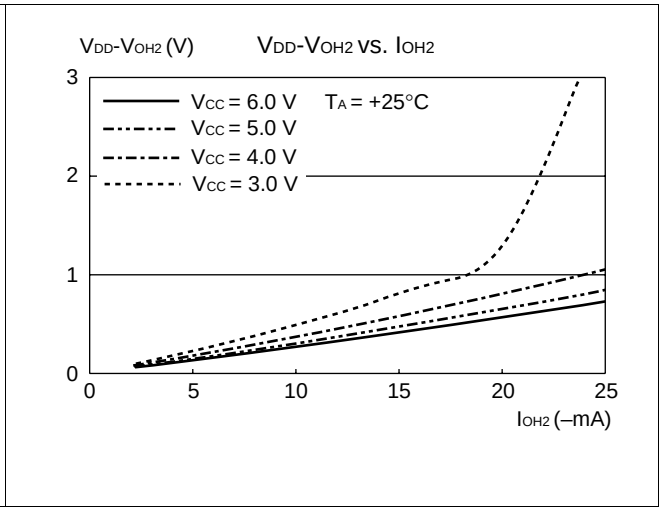
(2) "H" Level Output Voltage
P00 to P07, P10 to P17, P20 to P27, P30, P32 to P36, P40 to P47, P60 to P63



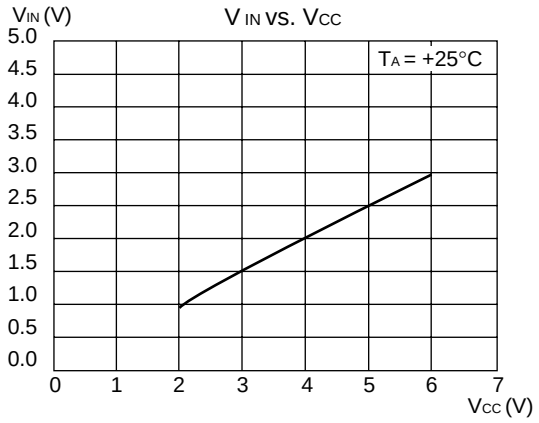
(3) "L" Level Output Voltage
P31, P37



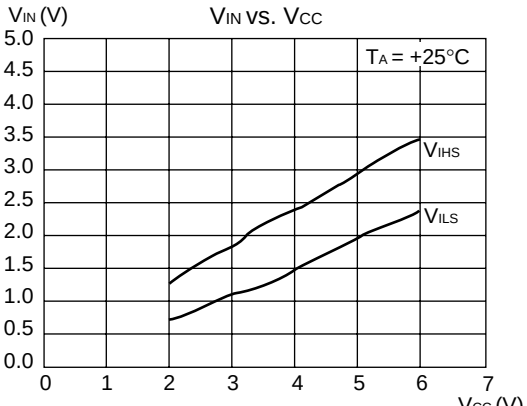
(4) "H" Level Output Voltage
P31, P37



(5) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



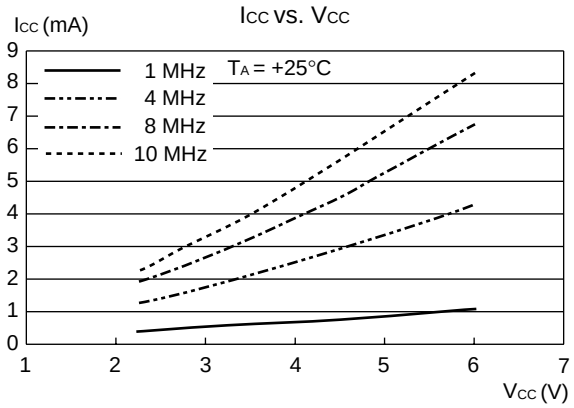
(6) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)

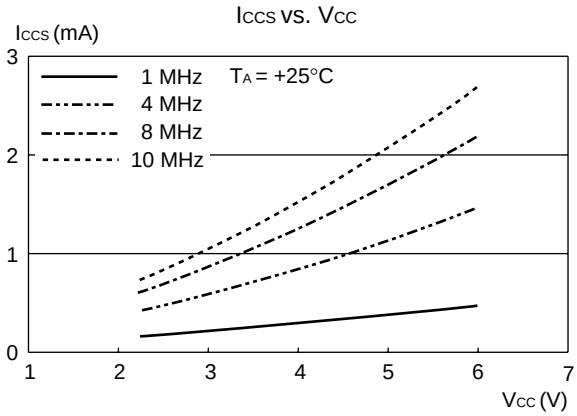


V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to “H” level

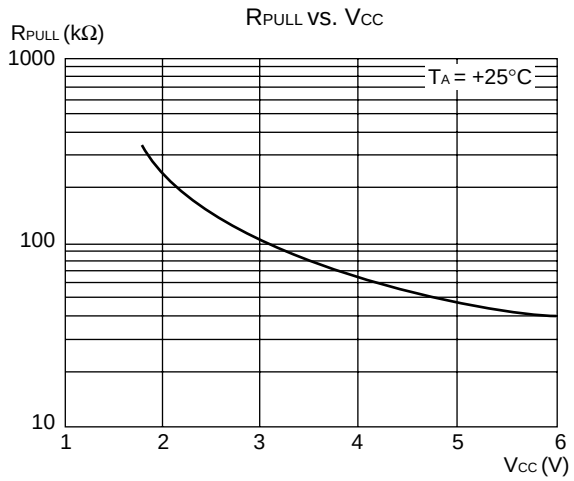
V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to “L” level

(7) Power Supply Current (External Clock)





(8) Pull-up Resistance



■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic:	Assembler notation of an instruction
~:	The number of instructions
#:	The number of bytes
Operation:	Operation of an instruction
TL, TH, AH:	A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following: • “–” indicates no change. • dH is the 8 upper bits of operation description data. • AL and AH must become the contents of AL and AH prior to the instruction executed. • 00 becomes 00.
N, Z, V, C:	An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.
OP code:	Code of an instruction. If an instruction is more than one code, it is written according to the following rule: Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A ┐	–	–	–	+ + – +	03
ROLC A	2	1	┌ C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX+d,#d8	CMP @IX+d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

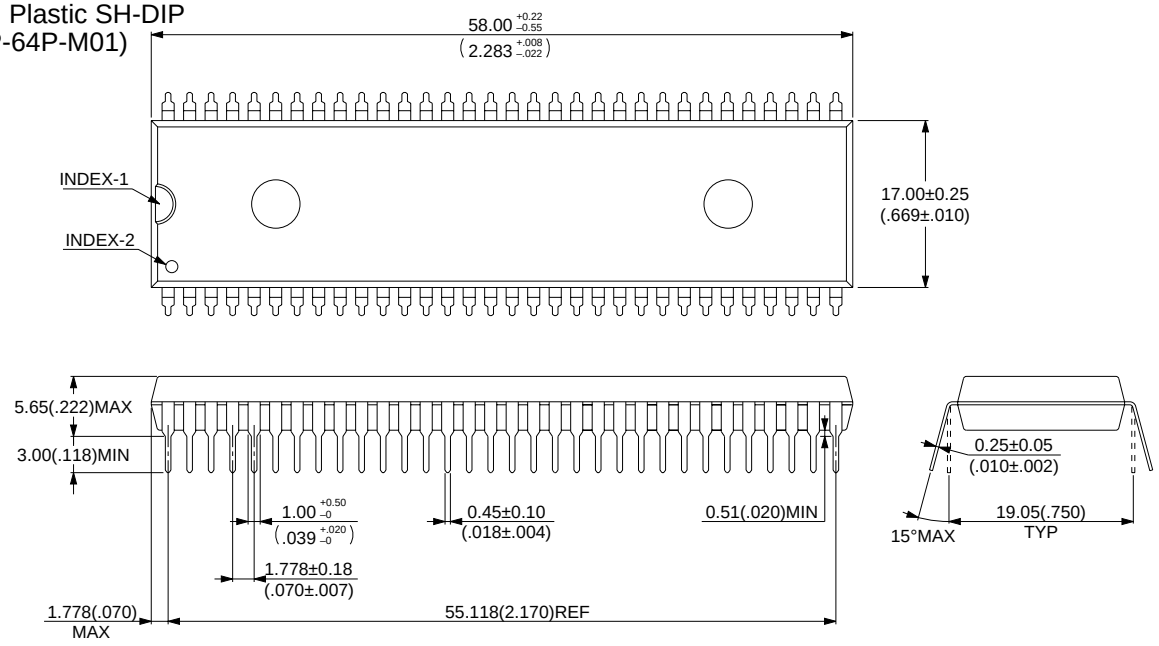
No.	Part number	MB89663R MB89665R	MB89P665 MB89W665
	Specifying procedure	**Specify when ordering masking**	**Specify with EPROM programmer**
1	Power-on reset • Power-on reset provided • No power-on reset	Selectable	Selectable
2	Selection of the oscillation stabilization time • Crystal oscillator (26.2 ms at 10 MHz) • Ceramic oscillator (1.64 ms at 10 MHz)	Selectable	Selectable
3	Reset pin output • With reset output • Without reset output	Selectable	Selectable
4	Pull-up resistors • P00 to P07, P10 to P17, • P30 to P37, P40 to P47, • P50 to P57, P60 to P63	Can be selected per pin. (Pull-up resistors can NOT be selected for P50 to P57 when an A/D converter is used.)	Can be set per pin. (P54 to P57 must have the same setting)

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89663RP-SH MB89665RP-SH MB89P665P-SH	64-pin Plastic SH-DIP (DIP-64P-M01)	
MB89663RPF MB89665RPF MB89P665PF	64-pin Plastic QFP (FPT-64P-M06)	
MB89W665C-SH	64-pin Ceramic SH-DIP (DIP-64C-A06)	

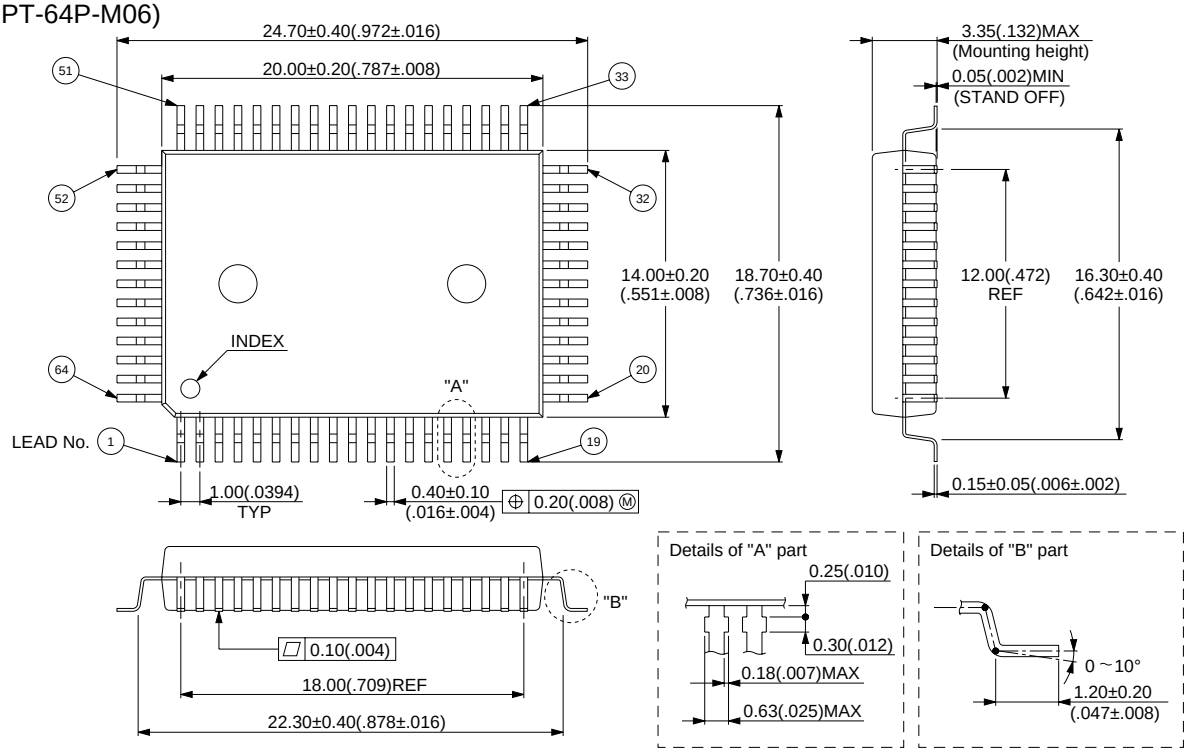
■ PACKAGE DIMENSION

64-pin Plastic SH-DIP
(DIP-64P-M01)



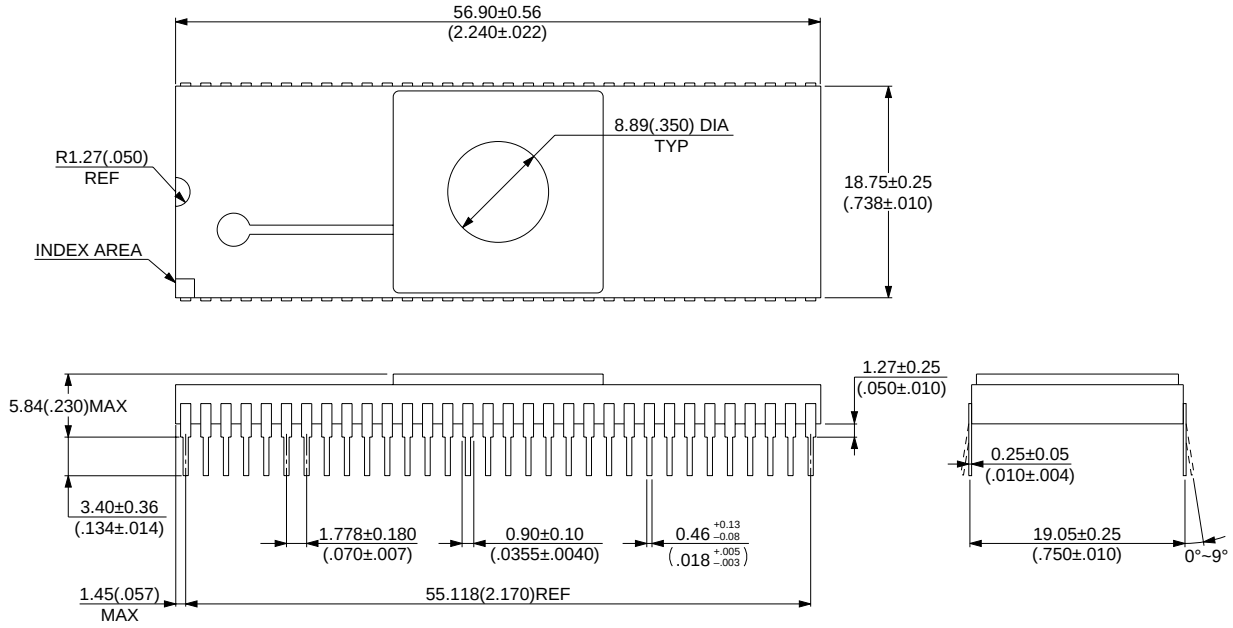
Dimensions in mm (inches)

64-pin Plastic QFP
(FPT-64P-M06)



Dimensions in mm (inches)

64-pin Ceramic SH-DIP
(DIP-64C-A06)



Dimensions in mm (inches)

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