Digital Video Level Shifter for dual mode DP signals w/ inverting buffer for HPD signal

Features

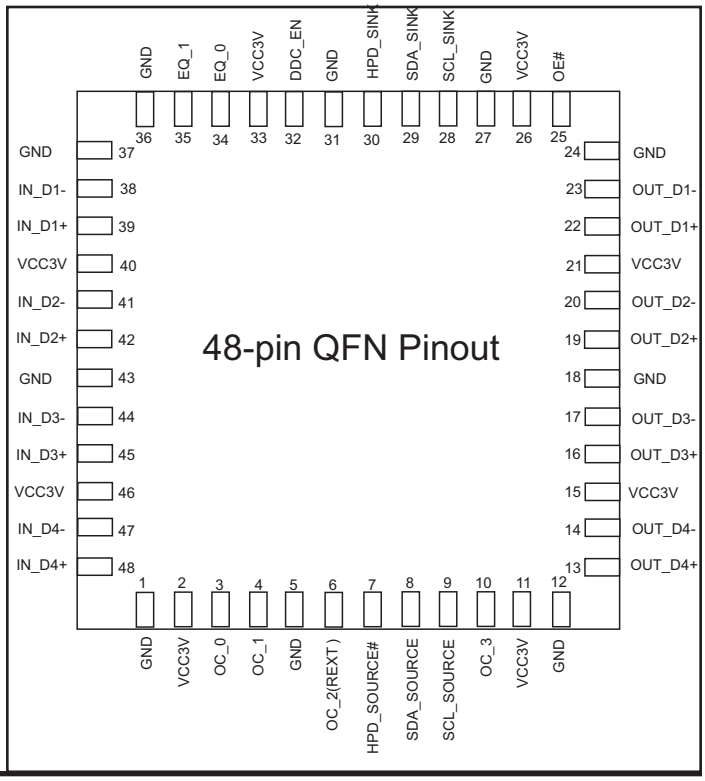
- Converts low-swing AC coupled differential input to HDMI rev 1.3 compliant open-drain current steering Rx terminated differential output
- HDMI level shifting operation up to 2.5Gbps per lane (250MHz pixel clock)
- Integrated 50-ohm termination resistors for AC-coupled differential inputs.
- Enable/Disable feature to turn off TMDS outputs to enter low-power state.
- Output slew rate control on TMDS outputs to minimize EMI.
- Transparent operation: no re-timing or configuration required.
- 3.3 Power supply required.
- Integrated ESD protection to 2kV Human Body on all I/O pins
- DDC level shifters
- Inverting level shifter for HPD signal from HDMI/DVI connector
- Integrated pull-down on HPD_sink input guarantees "input low" when no display is plugged in

Description

Pericom Semiconductor's PI3VDP411LST provides the ability to use a Dual-mode Display Port transmitter in HDMI mode. This flexibility provides the user a choice of how to connect to their favorite display. All signal paths accept AC coupled video signals. The PI3VDP411LST converts this AC coupled signal into an HDMI rev 1.3 compliant signal with proper signal swing. This converstion is automatic and transparent to the user.

The PI3VDP411LST supports up to 2.5Gbps, which provides 12-bits of color depth per channel, as indicated in HDMI rev 1.3.

Pin Configuration



Block Diagram

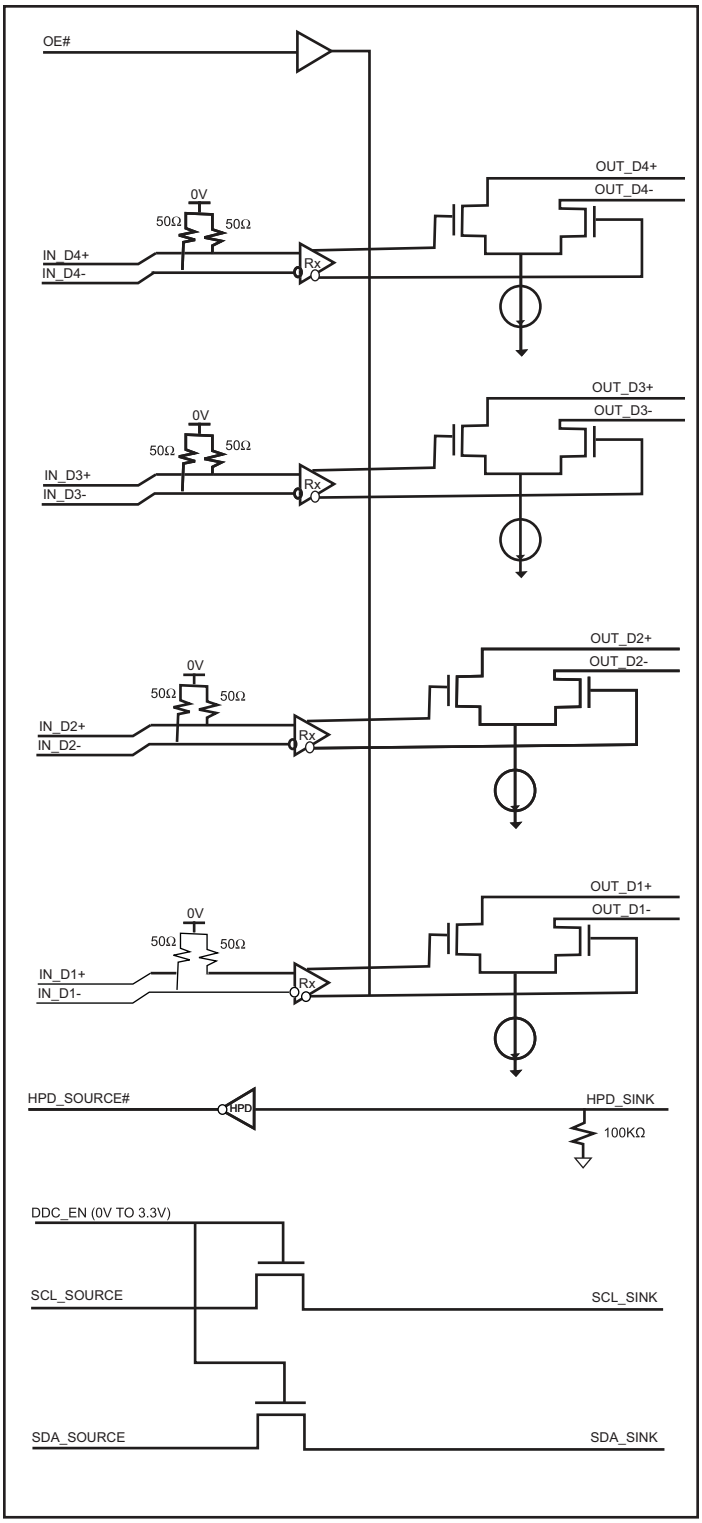


Table 1: Package Pinout

Pin Number	Pin Name
1	GND
2	VCC3V
3	OC_0
4	OC_1
5	GND
6	OC_2(REXT)
7	HPD_SOURCE#
8	SDA_SOURCE
9	SCL_SOURCE
10	OC_3
11	VCC3V
12	GND
13	OUT_D4+
14	OUT_D4-
15	VCC3V
16	OUIT_D3+
17	OUT_D3-
18	GND
19	OUT_D2+
20	OUT_D2-
21	VCC3V
22	OUT_D1+
23	OUT_D1-
24	GND
25	OE#
26	VCC3V
27	GND
28	SCL_SINK
29	SDA_SINK
30	HPD_SINK
31	GND
32	DDC_EN
33	VCC3V
34	EQ_0
35	EQ_1
36	GND
37	GND
38	IN_D1-
39	IN_D1+
40	VCC3V
41	IN_D2-
42	IN_D2+
43	GND
44	IN_D3-
45	IN_D3+
46	VCC3V
47	IN_D4-
48	IN_D4+

Maximum Ratings (Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....–65°C to +150°C
Supply Voltage to Ground Potential.....–0.5V to +5V
DC Input Voltage.....–0.5V to V_{DD}
DC Output Current.....120mA
Power Dissipation.....1.0W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 2: Signal Descriptions

Pin Name	Type	Description
OE#	5.5V tolerant low-voltage single-ended input	Enable for level shifter path OE# | IN_D Termination | OUT_D Outputs 1 | >100KΩ | High-Z 0 | 50Ω | Active
IN_D4+	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D4+ makes a differential pair with IN_D4–.
IN_D4–	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D4– makes a differential pair with IN_D4+.
IN_D3+	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D3+ makes a differential pair with IN_D3–.
IN_D3–	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D3– makes a differential pair with IN_D3+.
IN_D2+	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D2+ makes a differential pair with IN_D2–.
IN_D2–	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D2– makes a differential pair with IN_D2+.
IN_D1+	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D1+ makes a differential pair with IN_D1–.
IN_D1–	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D1– makes a differential pair with IN_D1+.
OUT_D4+	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D4+ makes a differential output signal with OUT_D4–.
OUT_D4–	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D4– makes a differential output signal with OUT_D4+.
OUT_D3+	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D3+ makes a differential output signal with OUT_D3–.
OUT_D3–	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D3– makes a differential output signal with OUT_D3+.

Pin Name	Type	Description
OUT_D2+	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D2+ makes a differential output signal with OUT_D2–.
OUT_D2–	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D2– makes a differential output signal with OUT_D2+.
OUT_D1+	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1–.
OUT_D1–	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D1– makes a differential output signal with OUT_D1+.
HPD_SINK	5V tolerance single-ended input	Low Frequency, 0V to 5V (nominal) input signal. This signal comes from the HDMI connector. Voltage High indicates "plugged" state; voltage low indicated "unplugged". HPD_SINK is pulled down by an integrated 100K ohm pulldown resistor.
HPD_SOURCE#	1V buffer	Inverted buffer from 0V to 5V input signal. If input is LOGIC HIGH, then output will be LOGIC LOW, with VOL max of 0.1V max. If input is LOGIC LOW, then output will be LOGIC LOW, with Voh of 0.8V min.
SCL_SOURCE	Single-ended 3.3V open-drain DDC I/O	3.3V DDC Data I/O. Pulled up by external termination to 3.3V. Connected to SCL_SINK through voltage-limiting intergrated NMOS passgate.
SDA_SOURCE	Single-ended 3.3V open-drain DDC I/O	3.3V DDC Data I/O. Pulled up by external termination to 3.3V. Connected to SDA_SINK through voltage-limiting intergrated NMOS passgate.
SCL_SINK	Single-ended 5V open-drain DDC I/O	5V DDC Clock I/O. Pulled up by external termination to 5V. Connected to SCL_SOURCE through voltage-limiting integrated NMOS passgate.
SDA_SINK	Single-ended 5V open-drain DDC I/O	5V DDC Data I/O. Pulled up by external termination to 5V. Connected to SDA_SOURCE through voltage-limiting integrated NMOS passgate.
DDC_EN	5.0V tolerant Single-ended input	Enables bias voltage to the DDC passgate level shifter gates. (May be implemented as a bias voltage connection to the DDC pass gates themselves.)
VCC3V	3.3V DC Supply	3.3V ± 10%
OC_2 (1) (REXT)	3.3V single-ended control input	Acceptable connections to OC_1 (REXT) pin are: Resistor to GND; Resistor to 3.3V; NC. (Resistor should be 0-ohm).

DDC_EN	Passgate
0V	Disabled
3.3V	Enabled

Note:
1) internal 100Kohm pull-up

Pin Name	Type	Description
OC_3(1)	Analog connection to external component or supply	Acceptable connections to OC_3 pin are: short to 3.3V or to GND; NC.
OC_0(1) OC_1(1) EQ_0(1) EQ_1(1)	Output and Input jitter elimination control	Control pins are to enable Jitter elimination features. For normal operation these pins are tied GND or to VCC3V. Please see the truth tables for more information.

Notes:
1) internal 100Kohm pull-up

Truth Table 1

OC_3	OC_2	OC_1	OC_0	Vswing (mV)	Pre/De-emphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0
0	0	1	1	1000	0
0	1	0	0	500	0
0	1	0	1	500	1.5dB
0	1	1	0	500	3.5dB
0	1	1	1	500	6dB
1	0	0	0	400	0
1	0	0	1	400	3.5dB
1	0	1	0	400	6dB
1	0	1	1	400	9dB
1	1	0	0	1000	0
1	1	0	1	1000	-3.5dB
1	1	1	0	1000	-6dB
1	1	1	1	1000	-9dB

Truth Table 2

EQ_0	EQ_1	Equalization (dB)
0	0	3
0	1	7.2
1	0	10
1	1	12

Electrical Characteristics

Table 3: Power Supplies and Temperature Range

Symbol	Parameter	Min	Nom	Max	Units	Comments
VCC3V	3.3V Power Supply	3.0	3.3	3.6	V	
ICC	Max Current			100	mA	Total current from VCC 3.3V supply when de-emphasis/ pre-emphasis is set to 0dB.
TCASE	Case temperature range for operation with spec.	-10		50	Celcius	

Table 4: $\overline{OE}$ Description

OE#	Device State	Comments
Asserted (low voltage)	Differential input buffers and output buffers enabled. Input impedance = 50Ω	Normal functioning state for IN_D to OUT_D level shifting function.
Unasserted (high voltage)	Low-power state. Differential input buffers and termination are disabled. Differential inputs are in a high-impedance state. OUT_D level-shifting outputs are disabled. OUT_D level-shifting outputs are in high-impedence state. Internal bias currents are turned off.	Intended for lowest power condition when: • No display is plugged in or • The level shifted data path is disabled HPD_SINK input and HPD_SOURCE output are not affected by OE# SCL_ SOURCE, SCL_SINK, SDA_SOURCE and SDA_SINK signals and functions are not affected by OE#

Table 5: Differential Input Characteristics for IN_D and RX_IN signals

Symbol	Parameter	Min	Nom	Max	Units	Comments
Tbit	Unit Interval	360			ps	Tbit is determined by the display mode. Nominal bit rate ranges from 250Mbps to 2.5Gbps per lane. Nominal Tbit at 2.5 Gbps=400ps. 360ps=400ps-10%
$V_{RX-DIFFp-p}$	Differential Input Peak to Peak Voltage	0.175		1.200	V	VRX-DIFFp-p=2'|VRX-D+ x VRX-D-| Applies to IN_D and RX_IN signals
T_{RX-EYE}	Minimum Eye Width at IN_D input pair	0.8			Tbit	The level shifter may add a maximum of 0.02UI jitter
$V_{CM-AC-pp}$	AC Peak Common Mode Input Voltage			100	mV	VCM-AC-pp = |VRX-D+ + VRX-D-|/2 - VRX-CM-DC. VRX-CM-DC = DC(avg) of|VRX-D+ + VRX-D-|/2 VCM-AC-pp includes all frequencies above 30 kHz.
Z_{RX-DC}		40	50	60	Ω	Required IN_D+ as well as IN_D- DC impedance (50Ω ± 20% tolerance).
$V_{RX-Bias}$		0		2.0	V	Intended to limit power-up stress on chipset's PCIE output buffers.
$Z_{RX-HIGH-Z}$		100			kΩ	Differential inputs must be in a high impedance state when OE# is HIGH.

TMDS Outputs

The level shifter's TMDS outputs are required to meet HMDI 1.3 specifications.
The HDMI 1.3 Specification is assumed to be the correct reference in instances where this document conflicts with the HDMI 1.3 specification.

Table 6: Differential Output Characteristics for TMDS_OUT signals

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_H	Single-ended high level output voltage	AVCC-10mV	AVCC	AVCC+10mV	V	AVCC is the DC termination voltage in the HDMI or DVI Sink. AVCC is nominally 3.3V
V_L	Single-ended low level output voltage	AVCC-600mV	AVCC-500mV	AVCC-400mV	V	The open-drain output pulls down from AVcc.
V_{SWING}	Single-ended output swing voltage	450mV	500mV	600mV	V	Swing down from TMDS termination voltage (3.3V ± 10%)
I_{OFF}	Single-ended current in high-Z state			10	µA	Measured with TMDS outputs pulled up to AVCC Max (3.6V)through 50Ω resistors.
T_R	Rise time	125ps		0.4Tbit	ps	Max Rise/Fall time @2.7Gbps = 148ps. 125ps = 148-15%
T_F	Fall time	125ps		0.4Tbit	ps	Max Rise/Fall time @2.7Gbps = 148ps. 125ps = 148-15%
$T_{SKEW-INTRA}$	Intra-pair differential skew			30	ps	This differential skew budget is in addition to the skew presented between D+ and D- paired input pins. HDMI revision 1.3 source allowable intra-pair skew is 0.15Tbit.
$T_{SKEW-INTER}$	Inter-pair lane-to-lane output skew			100	ps	This lane-to-lane skew budget is in addition to skew between differential input pairs
T_{JIT}	Jitter added to TMDS signals			25	ps	Jitter budget for TMDS signals as they pass through the level shifter. 25ps = 0.056 Tbit at 2.25 Gb/s

Table 8: HPD Input Characteristics

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{IH-HPD}	Input High Level	2.0	5.0	5.3	V	Low-speed input changes state on cable plug/unplug
V_{IL-HPD}	HPD_sink Input Low Level	0		0.8	V	
I_{IN-HPD}	HPD_sink Input Leakage Current			70	µA	Measured with HPD_sink at V_{IH-HPD} max and V_{IL-HPD} min
$V_{OH-HPDB}$	HPD_Source# Output High-Level, I_{OH} = -20mA	0.8		1.1	V	V_{CC} = 3.3V ± 10%
$V_{OL-HPDB}$	HPD_Source# Output Low-Level, I_{OL} = 1mA	0		0.1	V	
T_{HPD}	HPD_Source# to HPD_source propogation delay			200	ns	Time from HPD_sink changing state to HPD_source# changing state. Includes HPD_source rise/fall time
$T_{RF-HPDB}$	HPD_Source# rise/fall time	1		20	ns	Time required to transition from V_{OH-HPD} to V_{OL-HPD} or from V_{OL-HPD} to V_{OH-HPD}

Table 9: $\overline{OE}$ Input and DDC_EN

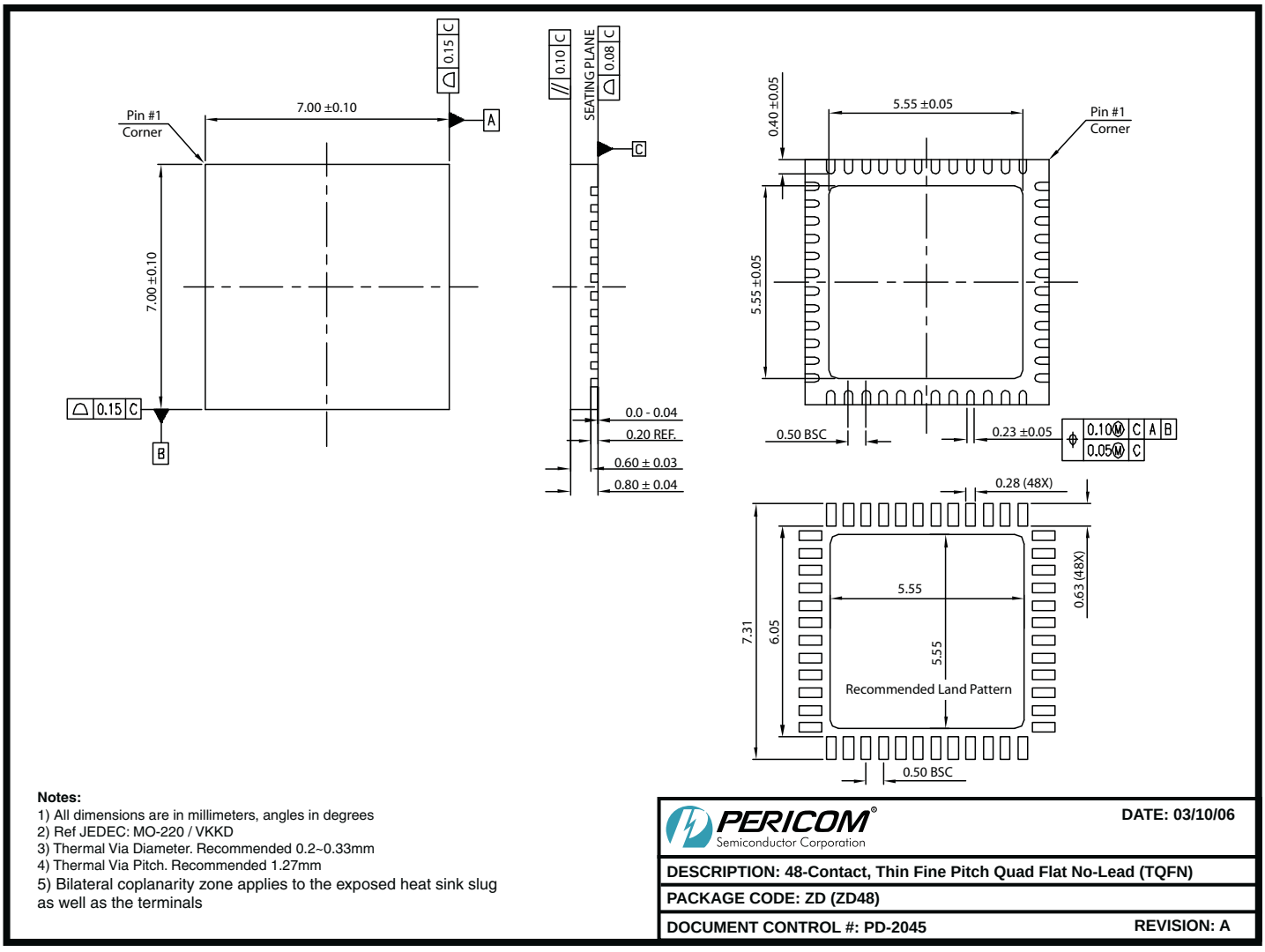
Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{IH}	Input High Level	2.0		VCC3V	V	TMDS enable input changes state on cable plug/unplug
V_{IL}	Input Low Level	0		0.8	V	
I_{IN}	Input Leakage Current			10	µA	Measured with input at V_{IH-EN} max and V_{IL-EN} min

DDC I/O Pins (SCL, SCL_SINK, SDA, SDA_SINK)							
$\|I_{lkg}\|$	Input leakage current	V_I = 0.1V_{CC} to 0.9V_{CC} to isolated DDC ports		0.1	2	µA
C_{IO}	Input/output capacitance	V_I = 0V		7.5		pF
R_{ON}	Switch resistance	I_O = 3mA, V_O = 0.4V		25	50	ohm
V_{PASS}	Switch output voltage	V_I = 3.3V, I_I = 100µA	1.5(2)	2.0	2.5(3)	V
Status Pins (HPD)						
$V_{OH(TTL)}$	TTL High-level output voltage	I_{OH} = -8mA	2.4			V
$V_{OL(TTL)}$	TTL Low-level output voltage	I_{OH} = 8mA			0.4	V

Table 10: Termination Resistors

Symbol	Parameter	Min	Nom	Max	Units	Comments
R_{HPD}	HPD_sink input pull-down resistor.	80K	100k	120K	Ω	Guarantees HPD_sink is LOW when no display is plugged in.

Packaging Mechanical: 48-Pin, TQFN (ZD)



Notes:
1) All dimensions are in millimeters, angles in degrees
2) Ref JEDEC: MO-220 / VKKD
3) Thermal Via Diameter. Recommended 0.2~0.33mm
4) Thermal Via Pitch. Recommended 1.27mm
5) Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals

PERICOM Semiconductor Corporation — DATE: 03/10/06

DESCRIPTION: 48-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD (ZD48)

DOCUMENT CONTROL #: PD-2045 — REVISION: A

Ordering Information

Ordering Code	Package Code	Package Description
PI3VDP411LSTZDE	ZD	48-pin Pb-free & Green, TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel