16-Mbit (512K X 32) Static RAM

Features

- **High speed**
  - **t_{AA} = 10 ns**
- **Low active power**
  - **I_{CC} = 150 mA @ 10 ns**
- **Low CMOS standby power**
  - **I_{SB2} = 25 mA**
- **Operating voltages of 3.3 ± 0.3V**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CE_3}$ features**
- **Available in Pb-free 119-ball plastic ball grid array (PBGA) package**

Functional Description

The CY7C1062DV33 is a high-performance CMOS Static RAM organized as 524,288 words by 32 bits.

Writing to the device is accomplished by enabling the chip ($\overline{CE_1}$, CE_2 and $\overline{CE_3}$ LOW) and forcing the Write Enable ($\overline{WE}$) input LOW. If Byte Enable A ($\overline{B_A}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$), is written into the location specified on the address pins (A$_0$ through A$_{18}$). If Byte Enable B ($\overline{B_B}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins (A$_0$ through A$_{18}$). Likewise, $\overline{B_C}$ and $\overline{B_D}$ correspond with the I/O pins I/O$_{16}$ to I/O$_{23}$ and I/O$_{24}$ to I/O$_{31}$, respectively.

Reading from the device is accomplished by enabling the chip ($\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CE_3}$ LOW) while forcing the Output Enable ($\overline{OE}$) LOW and Write Enable ($\overline{WE}$) HIGH. If the first Byte Enable ($\overline{B_A}$) is LOW, then data from the memory location specified by the address pins will appear on I/O$_0$ to I/O$_7$. If Byte Enable B ($\overline{B_B}$) is LOW, then data from memory will appear on I/O$_8$ to I/O$_{15}$. Similarly, $\overline{B_c}$ and $\overline{B_D}$ correspond to the third and fourth bytes. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O$_0$ through I/O$_{31}$) are placed in a high-impedance state when the device is deselected ($\overline{CE_1}$, $\overline{CE_2}$ or $\overline{CE_3}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the byte selects are disabled ($\overline{B_{A-D}}$ HIGH), or during a write operation ($\overline{CE_1}$, CE_2, and $\overline{CE_3}$ LOW, and $\overline{WE}$ LOW).

The CY7C1062DV33 is available in 119-ball plastic ball grid array (PBGA) package.

Logic Block Diagram
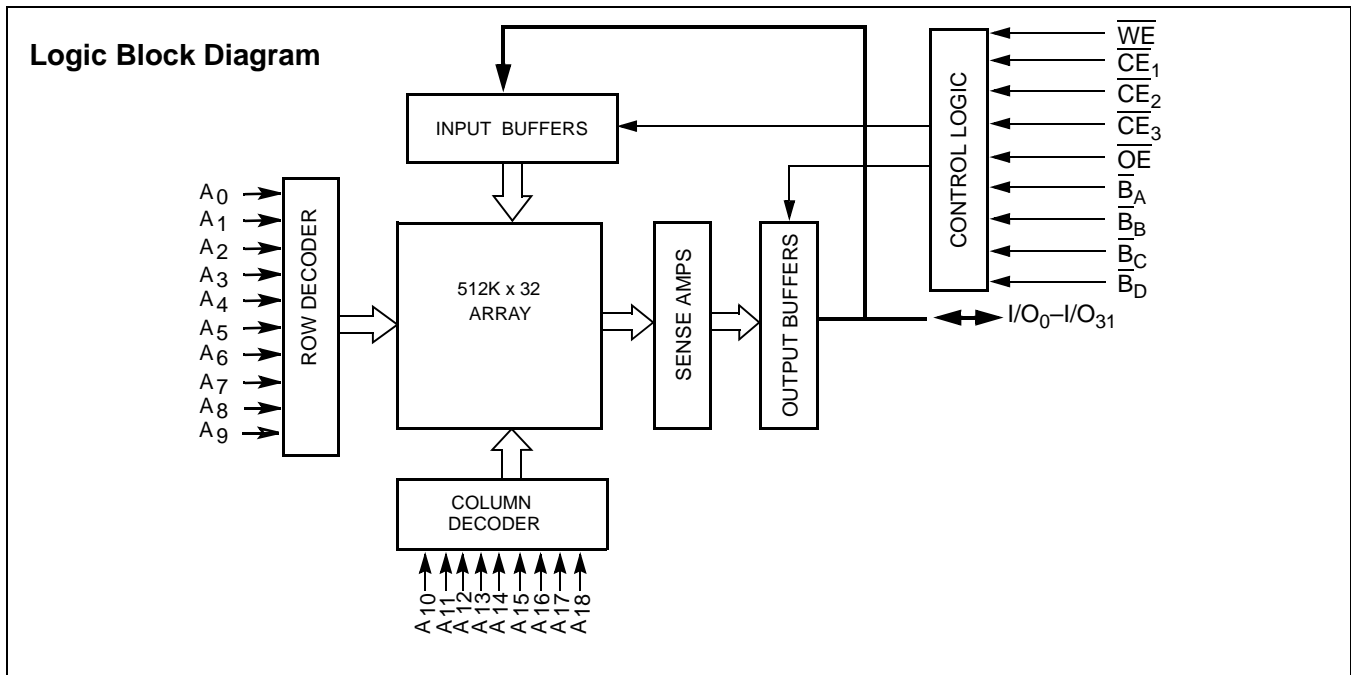
Selection Guide

	−10	**Unit**
Maximum Access Time	10	ns
Maximum Operating Current	150	mA
Maximum CMOS Standby Current	25	mA

Pin Configuration[1]

119-ball PBGA

(Top View)

	1	**2**	**3**	**4**	**5**	**6**	**7**
A	I/O_{16}	A	A	A	A	A	I/O_0
B	I/O_{17}	A	A	$\overline{CE_1}$	A	A	I/O_1
C	I/O_{18}	$\overline{B_c}$	$\overline{CE_2}$	NC	$\overline{CE_3}$	$\overline{B_a}$	I/O_2
D	I/O_{19}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_3
E	I/O_{20}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_4
F	I/O_{21}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_5
G	I/O_{22}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_6
H	I/O_{23}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_7
J	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	NC
K	I/O_{24}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_8
L	I/O_{25}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_9
M	I/O_{26}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{10}
N	I/O_{27}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_{11}
P	I/O_{28}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{12}
R	I/O_{29}	A	$\overline{B_d}$	NC	$\overline{B_b}$	A	I/O_{13}
T	I/O_{30}	A	A	$\overline{WE}$	A	A	I/O_{14}
U	I/O_{31}	A	A	$\overline{OE}$	A	A	I/O_{15}

Note:
1. NC pins are not connected on the die

[+] Feedback

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied ....–55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[2].....–0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State[2] .... –0.5V to V_{CC} + 0.5V

DC Input Voltage[2] ....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ....20 mA

Static Discharge Voltage...>2001V

(per MIL-STD-883, Method 3015)

Latch-up Current...>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	3.3V ± 0.3V

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions[7]	−10 Min.	−10 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]		−0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	−1	+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	−1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = 1/t_{RC} I_{OUT} = 0 mA CMOS levels		150	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		30	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V, or V_{IN} ≤ 0.3V, f = 0		25	mA

Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	I/O Capacitance		10	pF

Thermal Resistance[3]

Parameter	Description	Test Conditions	All - Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		TBD	°C/W

AC Test Loads and Waveforms[4]

(a)
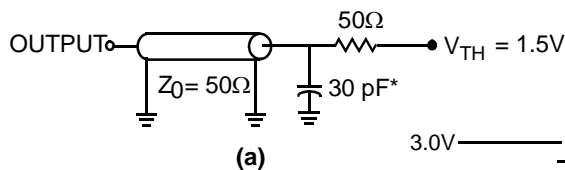
*Capacitive Load consists of all components of the test environment

(b)

(c)
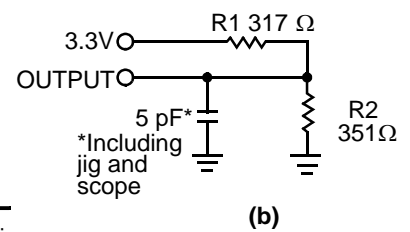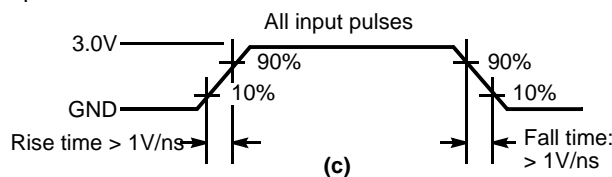
Notes:
2. V_{IL} (min.) = −2.0V and V_{IH}(max) = V_{CC} + 2V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.
4. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). 100μs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0V) voltage.

[+] Feedback

AC Switching Characteristics Over the Operating Range[5]

| Parameter	Description	−10 Min.	−10 Max.	Unit
Read Cycle				
t_{power}	V_{CC} (typical) to the first access[6]	100		µs
t_{RC}	Read Cycle Time	10		ns
t_{AA}	Address to Data Valid		10	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	$\overline{CE}$ active LOW to Data Valid[7]		10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[8]	1		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[8]		5	ns
t_{LZCE}	$\overline{CE}$ active LOW to Low-Z[7, 8]	3		ns
t_{HZCE}	$\overline{CE}$ deselect HIGH to High-Z[7, 8]		5	ns
t_{PU}	$\overline{CE}$ active LOW to Power-up[7, 9]	0		ns
t_{PD}	$\overline{CE}$ deselect HIGH to Power-down[7, 9]		10	ns
t_{DBE}	Byte Enable to Data Valid		5	ns
t_{LZBE}	Byte Enable to Low-Z[8]	1		ns
t_{HZBE}	Byte Disable to High-Z[8]		5	ns
Write Cycle[10, 11]				
t_{WC}	Write Cycle Time	10		ns
t_{SCE}	$\overline{CE}$ active LOW LOW to Write End[7]	7		ns
t_{AW}	Address Set-up to Write End	7		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		ns
t_{SD}	Data Set-up to Write End	5.5		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[8]	3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[8]		5	ns
t_{BW}	Byte Enable to End of Write	7		ns

Notes:
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V. Test conditions for the read cycle use output loading as shown in (a) of AC Test Loads, unless specified otherwise.
6. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
7. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE}_1$ and $\overline{CE}_2$ and $\overline{CE}_3$ LOW. When deselect HIGH, $\overline{CE}$ indicates the $\overline{CE}_1$ or $\overline{CE}_2$ or $\overline{CE}_3$ HIGH
8. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, and t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
9. These parameters are guaranteed by design and are not tested.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, $\overline{CE}_3$ LOW and $\overline{WE}$ LOW. The chip enables must be active and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

## Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2			V
I_{CCDR}	Data Retention Current	$V_{CC} = 2V$, $\overline{CE}_1 \geq V_{CC} - 0.2V$, $\overline{CE}_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			25	mA
t_{CDR}[3]	Chip Deselect to Data Retention Time		0			ns
t_R[12]	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform
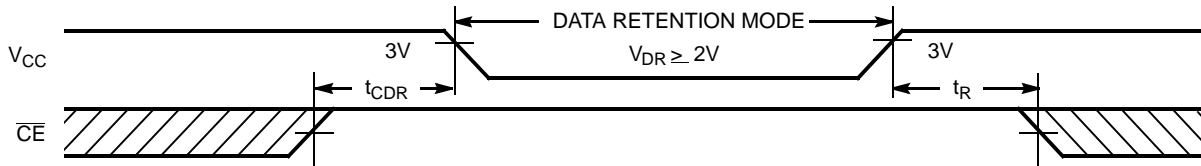
Switching Waveforms

Read Cycle No. 1[13,14]
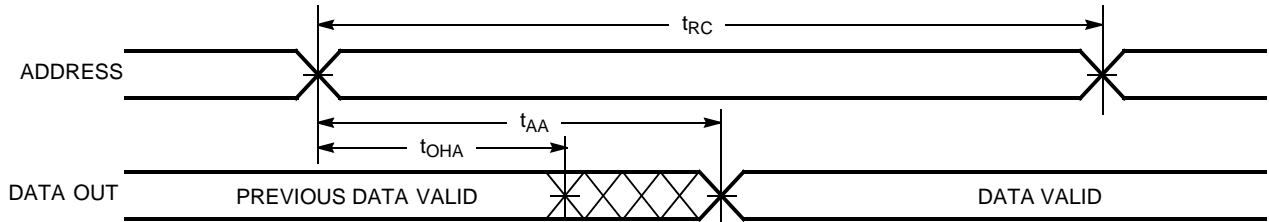
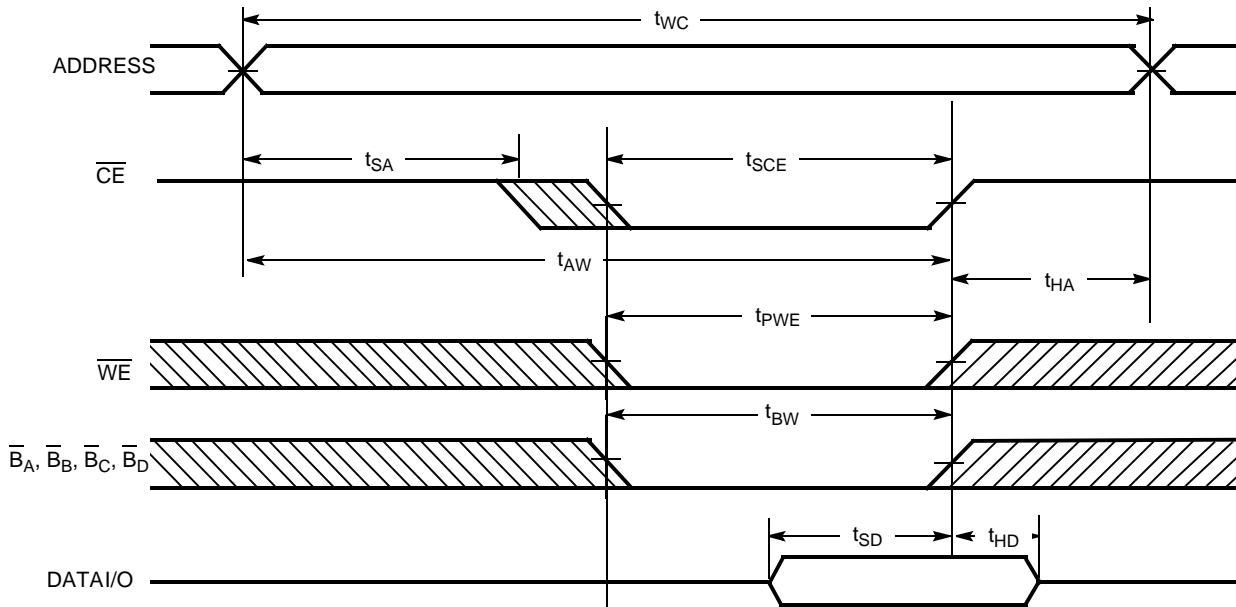**Read Cycle No. 2 ($\overline{OE}$ Controlled)**[13, 15, 15]
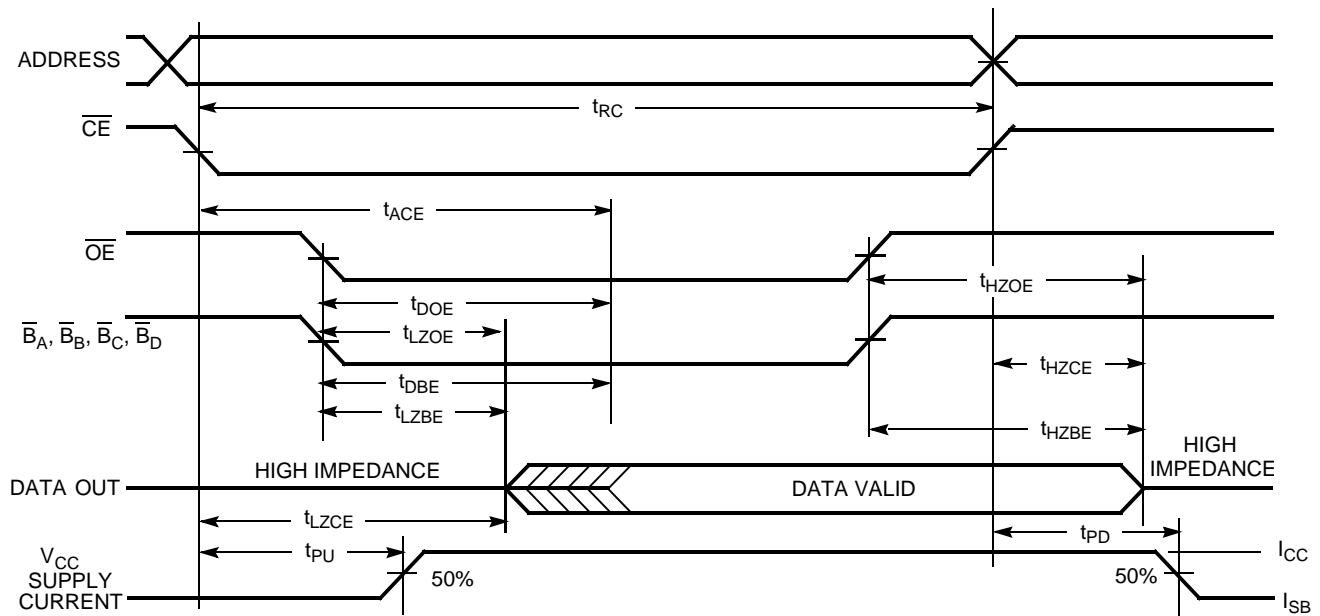
Notes:
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50\ \mu s$ or stable at $V_{CC(min.)} \geq 50\ \mu s$
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D = V_{IL}$.
14. $\overline{WE}$ is HIGH for read cycle.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

[+] Feedback

Switching Waveforms (continued)

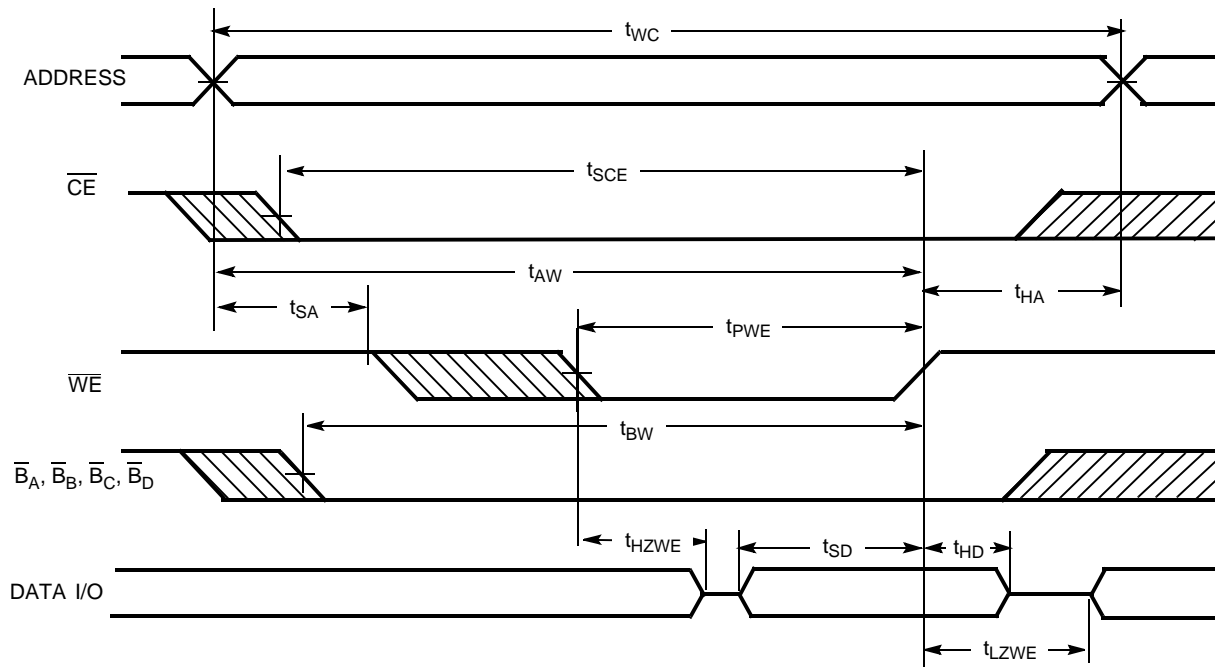**Write Cycle No. 1 ($\overline{CE}$ Controlled)**[15, 16, 17]

Write Cycle No. 2 ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ Controlled)[15, 16, 17]
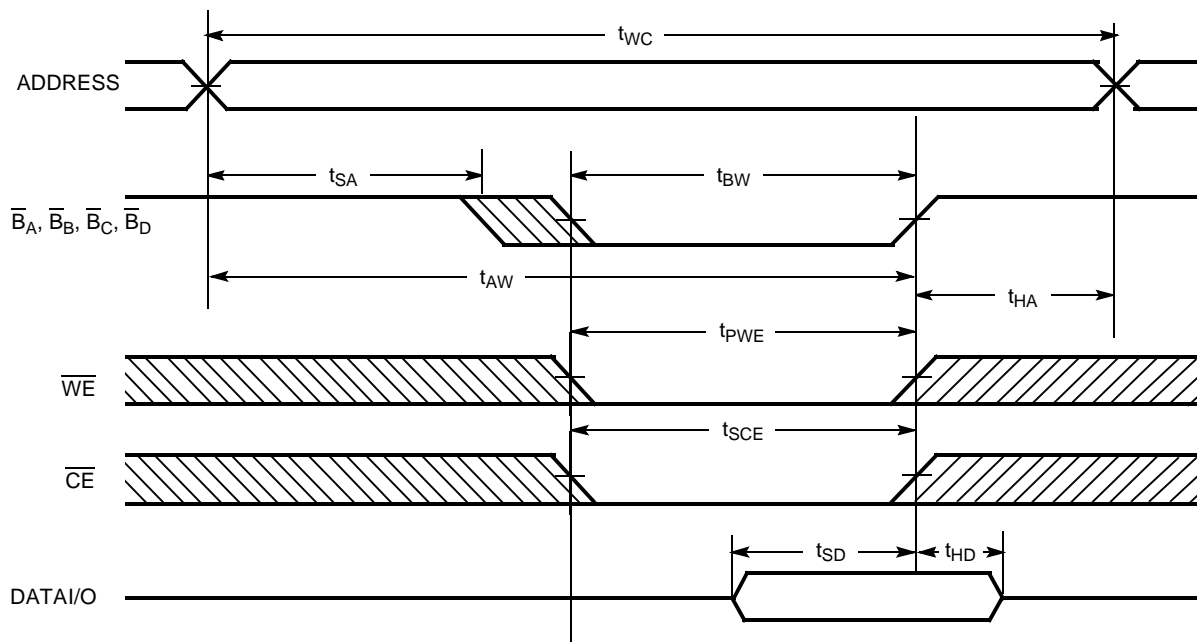
Notes:
16. Data I/O is high-impedance if $\overline{OE}$ or $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D = V_{IH}$.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

[+] Feedback

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)

Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{CE_3}$	$\overline{OE}$	$\overline{WE}$	$\overline{B_A}$	$\overline{B_B}$	$\overline{B_C}$	$\overline{B_D}$	I/O$_0$–I/O$_7$	I/O$_8$–I/O$_{15}$	I/O$_{16}$–I/O$_{23}$	I/O$_{24}$–I/O$_{31}$	Mode	Power
H	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I_{SB})
X	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I_{SB})
X	X	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I_{SB})
L	L	L	L	H	L	L	L	L	Data Out	Data Out	Data Out	Data Out	Read All Bits	(I_{CC})
L	L	L	L	H	L	H	H	H	Data Out	High-Z	High-Z	High-Z	Read Byte A Bits Only	(I_{CC})
L	L	L	L	H	H	L	H	H	High-Z	Data Out	High-Z	High-Z	Read Byte B Bits Only	(I_{CC})
L	L	L	L	H	H	H	L	H	High-Z	High-Z	Data Out	High-Z	Read Byte C Bits Only	(I_{CC})
L	L	L	L	H	H	H	H	L	High-Z	High-Z	High-Z	Data Out	Read Byte D Bits Only	(I_{CC})
L	L	L	X	L	L	L	L	L	Data In	Data In	Data In	Data In	Write All Bits	(I_{CC})
L	L	L	X	L	L	H	H	H	Data In	High-Z	High-Z	High-Z	Write Byte A Bits Only	(I_{CC})
L	L	L	X	L	H	L	H	H	High-Z	Data In	High-Z	High-Z	Write Byte B Bits Only	(I_{CC})
L	L	L	X	L	H	H	L	H	High-Z	High-Z	Data In	High-Z	Write Byte C Bits Only	(I_{CC})
L	L	L	X	L	H	H	H	L	High-Z	High-Z	High-Z	Data In	Write Byte D Bits Only	(I_{CC})
L	L	L	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Selected, Outputs Disabled	(I_{CC})
L	L	L	X	X	H	H	H	H	High-Z	High-Z	High-Z	High-Z	Selected, Outputs Disabled	(I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1062DV33-10BGXI	51-85115	119-ball Plastic Ball Grid Array (14 x 22 x 2.4 mm) (Pb-free)	Industrial

[+] Feedback

Package Diagram

119-ball PBGA (14 x 22 x 2.4 mm) (51-85115)
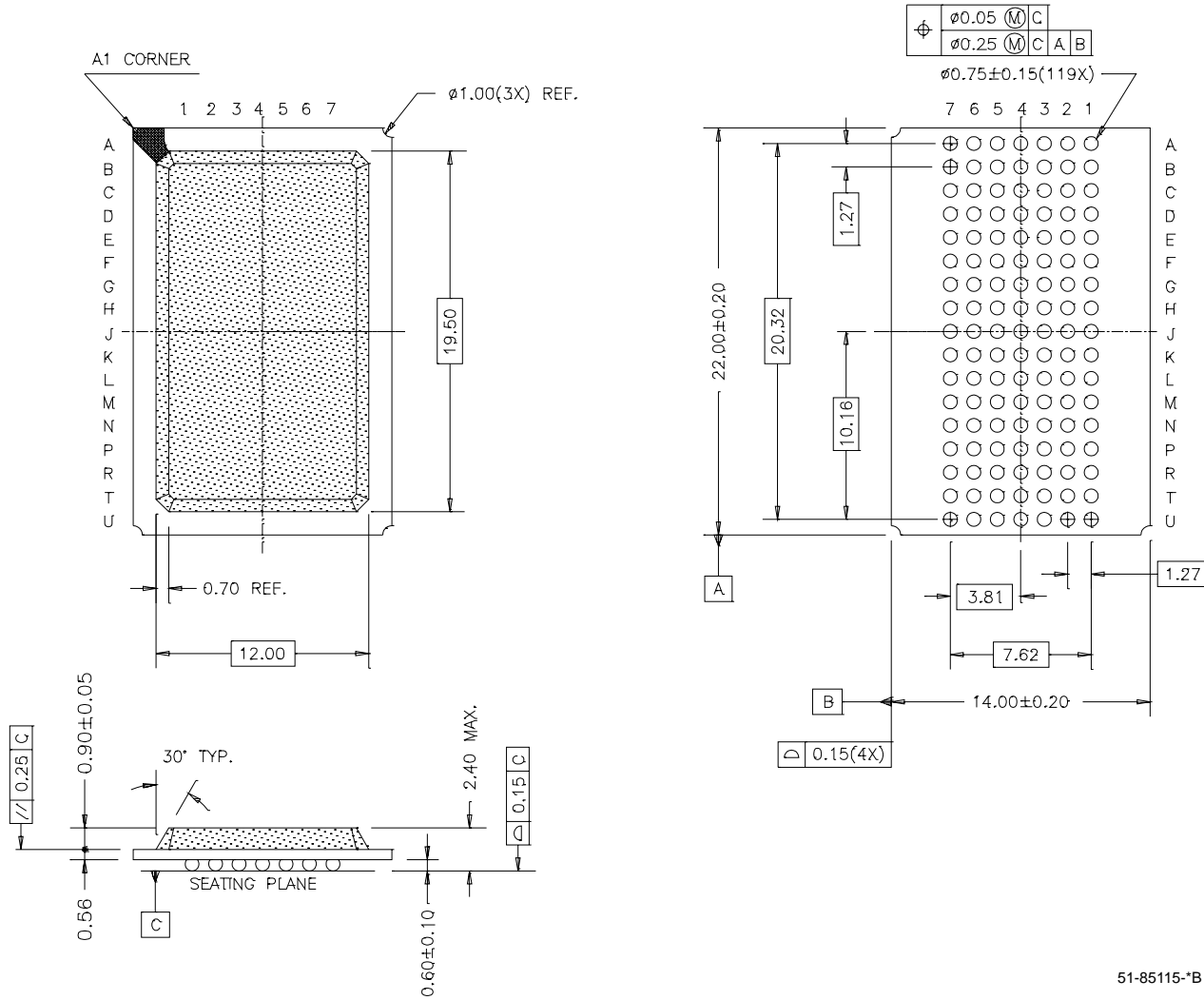
51-85115-*B

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Document History

| Document Title: CY7C1062DV33 16-Mbit (512K X 32) Static RAM | | | | |
| Document Number: 38-05477 | | | | |

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Data sheet for C9 IPP
*A	233748	See ECN	RKF	1.AC, DC parameters are modified as per EROS (Spec # 01-2165) 2.Pb-free offering in the 'ordering information'
*B	469420	See ECN	NXR	Converted from Advance Information to Preliminary Removed –8 and –12 speed bins from product offering Removed Commercial operating Range Changed J7 ball of PBGA from DNU to NC in the pinout diagram Included the Maximum ratings for Static Discharge Voltage and Latch Up Current on page #3 Changed $I_{CC(Max)}$ from 220 mA to 150 mA Changed $I_{SB1(Max)}$ from 70 mA to 30 mA Changed $I_{SB2(Max)}$ from 40 mA to 25 mA Specified the Overshoot spec in footnote # 1 Changed t_{SD} from 5.5 ns to 5 ns Added Data Retention Characteristics table and waveform on page # 5. Updated the 48-pin FBGA package Updated the Ordering Information Table
*C	499604	See ECN	NXR	Added note# 1 for NC pins Updated Test Condition for I_{CC} in DC Electrical Characteristics table Added note for t_{ACE}, t_{LZCE}, t_{HZCE}, t_{PU}, t_{PD}, t_{SCE} in AC Switching Characteristics Table on page# 4

[+] Feedback