



# EMP216MEAF Series

## 2Mx16 Pseudo Static RAM

### Document Title

2M x 16 bit Pseudo SRAM ( EMP216MEAF Series ) Specification

### Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	Oct. 24 , 2005	Preliminary

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**2Mb x16 Pseudo Static RAM Specification**

**GENERAL DESCRIPTION**

The EMP216MEAF series is 33,554,432 bits of Pseudo SRAM which uses DRAM type memory cells, but this device has refresh-free operation and extreme low power consumption technology. Furthermore the interface is compatible to a low power Asynchronous type SRAM. The EMP216MEAF is organized as 2,097,152 Words x 16 bit.

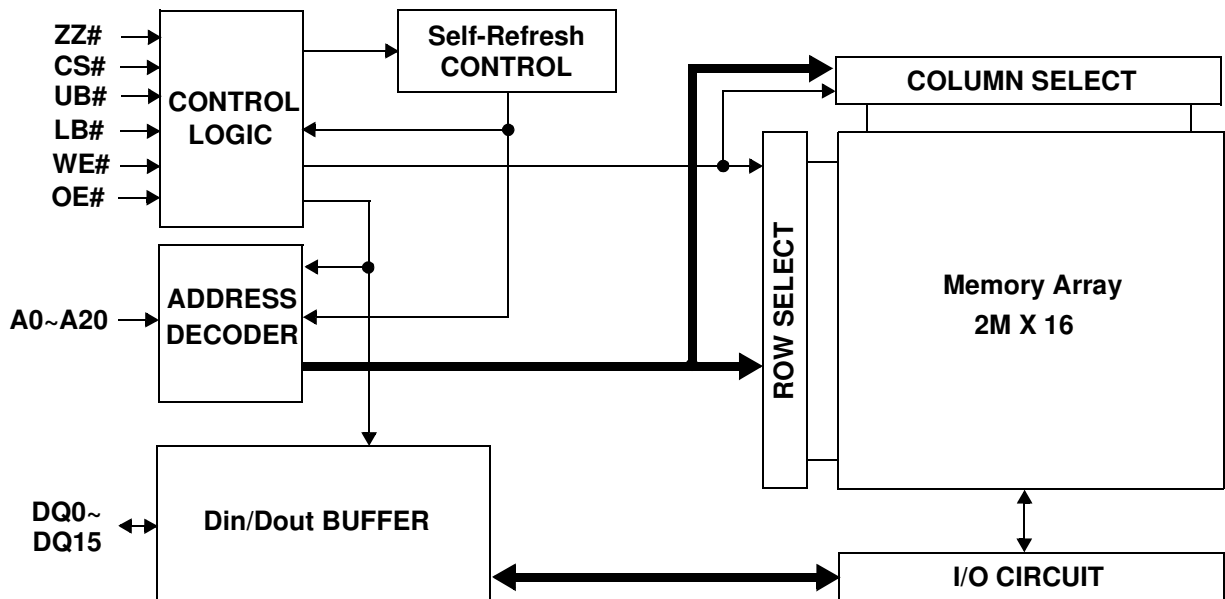
**FEATURES**

- Organization :2M x16
- Power Supply Voltage : 2.7 ~ 3.3V
- Separated I/O power(VccQ) & Core power(Vcc)
- Three state outputs
- Byte read/write control by UB# / LB#
- Support Page Read/Write operation with 16 words
- Support PASR, RMS, DPD and Auto-TCSR for power saving
- Package type : 48-FPBGA 6.0x8.0

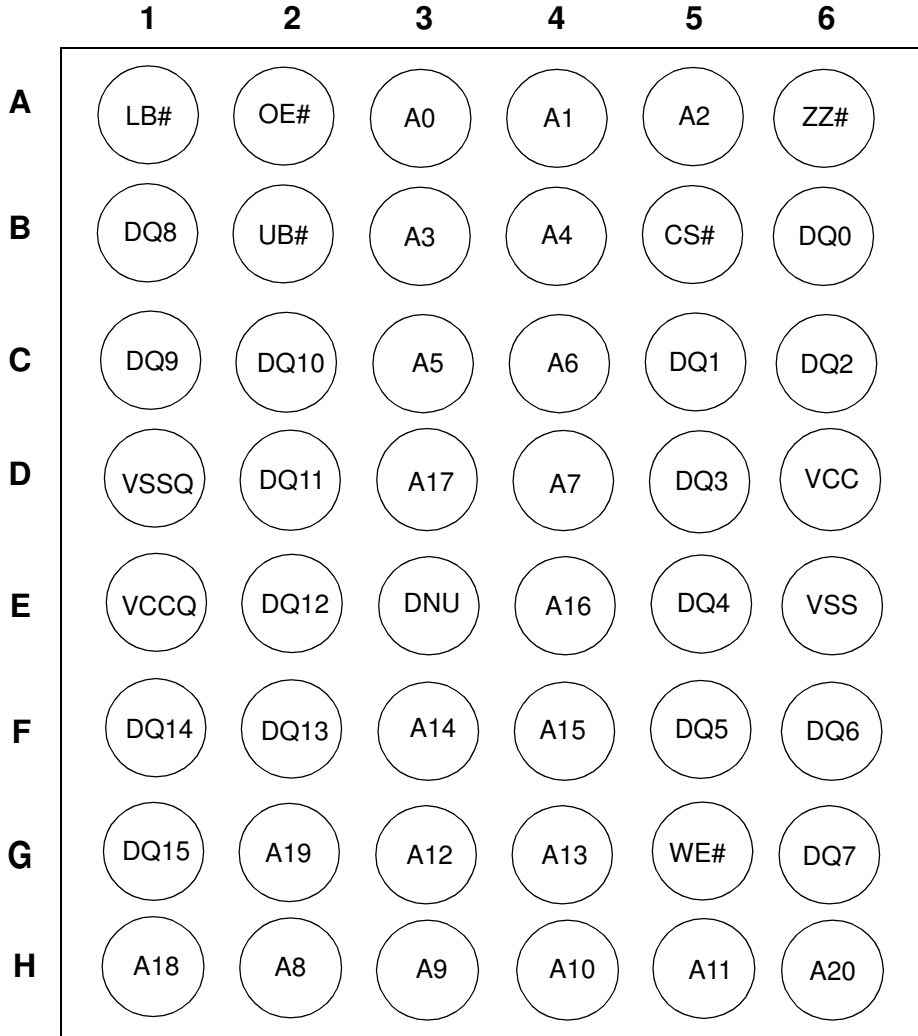
**PRODUCT FAMILY**

Part Number	Operating Temp.	Power Supply	Speed (t <sub>RC</sub> )	Power Dissipation	
				Standby (I <sub>SB1</sub> , Max.)	Operating (I <sub>CC2</sub> , Max.)
EMP216MEAF-70E	-25°C to 85°C	2.7V to 3.3V	70ns	100uA	25mA

**FUNCTION BLOCK DIAGRAM**



**PIN DESCRIPTION ( 48-FBGA-6.00x8.00 )**



**TOP VIEW (Ball Down)**

Name	Function	Name	Function
CS#	Chip select inputs	LB#	Lower byte (DQ <sub>0-7</sub> )
OE#	Output enable input	UB#	Upper byte (DQ <sub>8-15</sub> )
WE#	Write enable input	VCC	Power supply
ZZ#	Low Power Control	VCCQ	I/O Power supply
DQ <sub>0-15</sub>	Data In-out	VSS(Q)	Ground
A <sub>0-20</sub>	Address inputs	NC	No connection
DNU	Do Not Use		

**ABSOLUTE MAXIMUM RATINGS** <sup>1)</sup>

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss	$V_{IN}, V_{OUT}$	-0.2 to $V_{CCQ}+0.3V$	V
Voltage on Vcc supply relative to Vss	$V_{CC}, V_{CCQ}$	-0.2 <sup>2)</sup> to 3.6V	V
Power Dissipation	$P_D$	1.0	W
Storage Temperature	$T_{STG}$	-65 to 150	°C
Operating Temperature	$T_A$	-25 to 85	°C

1. Stresses greater than those listed above “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Undershoot at power-off : -1.0V in case of pulse width  $\leq 20ns$

**FUNCTIONAL DESCRIPTION**

CS#	ZZ#	OE#	WE#	LB#	UB#	DQ <sub>0~7</sub>	DQ <sub>8~15</sub>	Mode	Power
H	H	X	X	X	X	High-Z	High-Z	Deselected	Stand by
H	L	X	X	X	X	High-Z	High-Z	Deselected	Low Power Mode
X	H	X	X	H	H	High-Z	High-Z	Deselected	Stand by
L	H	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Data Out	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Data Out	Upper Byte Read	Active
L	H	L	H	L	L	Data Out	Data Out	Word Read	Active
L	H	X	L	L	H	Data In	High-Z	Lower Byte Write	Active
L	H	X	L	H	L	High-Z	Data In	Upper Byte Write	Active
L	H	X	L	L	L	Data In	Data In	Word Write	Active

Note: X means don't care. (Must be low or high state)

**RECOMMENDED DC OPERATING CONDITIONS**<sup>1)</sup>

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	2.7	3.0	3.3	V
	$V_{CCQ}$	2.7	3.0	3.3	V
Ground	$V_{SS}, V_{SSQ}$	0	0	0	V
Input high voltage	$V_{IH}$	$0.8 * V_{CCQ}$	-	$V_{CCQ} + 0.2^{2)}$	V
Input low voltage	$V_{IL}$	$-0.2^{3)}$	-	$0.2 * V_{CCQ}$	V

- $T_A = -25$  to  $85^\circ\text{C}$ , otherwise specified
- Overshoot:  $V_{CC} + 1.0$  V in case of pulse width  $\leq 20\text{ns}$
- Undershoot:  $-1.0$  V in case of pulse width  $\leq 20\text{ns}$
- Overshoot and undershoot are sampled, not 100% tested.

**CAPACITANCE**<sup>1)</sup> ( $f = 1\text{MHz}$ ,  $T_A = 25^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	$C_{IN}$	$V_{IN} = 0\text{V}$	-	8	pF
Input/Output capacitance	$C_{IO}$	$V_{IO} = 0\text{V}$	-	8	pF

- Capacitance is sampled, not 100% tested

**DC AND OPERATING CHARACTERISTICS**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	$I_{LI}$	$V_{IN} = V_{SS}$ to $V_{CCQ}$ , $V_{CC} = V_{CCmax}$	-1	-	1	$\mu\text{A}$
Output leakage current	$I_{LO}$	$CS\# = V_{IH}$ , $ZZ\# = V_{IH}$ , $OE\# = V_{IH}$ or $WE\# = V_{IL}$ , $V_{IO} = V_{SS}$ to $V_{CCQ}$ , $V_{CC} = V_{CCmax}$	-1	-	1	$\mu\text{A}$
Average operating current	$I_{CC1}$	Cycle time = $1\mu\text{s}$ , 100% duty, $I_{IO} = 0\text{mA}$ , $CS\# \leq 0.2\text{V}$ , $ZZ\# = V_{IH}$ , $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CCQ} - 0.2\text{V}$	-	-	3	mA
	$I_{CC2}$	Cycle time = Min, $I_{IO} = 0\text{mA}$ , 100% duty, $CS\# = V_{IL}$ , $ZZ\# = V_{IH}$ , $V_{IN} = V_{IL}$ or $V_{IH}$	-	-	25	mA
Output low voltage	$V_{OL}$	$I_{OL} = 0.5\text{mA}$ , $V_{CC} = V_{CCmin}$	-	-	$0.2 * V_{CCQ}$	V
Output high voltage	$V_{OH}$	$I_{OH} = -0.5\text{mA}$ , $V_{CC} = V_{CCmin}$	$0.8 * V_{CCQ}$	-	-	V
Standby Current (CMOS)	$I_{SB}$	$CS\#, ZZ\# \geq V_{CCQ} - 0.2\text{V}$ , Other inputs = $0 \sim V_{CCQ}$ (Typ. condition : $V_{CC} = 3.0\text{V}$ @ $25^\circ\text{C}$ ) (Max. condition : $V_{CC} = 3.3\text{V}$ @ $85^\circ\text{C}$ )	-	-	100	$\mu\text{A}$

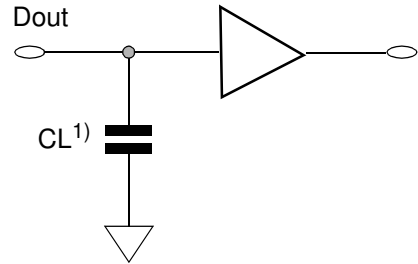
- Maximum  $I_{CC}$  specifications are tested with  $V_{CC} = V_{CCmax}$ .

**AC OPERATING CONDITIONS**

**Test Conditions** (Test Load and Test Input/Output Reference)

- Input Pulse Level : 0.2V to  $V_{CCQ}-0.2V$
- Input Rise and Fall Time : 5ns
- Input and Output reference Voltage :  $V_{CCQ}/2$
- Output Load (See right) :  $CL^1) = 30pF$

1. Including scope and Jig capacitance

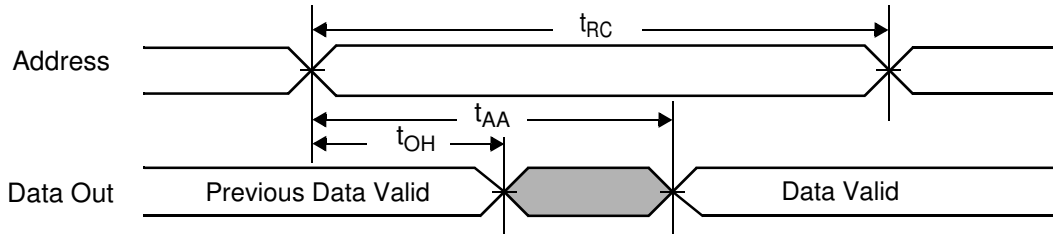


**AC CHARACTERISTICS** ( $V_{CC} = 2.7$  to  $3.3V$ ,  $Gnd = 0V$ ,  $T_A = -25C$  to  $+85^{\circ}C$ )

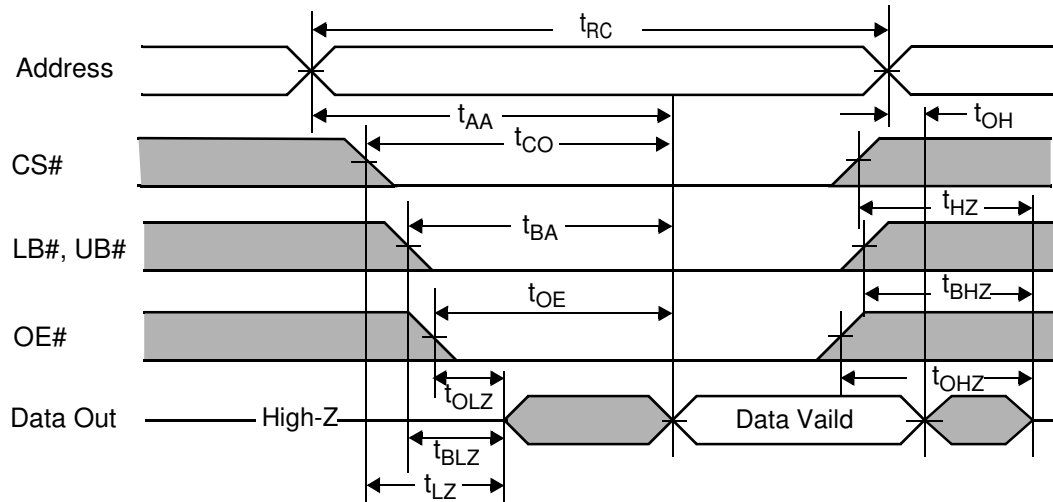
Parameter List		Symbol	Speed		Unit
			Min	Max	
Read	Read Cycle Time	$t_{RC}$	70	20k	ns
	Address access time	$t_{AA}$	-	70	ns
	Chip enable to data output	$t_{CO}$	-	70	ns
	Output enable to valid output	$t_{OE}$	-	25	ns
	UB#, LB# enable to data output	$t_{BA}$	-	70	ns
	Chip enable to low-Z output	$t_{LZ}$	10	-	ns
	UB#, LB# enable to low-Z output	$t_{BLZ}$	10	-	ns
	Output enable to low-Z output	$t_{OLZ}$	5	-	ns
	Chip disable to high-Z output	$t_{HZ}$	0	15	ns
	UB#, LB# disable to high-Z output	$t_{BHZ}$	0	15	ns
	Output disable to high-Z output	$t_{OHZ}$	0	15	ns
	Output hold from Address change	$t_{OH}$	5	-	ns
Write	Write Cycle Time	$t_{WC}$	70	20k	ns
	Chip enable to end of write	$t_{CW}$	60	-	ns
	Address setup time	$t_{AS}$	0	-	ns
	Address valid to end of write	$t_{AW}$	60	-	ns
	UB#, LB# valid to end of write	$t_{BW}$	60	-	ns
	Write pulse width	$t_{WP}$	50	-	ns
	Write recovery time	$t_{WR}$	0	-	ns
	Write to output high-Z	$t_{WHZ}$	0	15	ns
	Data to write time overlap	$t_{DW}$	20	-	ns
	Data hold from write time	$t_{DH}$	0	-	ns
	End write to output low-Z	$t_{OW}$	5	-	ns
Page	Maximum cycle time	$t_{MRC}$	-	20k	ns
	Page mode cycle time	$t_{PC}$	25	-	ns
	Page mode address access time	$t_{PAA}$	-	25	ns

**TIMING DIAGRAMS**

**READ CYCLE (1)** (Address controlled, CS#=OE#=V<sub>IL</sub>, ZZ#=WE#=V<sub>IH</sub>, UB# or/and LB#=V<sub>IL</sub>)



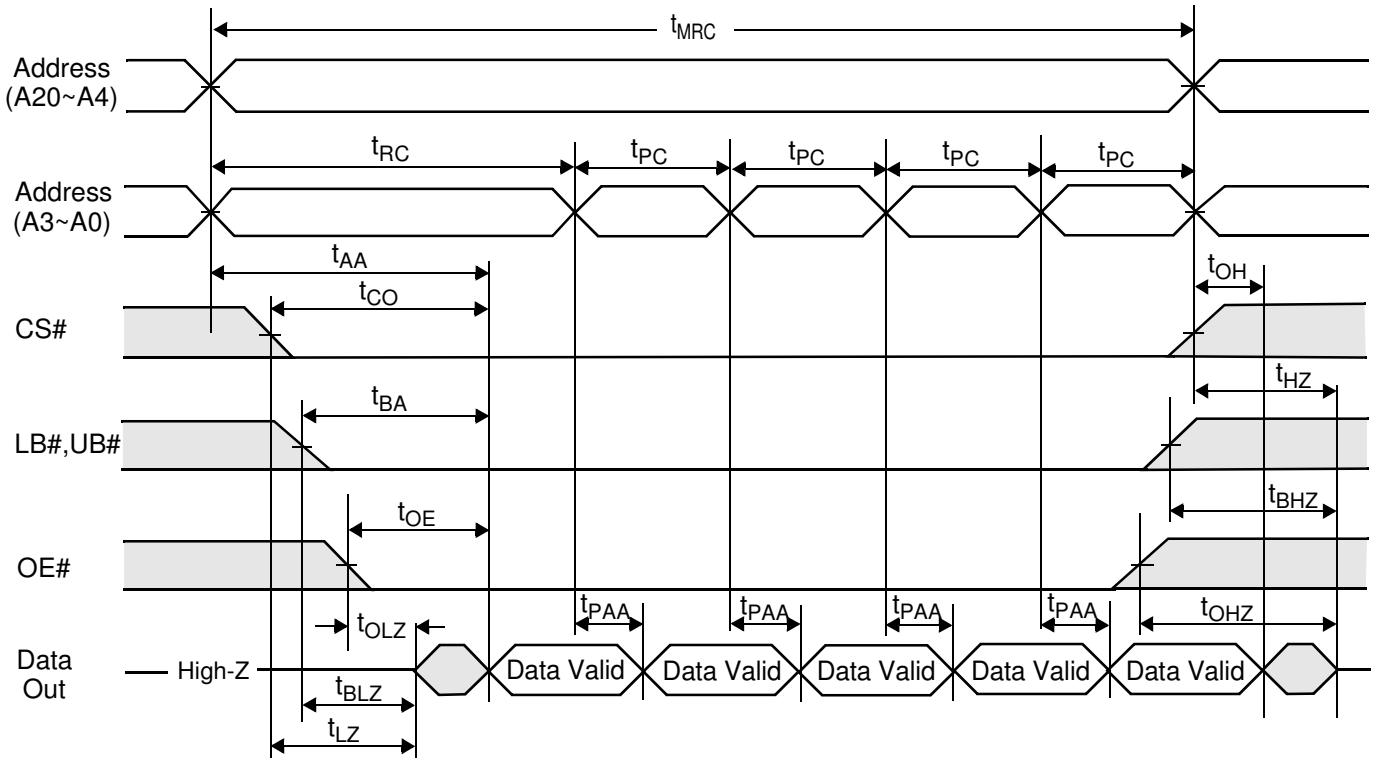
**READ CYCLE (2)** (ZZ#=WE#=V<sub>IH</sub>)



**NOTES (READ CYCLE)**

1. t<sub>HZ</sub>, t<sub>BHZ</sub> and t<sub>OHZ</sub> are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. Do not Access device with cycle timing shorter than t<sub>RC</sub> for continuous periods > 20us.

**PAGE READ CYCLE** ( $ZZ\#=WE\#=V_{IH}$ , 16 Words access)

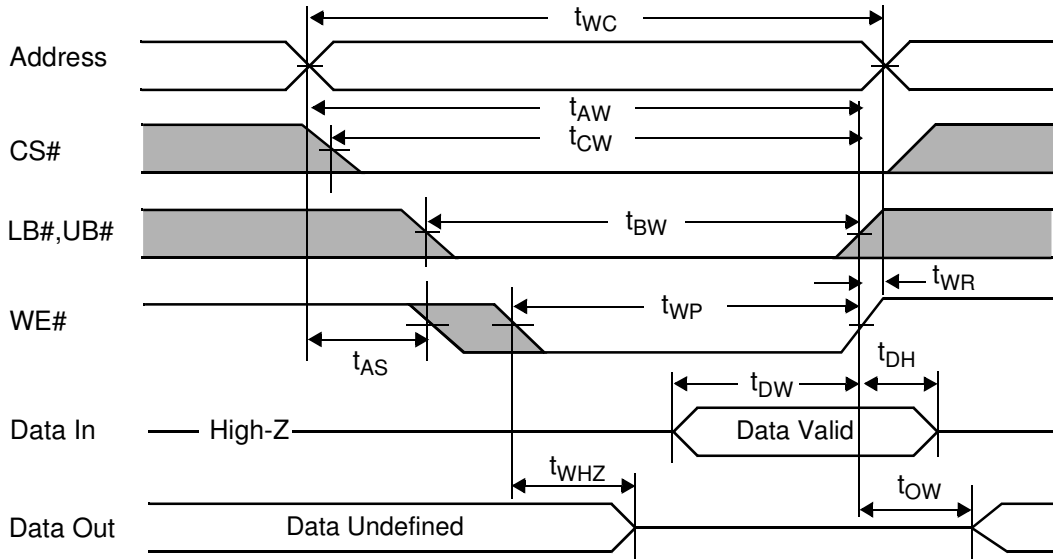


**NOTES (READ CYCLE)**

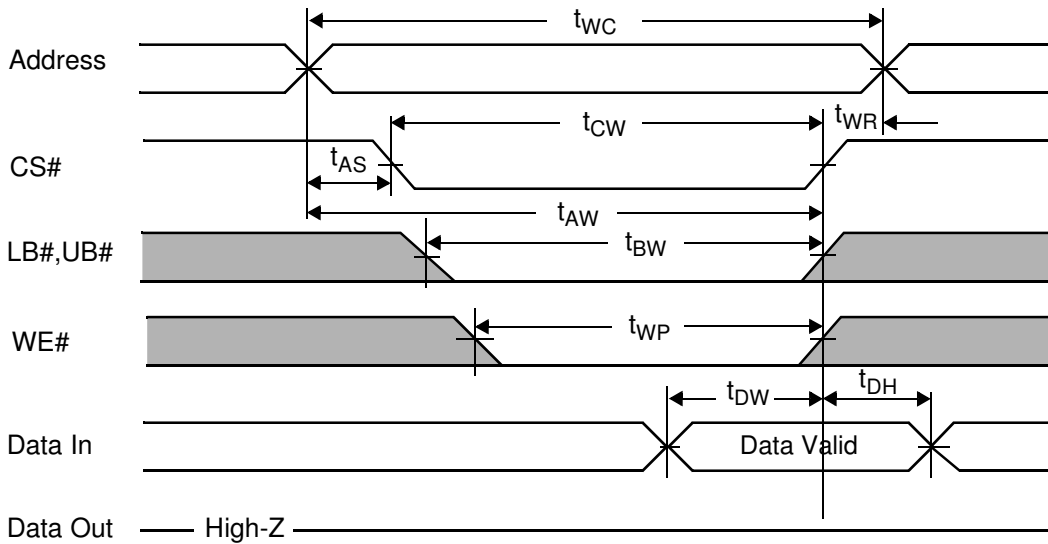
1.  $t_{HZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. Do not Access device with cycle timing shorter than  $t_{RC}$  for continuous periods > 20us.



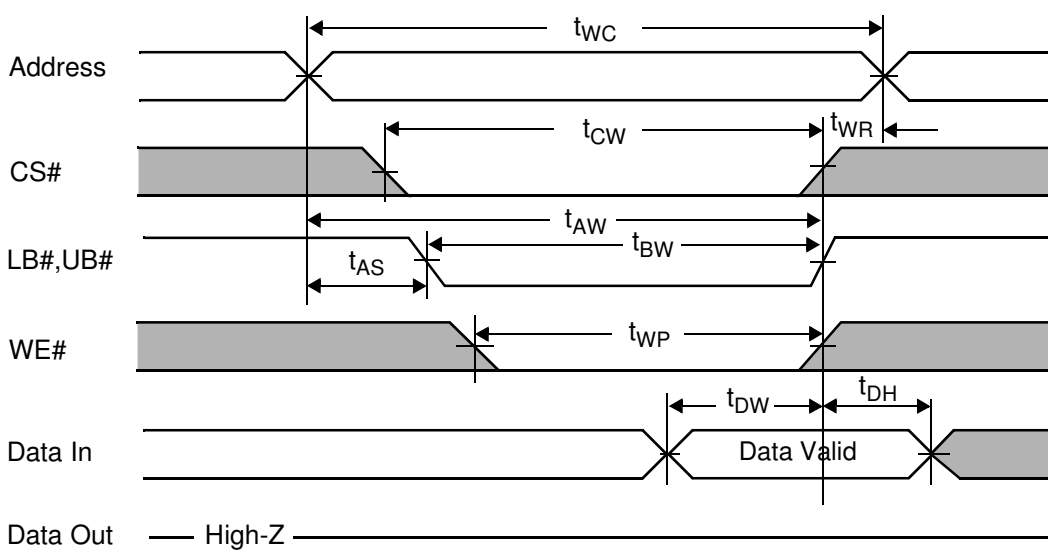
**WRITE CYCLE (1) (WE# controlled, ZZ#=V<sub>IH</sub>)**



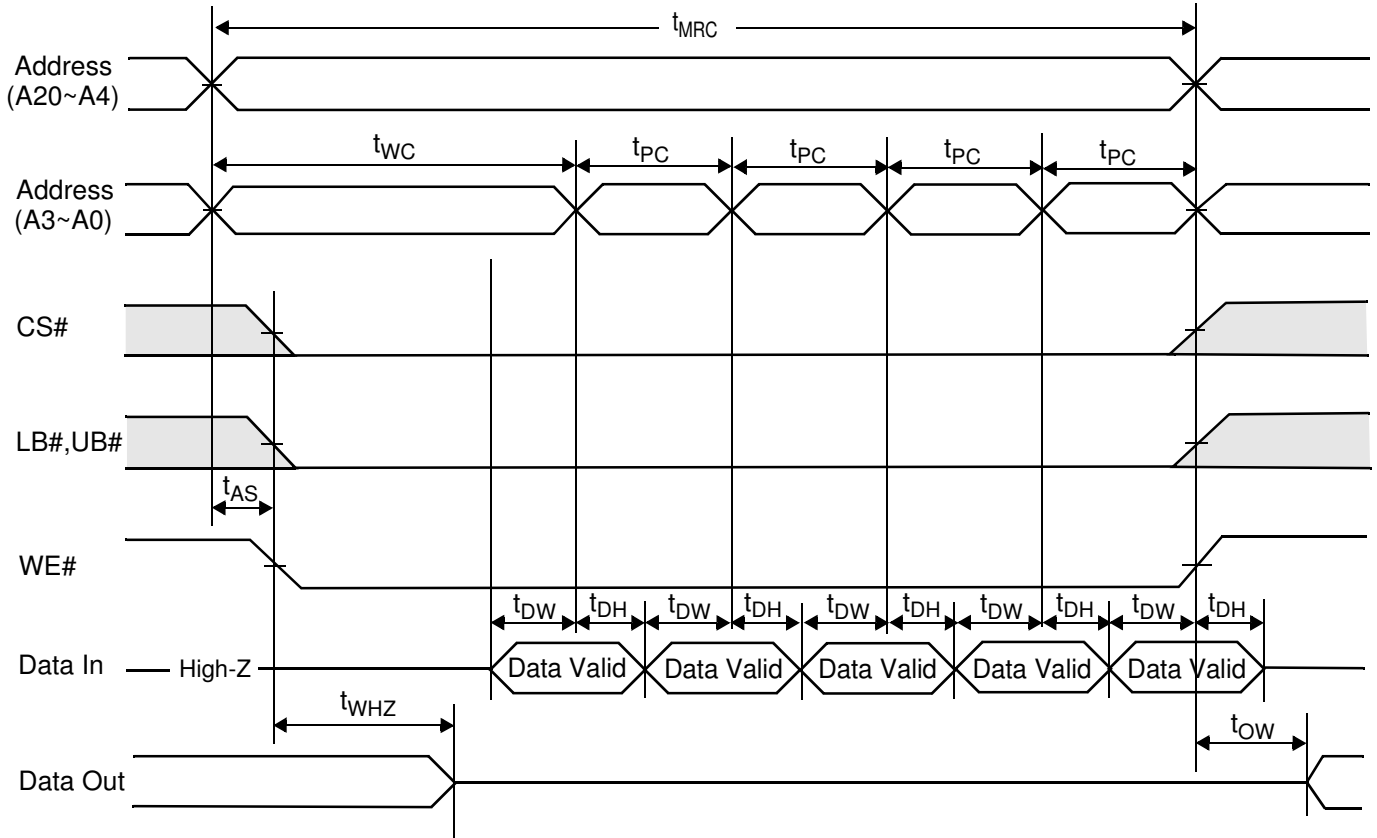
**WRITE CYCLE (2) (CS# controlled, ZZ#=V<sub>IH</sub>)**



**WRITE CYCLE (3) (UB#/LB# controlled, ZZ#=V<sub>IH</sub>)**



**PAGE WRITE CYCLE** ( $ZZ\#=V_{IH}$ , 16 Words access)



**NOTES (WRITE CYCLE)**

1. A write occurs during the overlap( $t_{WP}$ ) of low CS#, low WE# and low UB# or LB#. A write begins at the last transition among low CS# and low WE# with asserting UB# or LB# low for single byte operation or simultaneously asserting UB# and LB# low for word operation. A write ends at the earliest transition among high CS# and high WE#. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from CS# going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as CS# or WE# going high.
5. Do not Access device with cycle timing shorter than  $t_{WC}$  for continuous periods > 20us.

### LOW POWER MODES

#### Mode Register Set

A20 ~ A5	A4	A3	A2	A1	A0
All 0 (Reserved for future)	DPD Enable/Disable	Array Mode Selection	Array Half Selection	Array Refresh Area Selection	

#### DPD Enable / Disable

A4	Type
0	Deep Power Down Enable
1	DPD Disable (Default)

#### Array Mode Selection

A3	Type
0	Partial Array Refresh Mode (Default)
1	Reduced Memory Size Mode

#### Array Half Selection (Top/Down)

A2	Type
0	Bottom (Default)
1	Top

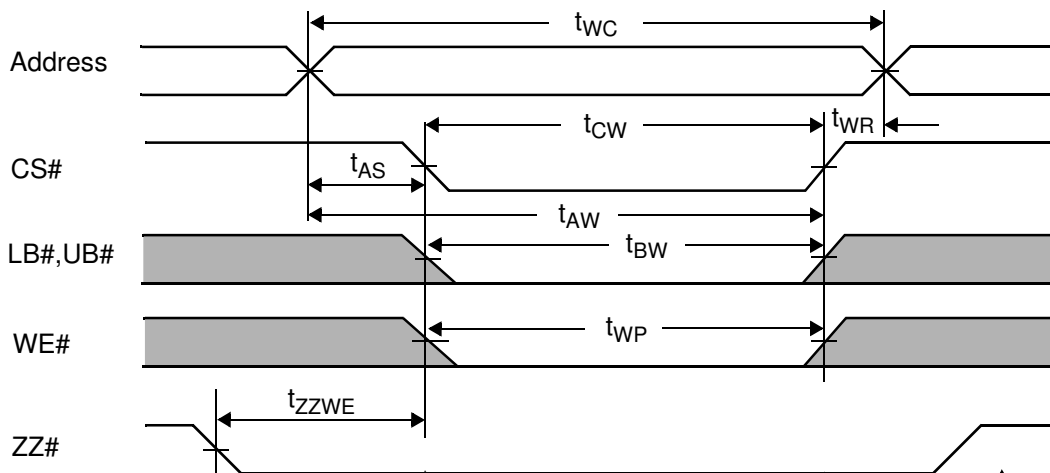
#### Array Refresh Area Selection

A1	A0	Type
0	0	Full Array (Default)
0	1	RFU (Reserved for future)
1	0	1/2 Array
1	1	1/4 Array

#### NOTES

1. The Partial Array Refresh and Deep Power Down mode is issued only during ZZ# low state.
2. The RMS (Reduced Memory Size) mode is enabled after ZZ# goes high and remains enabled after ZZ# goes high. To change to a different mode, the mode register will have to be re-written.
3. If register is written to enable the Deep Power Down, the part will go into Deep Power Down during the following time that ZZ# is driven low and there is no MRS update. When ZZ# is driven high, all of the register settings will return to default state for the part (i.e. full array refresh, Deep Power Down disabled.)

#### Mode Register Set Update Timing Diagram

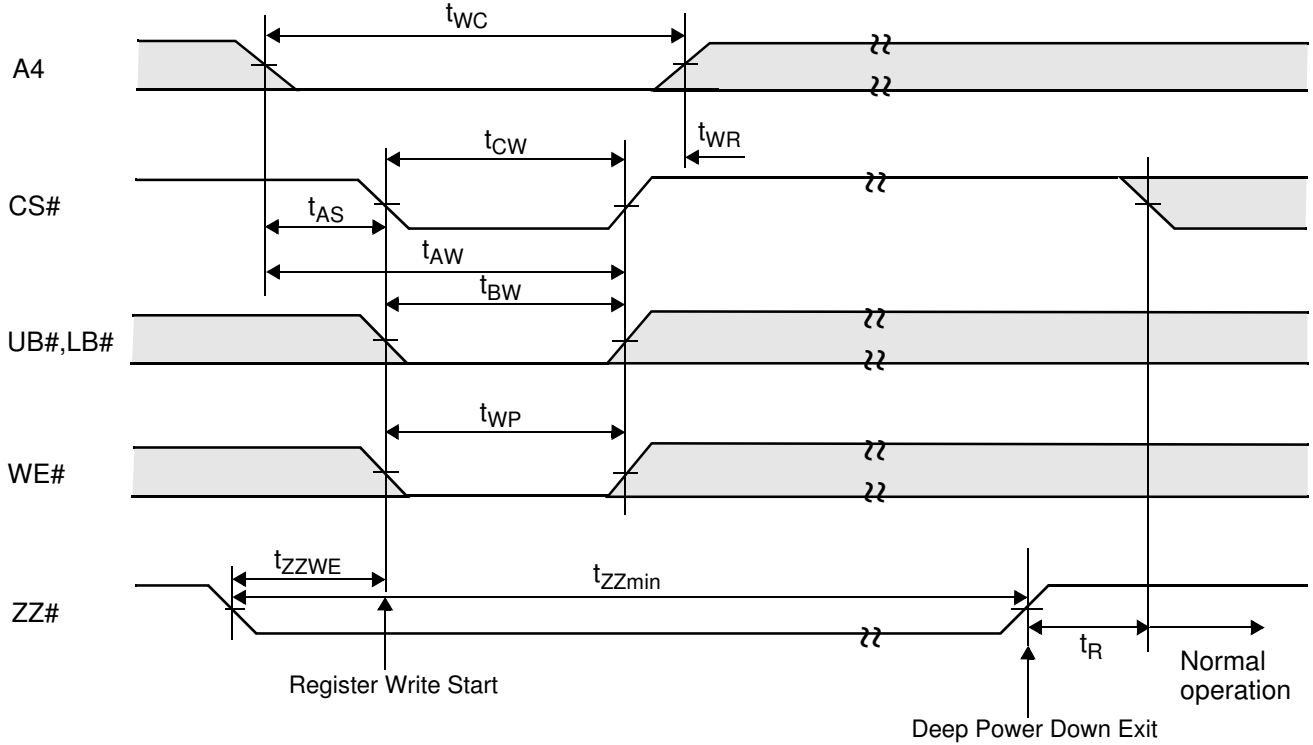


#### NOTES

The register update takes place after over the t<sub>ZZWE</sub> maximum time of 1us. Once the register is updated the next time ZZ# goes low, without any updates to the register starting within the t<sub>ZZWE</sub> maximum time of 1us, the part will refresh the array selected. The data bus is a don't care when ZZ# is low during the register updates.

## LOW POWER MODES

### Deep Power Down Mode Entry & Exit



Parameter	Description	Min	Max	Unit
$t_{ZZWE}$	ZZ# low to Write Enable Low	0	1	us
$t_R$ (Deep Power Down mode only)	Operation Recovery Time	200	-	us
$t_{ZZmin}$	Low Power Mode Time	10	-	us

## Address Information for PASR mode and RMS mode

### Partial Array Self Refresh Mode (A3=0, A4=1)

A2	A1	A0	Refresh Section	Address	Size	Density
0	1	1	1/4	000000h~07FFFFh	512Kb x 16	8Mb
0	1	0	1/2	000000h~0FFFFFFh	1Mb x 16	16Mb
X	0	0	Full	000000h~1FFFFFFh	2Mb x 16	32Mb
1	1	1	1/4	180000h~1FFFFFFh	512Kb x 16	8Mb
1	1	0	1/2	100000h~1FFFFFFh	1Mb x 16	16Mb

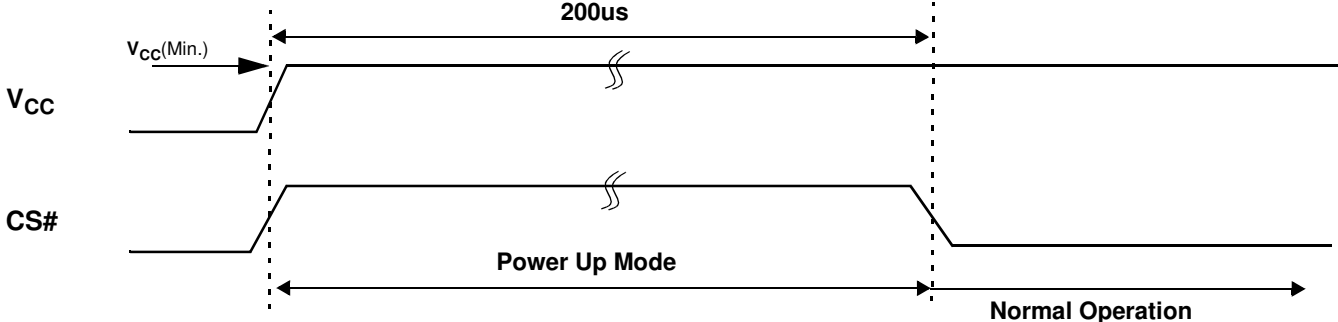
### Reduced Memory Size Mode (A3=1, A4=1)

A2	A1	A0	Refresh Section	Address	Size	Density
0	1	1	1/4	000000h~07FFFFh	512Kb x 16	8Mb
0	1	0	1/2	000000h~0FFFFFFh	1Mb x 16	16Mb
1	1	1	1/4	180000h~1FFFFFFh	512Kb x 16	8Mb
1	1	0	1/2	100000h~1FFFFFFh	1Mb x 16	16Mb

## Low Power Mode Characteristics

Parameter	Symbol	Test Conditions	Array	Min	Typ	Max	Unit
Deep Power Down Current	$I_{ZZ}$	$ZZ\# \leq 0.2V$ , Other inputs = 0 ~ $V_{CCQ}$ (Max. condition : $V_{CC}=3.3V$ @ $85^{\circ}C$ )	No Refresh	-	-	10	$\mu A$
Partial Array Refresh Mode Standby Current	$I_{ZZa}$		1/4 Array	-	-	65	$\mu A$
	$I_{ZZb}$	1/2 Array	-	-	75	$\mu A$	
Reduced Memory Size Mode Standby Current	$I_{SB1a}$	RMS mode. Other inputs = 0 ~ $V_{CCQ}$ (Max. condition : $V_{CC}=3.3V$ @ $85^{\circ}C$ )	1/4 Array	-	-	65	$\mu A$
	$I_{SB1b}$		1/2 Array	-	-	75	$\mu A$

**TIMING WAVEFORM OF POWER UP**

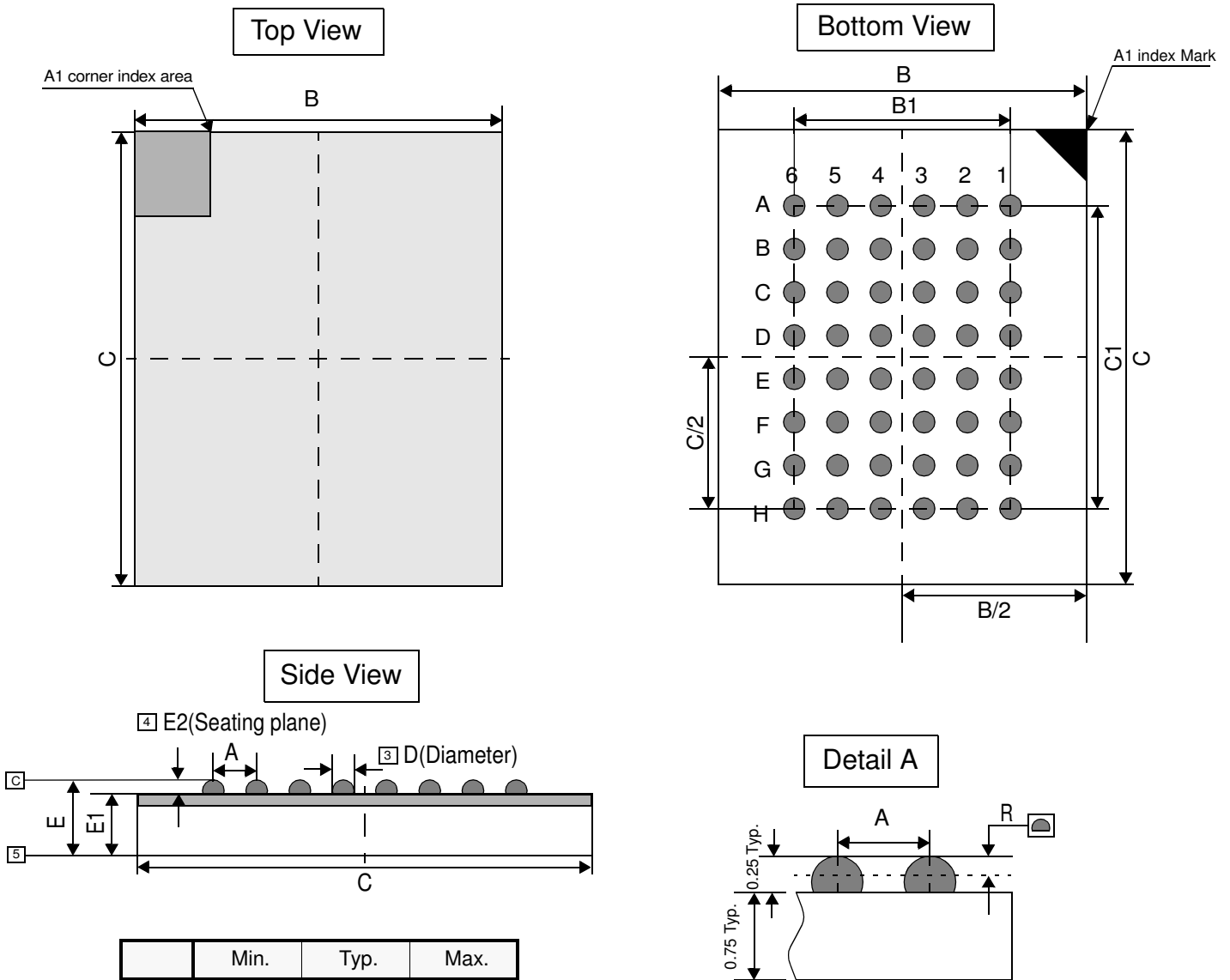


**NOTE ( POWER UP )**

- 1. After V<sub>CC</sub> reaches V<sub>CC(Min.)</sub> , wait 200us with CS# high. Then you get into the normal operation.

**PACKAGE DIMENSION**

48 Ball Fine Pitch BGA (0.75mm ball pitch)



	Min.	Typ.	Max.
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.00	1.10
E1	-	0.75	-
E2	0.20	0.25	0.30
R	-	-	0.08

**NOTES**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. All dimensions are millimeters.
3. Dimension "D" is measured at the maximum solder ball diameter in a plane parallel to datum C.
4. Primary datum C (Seating plane) is defined by the crown of the solder balls.
5. This is a controlling dimension.