

## **+1.8V to +5.5V, 2.5Ω, Single SPST Analog Switches**

The Intersil ISL54504 and ISL54505 devices are low ON-resistance, low voltage, bidirectional, single pole/single throw (SPST) analog switches designed to operate from a single +1.8V to +5.5V supply. Targeted applications include battery powered equipment that benefit from low  $r_{ON}$  resistance (2.5Ω), excellent  $r_{ON}$  flatness (0.6Ω), and fast switching speeds ( $t_{ON} = 25ns$ ,  $t_{OFF} = 15ns$ ). The digital logic input is 1.8V CMOS compatible when using a single +3V supply.

Cell phones, for example, often face ASIC functionality limitations. The number of analog input or GPIO pins may be limited and digital geometries are not well suited to analog switch performance. This family of parts may be used to switch in additional functionality while reducing ASIC design risk. The ISL54054, ISL54055 are offered in a 6 Ld 1.2mmx1.0mmx0.4mm pitch μTDFN package, alleviating board space limitations.

The ISL54504 has one normally open (NO) switch and ISL54505 has one normally closed (NC) switch.

**TABLE 1. FEATURES AT A GLANCE**

	<b>ISL54504</b>	<b>ISL54505</b>
<b>Number of Switches</b>	1	1
<b>SW</b>	NO	NC
<b>1.8V <math>r_{ON}</math></b>	6Ω	6Ω
<b>1.8V <math>t_{ON}/t_{OFF}</math></b>	65ns/40ns	65ns/40ns
<b>3V <math>r_{ON}</math></b>	4Ω	4Ω
<b>3V <math>t_{ON}/t_{OFF}</math></b>	30ns/20ns	30ns/20ns
<b>5V <math>r_{ON}</math></b>	2.5Ω	2.5Ω
<b>5V <math>t_{ON}/t_{OFF}</math></b>	25ns/15ns	25ns/15ns
<b>Package</b>	6 Ld μTDFN	

## **Features**

- ON-resistance ( $r_{ON}$ )
  - $V_{CC} = +5.0V$  ..... 2.5Ω
  - $V_{CC} = +3.0V$  ..... 4.0Ω
  - $V_{CC} = +1.8V$  ..... 7.0Ω
- $r_{ON}$  flatness (+4.5V Supply) ..... 0.6Ω
- Single supply operation ..... +1.8V to +5.5V
- Fast switching action (+4.5V Supply)
  - $t_{ON}$  ..... 25ns
  - $t_{OFF}$  ..... 15ns
- ESD HBM rating ..... 6kV
- 1.8V CMOS logic compatible (+3V supply)
- Available in 6 Ld μTDFN Package
- Pb-free available (RoHS compliant)

## **Applications**

- Battery powered, handheld, and portable equipment
  - Cellular/mobile phones
  - Pagers
  - Laptops, notebooks, palmtops
- Portable Test and Measurement
- Medical Equipment
- Audio and video switching

## **Related Literature**

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

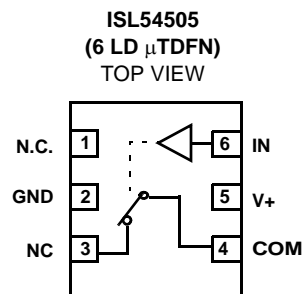
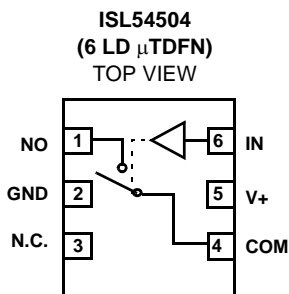
## Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54504IRUZ-T*	4	-40 to +85	6 Ld $\mu$ TDFN (Tape and Reel)	L6.1.2x1.0A
ISL54505IRUZ-T*	5	-40 to +85	6 Ld $\mu$ TDFN (Tape and Reel)	L6.1.2x1.0A

\*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Pinouts (Note 1)



NOTE:

1. Switches Shown for Logic "0" Input.

## Truth Table

LOGIC	ISL54504	ISL54505
0	Off	On
1	On	Off

NOTE: Logic "0"  $\leq 0.5V$ . Logic "1"  $\geq 1.4V$  with a 3V supply.

## Pin Descriptions

PIN NAME	FUNCTION
V+	System Power Supply Input (+1.8V to +5.5V)
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin
N.C.	No Connect

## Absolute Maximum Ratings

V+ to GND	-0.5V to 6.5V
Input Voltages	
NO, NC, IN (Note 2)	-0.5V to ((V+) + 0.5V)
Output Voltages	
COM (Note 2)	-0.5V to ((V+) + 0.5V)
Continuous Current NO, NC, or COM	±300mA
Peak Current NO, NC, or COM (Pulsed 1ms, 10% Duty Cycle, Max)	± 600mA
ESD Rating	
Human Body Model	>6kV
Machine Model	>300V
Charged Device Model	>1400V

## Thermal Information

Thermal Resistance (Typical, Notes 3, 4)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
6 Ld $\mu$ TDFN Package	239.2	111.6
Maximum Junction Temperature (Plastic Package)	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Pb-free reflow profile	see link below	
<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>		

## Operating Conditions

V+ (Positive DC Supply Voltage)	1.8V to 5.5V
Analog Signal Range	0V to V+
V <sub>IN</sub> (Digital Logic Input Voltage (IN))	0V to V+
Temperature Range	
ISL54504IRUZ, ISL54505IRUZ	-40°C to +85°C

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

- Signals on NC, NO, IN, or COM exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.

## Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V<sub>INH</sub> = 2.0V, V<sub>INL</sub> = 0.8V (Note 5), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 6, 7)	TYP	MAX (Notes 6, 7)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V <sub>ANALOG</sub>		Full	0	-	V+	V
ON-Resistance, r <sub>ON</sub>	V+ = 4.5V, I <sub>COM</sub> = 100mA, V <sub>NO</sub> or V <sub>NC</sub> = 0V to V+, (Note 9, See Figure 4)	25	-	2.2	2.5	Ω
		Full	-	-	3	Ω
r <sub>ON</sub> Flatness, r <sub>FLAT(ON)</sub>	V+ = 4.5V, I <sub>COM</sub> = 100mA, V <sub>NO</sub> or V <sub>NC</sub> = 0V to V+, (Notes 8, 9)	25	-	0.6	0.65	Ω
		Full	-	-	0.7	Ω
NO or NC OFF Leakage Current, I <sub>NO(OFF)</sub> or I <sub>NC(OFF)</sub>	V+ = 5.5V, V <sub>COM</sub> = 0.3V, 5V, V <sub>NO</sub> or V <sub>NC</sub> = 5V, 0.3V	25	-25	1.5	25	nA
		Full	-150	-	150	nA
COM ON Leakage Current, I <sub>COM(ON)</sub>	V+ = 5.5V, V <sub>COM</sub> = 0.3V, 5V, or V <sub>NO</sub> or V <sub>NC</sub> = 0.3V, 5V, or Floating	25	-30	2.8	30	nA
		Full	-300	-	300	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t <sub>ON</sub>	V+ = 4.5V, V <sub>NO</sub> or V <sub>NC</sub> = 3.0V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF (See Figure 1, Note 9)	25	-	25	-	ns
		Full	-	25	-	ns
Turn-OFF Time, t <sub>OFF</sub>	V+ = 4.5V, V <sub>NO</sub> or V <sub>NC</sub> = 3.0V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF (See Figure 1, Note 9)	25	-	15	-	ns
		Full	-	16	-	ns
Break-Before-Make Time Delay, t <sub>D</sub>	V+ = 5.5V, V <sub>NO</sub> or V <sub>NC</sub> = 3.0V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF (See Figure 3, Note 9)	Full	-	15	-	ns
Charge Injection, Q	V <sub>G</sub> = 0V, R <sub>G</sub> = 0Ω, C <sub>L</sub> = 1.0nF (See Figure 2)	25	-	24	-	pC
OFF Isolation	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, f = 1MHz, V <sub>COM</sub> = 1V <sub>P-P</sub> (See Figure 3)	25	-	70	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V <sub>COM</sub> = 2V <sub>P-P</sub> , R <sub>L</sub> = 32Ω	25	-	0.15	-	%
Total Harmonic Distortion	f = 20Hz to 20kHz, V <sub>COM</sub> = 2V <sub>P-P</sub> , R <sub>L</sub> = 600Ω	25	-	0.014	-	%
-3dB Bandwidth	Signal = 0dBm, R <sub>L</sub> = 50Ω	25	-	250	-	MHz
NO or NC OFF Capacitance, C <sub>OFF</sub>	V+ = 4.5V, f = 1MHz, V <sub>NO</sub> or V <sub>NC</sub> = V <sub>COM</sub> = 0V (See Figure 5)	25	-	7	-	pF
COM ON Capacitance, C <sub>COM(ON)</sub>	V+ = 4.5V, f = 1MHz, V <sub>NO</sub> or V <sub>NC</sub> = V <sub>COM</sub> = 0V (See Figure 5)	25	-	18	-	pF

**Electrical Specifications - 5V Supply**

Test Conditions:  $V_+ = +4.5V$  to  $+5.5V$ ,  $GND = 0V$ ,  $V_{INH} = 2.0V$ ,  $V_{INL} = 0.8V$  (Note 5),  
Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 6, 7)	TYP	MAX (Notes 6, 7)	UNITS
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.8	-	5.5	V
Positive Supply Current, I+	V+ = 5.5V, VIN = 0V or V+	25	-	0.028	0.1	μA
		Full	-	1.1	2.5	μA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, VINL		Full	-	-	0.8	V
Input Voltage High, VINH		Full	2.4	-	-	V
Input Current, IINH, IINL	V+ = 5.5V, VIN = 0V or V+	Full	-0.1	0.053	0.1	μA

**Electrical Specifications - 3V Supply**

Test Conditions:  $V_+ = +2.7V$  to  $+3.6V$ ,  $GND = 0V$ ,  $V_{INH} = 1.4V$ ,  $V_{INL} = 0.5V$  (Note 5),  
Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 6, 7)	TYP	MAX (Notes 6, 7)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V <sub>ANALOG</sub>		Full	0	-	V+	V
ON-Resistance, r <sub>ON</sub>	V+ = 2.7V, I <sub>COM</sub> = 100mA, V <sub>NO</sub> or V <sub>NC</sub> = 0V to V+, (Note 9, See Figure 4)	25	-	3.3	3.5	Ω
		Full	-	-	4.5	Ω
r <sub>ON</sub> Flatness, r <sub>FLAT(ON)</sub>	V+ = 2.7V, I <sub>COM</sub> = 100mA, V <sub>NO</sub> or V <sub>NC</sub> = 0V to V+, (Notes 7, 9)	25	-	1	1.1	Ω
		Full	-	-	1.2	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t <sub>ON</sub>	V+ = 2.7V, V <sub>NO</sub> or V <sub>NC</sub> = 1.5V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF (See Figure 1, Note 9)	25	-	30	-	ns
		Full	-	30	-	ns
Turn-OFF Time, t <sub>OFF</sub>	V+ = 2.7V, V <sub>NO</sub> or V <sub>NC</sub> = 1.5V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF (See Figure 1, Note 9)	25	-	20	-	ns
		Full	-	20	-	ns
Charge Injection, Q	V <sub>G</sub> = 0V, R <sub>G</sub> = 0Ω, C <sub>L</sub> = 1.0nF (See Figure 2)	25	-	16	-	pC
OFF Isolation	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF, f = 1MHz, V <sub>COM</sub> = 1V <sub>P-P</sub> (See Figure 3)	25	-	-70	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V <sub>COM</sub> = 2V <sub>P-P</sub> , R <sub>L</sub> = 32Ω	25	-	0.36	-	%
Total Harmonic Distortion	f = 20Hz to 20kHz, V <sub>COM</sub> = 2V <sub>P-P</sub> , R <sub>L</sub> = 600Ω	25	-	0.03	-	%
-3dB Bandwidth	Signal = 0dBm, R <sub>L</sub> = 50Ω	25	-	250	-	MHz
NO or NC OFF Capacitance, C <sub>OFF</sub>	f = 1MHz, V <sub>NO</sub> or V <sub>NC</sub> = V <sub>COM</sub> = 0V (See Figure 5)	25	-	6	-	pF
COM OFF Capacitance, C <sub>COM(OFF)</sub>	f = 1MHz, V <sub>NO</sub> or V <sub>NC</sub> = V <sub>COM</sub> = 0V (See Figure 5)	25	-	15	-	pF
COM ON Capacitance, C <sub>COM(ON)</sub>	f = 1MHz, V <sub>NO</sub> or V <sub>NC</sub> = V <sub>COM</sub> = 0V (See Figure 5)	25	-	18	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 3.6V, V <sub>IN</sub> = 0V or V+	25	-	0.013	-	μA
		Full	-	0.7	-	μA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V <sub>INL</sub>		Full	-	-	0.5	V
Input Voltage High, V <sub>INH</sub>		Full	1.4	-	-	V
Input Current, I <sub>INH</sub> , I <sub>INL</sub>	V+ = 3.6V, V <sub>IN</sub> = 0V or V+	Full	-0.1	0.058	0.1	μA

# Electrical Specifications - 1.8V Supply

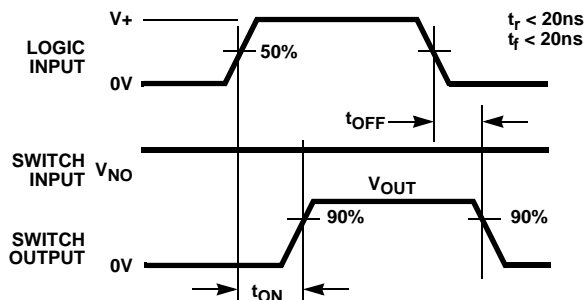
Test Conditions:  $V_+ = +1.8V$ ,  $GND = 0V$ ,  $V_{INH} = 1V$ ,  $V_{INL} = 0.4V$  (Note 5),  
Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 6, 7)	TYP	MAX (Notes 6, 7)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V <sub>ANALOG</sub>		Full	0	-	V+	V
ON-Resistance, r <sub>ON</sub>	V+ = 1.8V, I <sub>COM</sub> = 10mA, V <sub>NO</sub> or V <sub>NC</sub> = 0V to V+ (Note 9, See Figure 4)	25	-	6	6.5	Ω
		Full	-	-	7	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t <sub>ON</sub>	V+ = 1.8V, V <sub>NO</sub> or V <sub>NC</sub> = 1.5V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF (See Figure 1, Note 9)	25	-	65	-	ns
		Full	-	95	-	ns
Turn-OFF Time, t <sub>OFF</sub>	V+ = 1.8V, V <sub>NO</sub> or V <sub>NC</sub> = 1.5V, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 35pF (See Figure 1, Note 9)	25	-	40	-	ns
		Full	-	65	-	ns
Charge Injection, Q	V <sub>G</sub> = V+/2, R <sub>G</sub> = 0Ω, C <sub>L</sub> = 1.0nF (See Figure 2)	25	-	8.2	-	pC
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V <sub>INL</sub>		Full	-	-	0.4	V
Input Voltage High, V <sub>INH</sub>		Full	1	-	-	V

## NOTES:

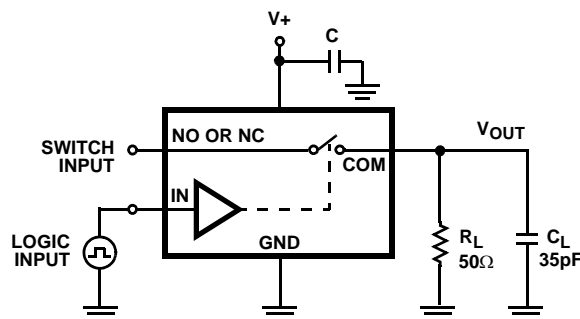
- $V_{IN}$  = input voltage to perform proper function.
- The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.
- Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
- Limits established by characterization and are not production tested.

## Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches.  $C_L$  includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO \text{ or } NC)} \frac{R_L}{R_L + r_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

Test Circuits and Waveforms (Continued)

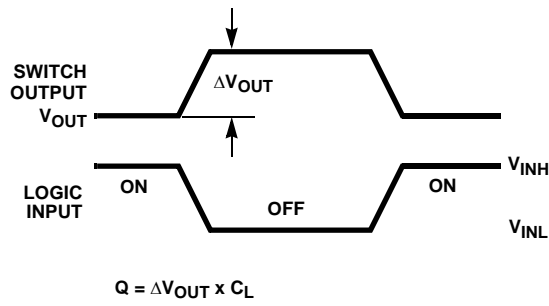


FIGURE 2A. MEASUREMENT POINTS

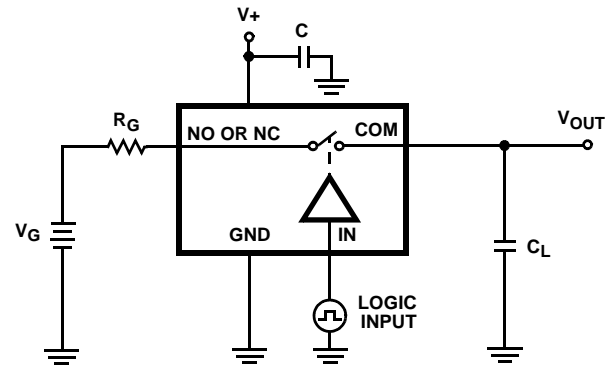


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

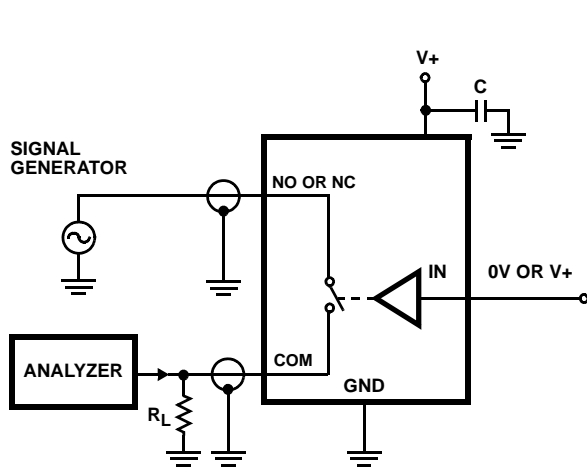


FIGURE 3. OFF ISOLATION TEST CIRCUIT

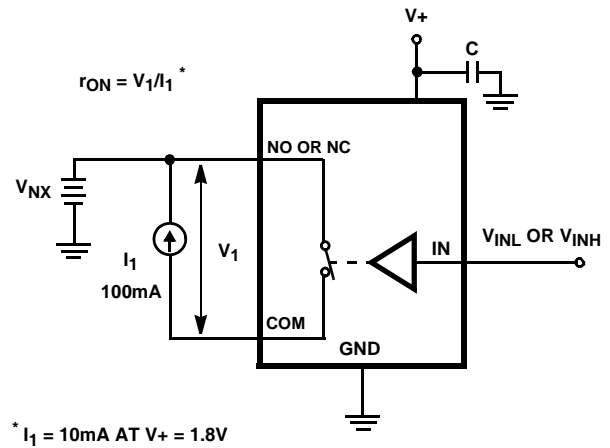


FIGURE 4.  $r_{ON}$  TEST CIRCUIT

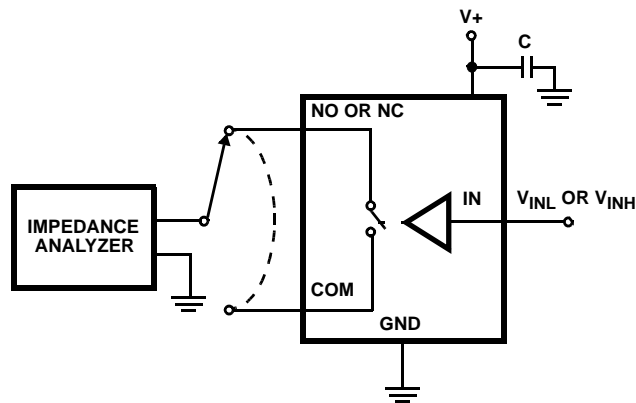


FIGURE 5. CAPACITANCE TEST CIRCUIT



The minimum recommended supply voltage is 1.8V but the part will operate with a supply below 1.8V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the “Electrical Specifications” tables starting on page 3 and the “Typical Performance Curves” starting on page 8 for details.

V+ and GND also power the internal logic and level shifter. The level shifter converts the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies because the input switching point becomes negative in this configuration.

### Logic-Level Thresholds

This switch family is 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 2V to 3.6V (see Figure 14). At 3.6V the  $V_{IH}$  level is about 0.95V. This is still below the 1.8V CMOS guaranteed high output minimum level of 1.4V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

### High-Frequency Performance

In 50Ω systems, the ISL54504/ISL54505 has a -3dB bandwidth of 250MHz (see Figure 15). The frequency response is very consistent over a wide V+ range and for varying analog signal levels.

An OFF switch behaves like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch’s input to output. Off isolation is the resistance of this signal feedthrough. Figure 16 details the high off isolation provided by the ISL54504/ISL54505. At 1MHz, off isolation is about 70dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease off isolation due to the voltage divider action of the switch OFF impedance and the load impedance.

### Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

### Typical Performance Curves $T_A = +25^\circ\text{C}$ , Unless Otherwise Specified.

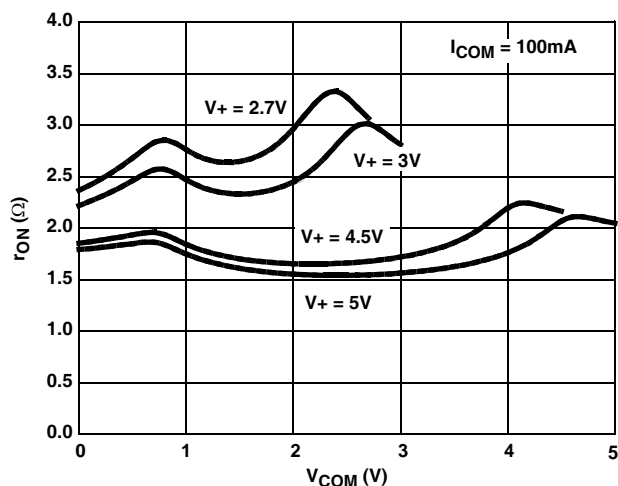


FIGURE 8. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

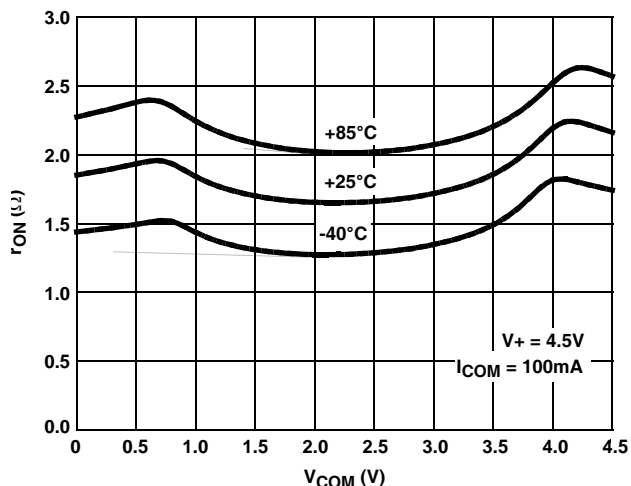


FIGURE 9. ON-RESISTANCE vs SWITCH VOLTAGE

**Typical Performance Curves**  $T_A = +25^\circ\text{C}$ , Unless Otherwise Specified. (Continued)

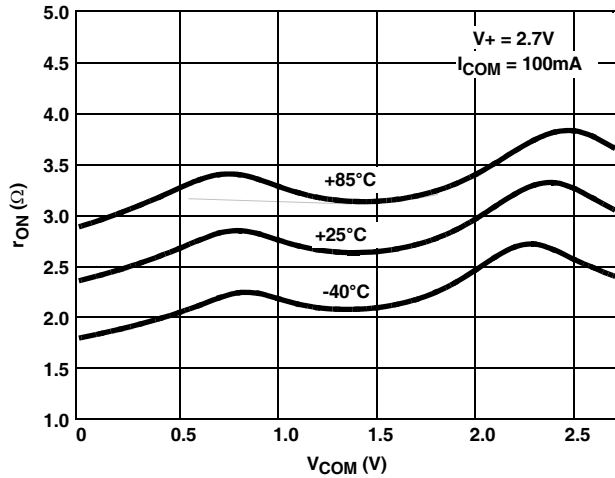


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

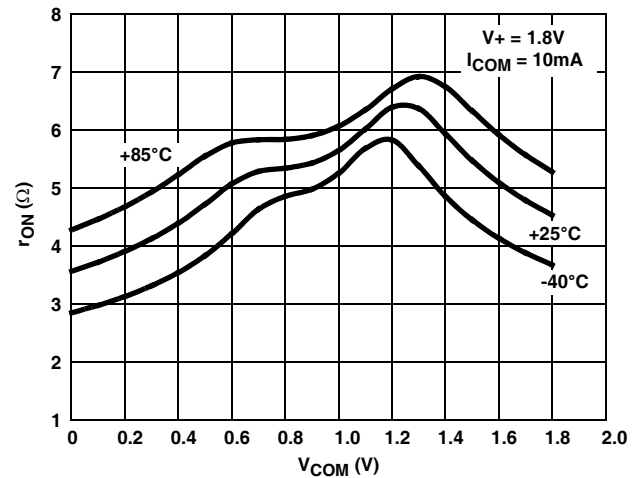


FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE

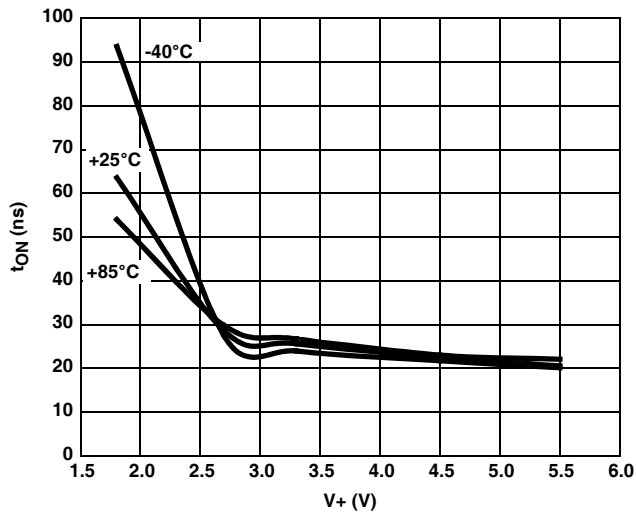


FIGURE 12. TURN-ON TIME vs SUPPLY VOLTAGE

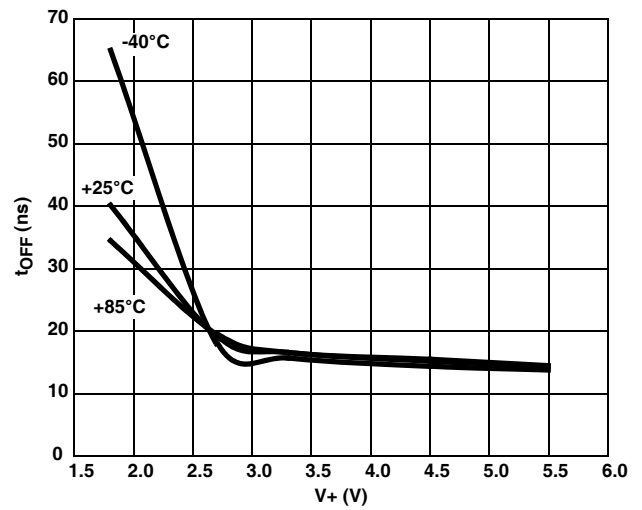


FIGURE 13. TURN-OFF TIME vs SUPPLY VOLTAGE

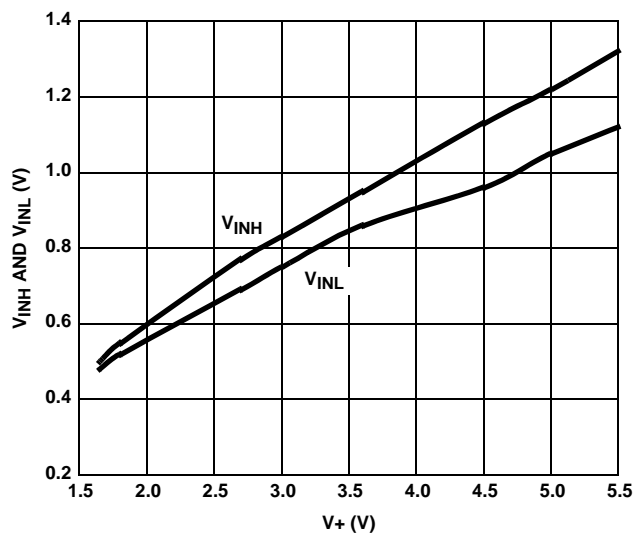


FIGURE 14. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

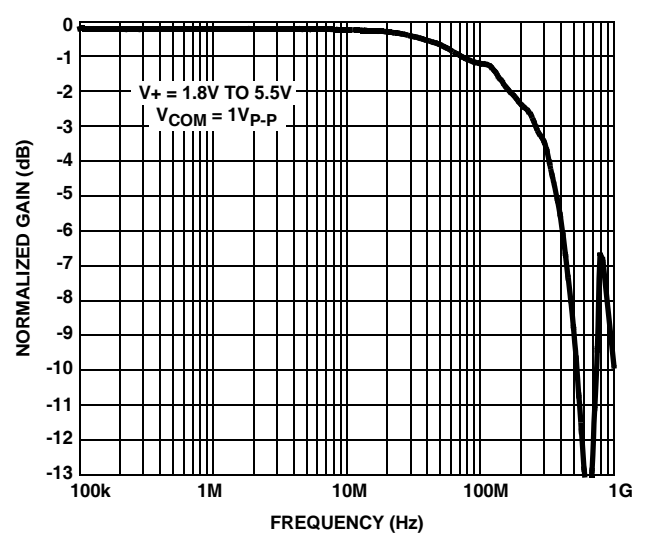


FIGURE 15. FREQUENCY RESPONSE

**Typical Performance Curves**  $T_A = +25^\circ\text{C}$ , Unless Otherwise Specified. (Continued)

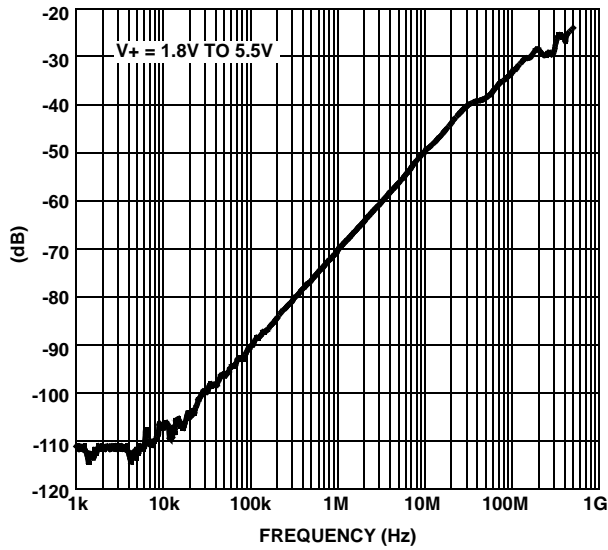


FIGURE 16. OFF ISOLATION

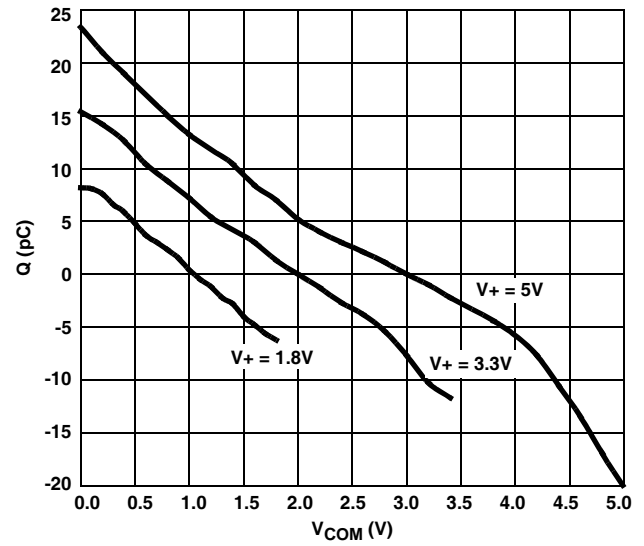


FIGURE 17. CHARGE INJECTION vs SWITCH VOLTAGE

**Die Characteristics**

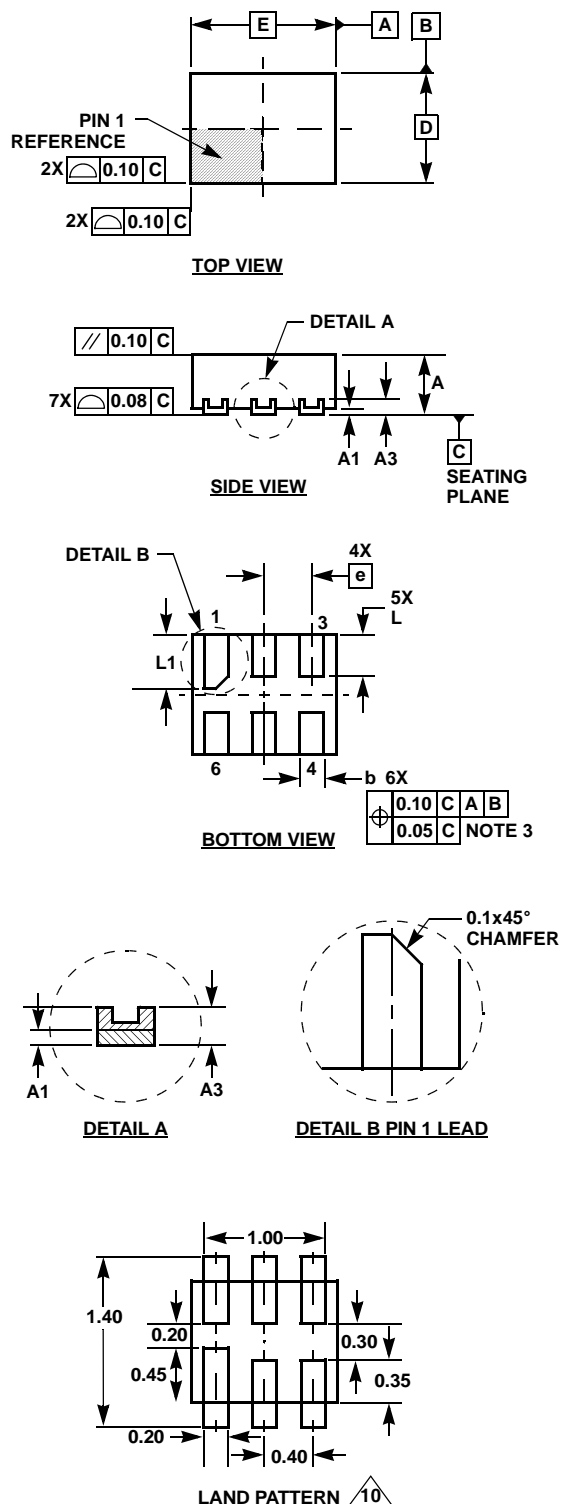
SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

PROCESS:

Submicron CMOS

**Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)****L6.1.2x1.0A****6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE**

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3	0.127 REF			-
b	0.15	0.20	0.25	5
D	0.95	1.00	1.05	-
E	1.15	1.20	1.25	-
e	0.40 BSC			-
L	0.30	0.35	0.40	-
L1	0.40	0.45	0.50	-
N	6			2
Ne	3			3
θ	0	-	12	4

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**NOTES:**

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Ne refers to the number of terminals on E side.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

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Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

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