1. General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS design technology combines higher speeds and smaller size with the low power and high noise immunity of CMOS.

On chip memory system includes 0.5 K(for MDT2005) bytes of ROM, and 32 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software :

- ◆ Fully CMOS static design
- ◆ 8-bit data bus
- ◆ On chip ROM size : 512 words for MDT2005
- ◆ Internal RAM size : 32 bytes

(25 general purpose registers, 7 special registers)

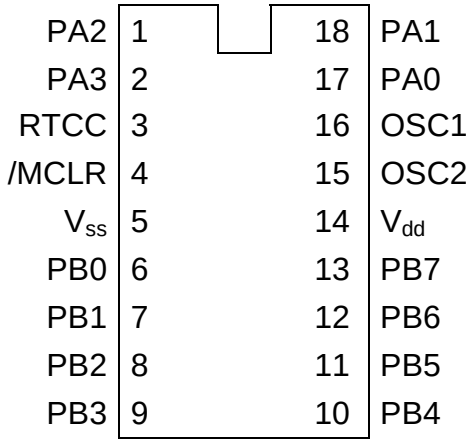
- ◆ 36 single word instructions
- ◆ 14-bit instructions
- ◆ 2-level stacks
- ◆ Operating voltage : 2.3V ~ 6.0 V
- ◆ Operating frequency : 0 ~ 20 MHz
- ◆ The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- ◆ Addressing modes include direct, indirect and relative addressing modes
- ◆ Power-on Reset (POR), only available while PED is Disable
- ◆ Power edge-detector Reset (PED)
- ◆ Sleep Mode for power saving
- ◆ 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler
- ◆ 4 types of oscillator can be selected by programming option:
  - RC－Low cost RC oscillator
  - LFXT－Low frequency crystal oscillator
  - XTAL－Standard crystal oscillator
  - HFXT－High frequency crystal oscillator
- ◆ 4 oscillator start-up time can be selected by programming option:
  - 150 μs, 20 ms, 40 ms, 80 ms
- ◆ On-chip RC oscillator based Watchdog Timer(WDT) can be operated freely
- ◆ 12 I/O pins with their own independent direction control

3. Applications

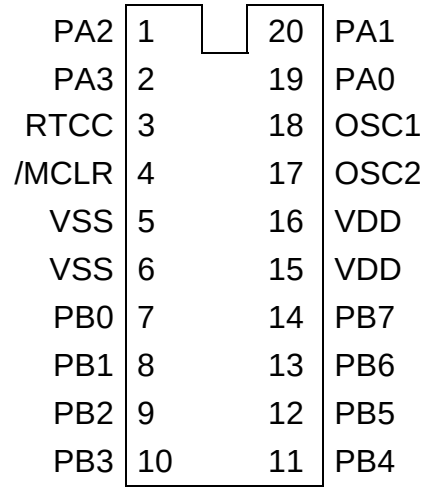
The application areas of this MDT2005 range from appliance motor control and high speed automotive to low power remote transmitters/receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral … etc.

4. Pin Assignment

DIP / SOP



SSOP



5. Pin Function Description

Pin Name	I/O	Function Description
PA0~PA3	I/O	Port A, TTL input level
PB0~PB7	I/O	Port B, TTL input level
RTCC	I	Real Time Clock/Counter, Schmitt Trigger input levels
/MCLR	I	Master Clear, Schmitt Trigger input levels
OSC1	I	Oscillator Input
OSC2	O	Oscillator Output
V_{dd}		Power supply
V_{ss}		Ground

6. Memory Map

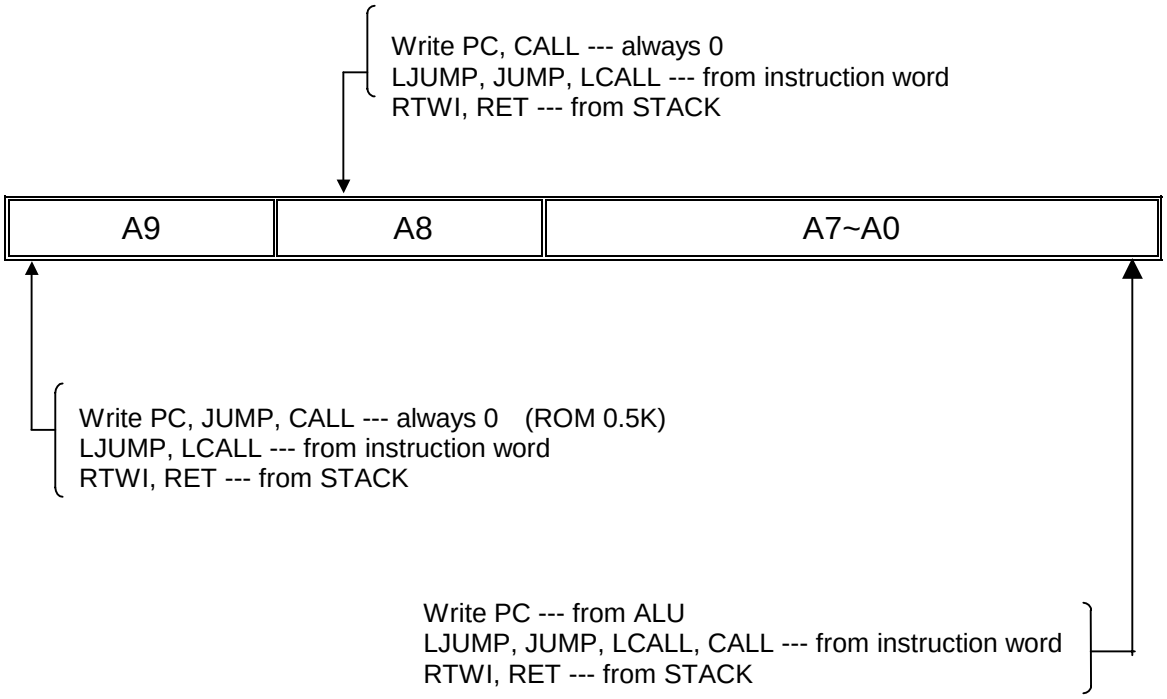
(A) Register Map

Address	Description
00	Indirect Addressing Register
01	RTCC
02	PC
03	STATUS
04	MSR
05	Port A
06	Port B
07~1F	Internal RAM, General Purpose Register

(1) IAR (Indirect Address Register) : R0

(2) RTCC (Real Time Counter/Counter Register) : R1

(3) PC (Program Counter) : R2



(4) STATUS (Status register) : R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power loss Flag bit
4	TF	Time overflow Flag bit
5-7	——	General purpose bit

(5) MSR (Memory Select Register) : R4

(6) PORT A : R5

PA3~PA0, I/O Register

(7) PORT B : R6

PB7~PB0, I/O Register

(8) TMR (Time Mode Register)

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2—0	PS2—0	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer		
4	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin		

(9) CPIO A, CPIO B (Control Port I/O Mode Register)
The CPIO register is “write-only”
＝“0”, I/O pin in output mode;
＝“1”, I/O pin in input mode.

(10) EPROM Option by writer programming :

Oscillator Type	Oscillator Start-up Time
RC Oscillator	150 μs,20ms,40ms,80ms
HFXT Oscillator	20 ms,40ms,80ms
XTAL Oscillator	20ms,40 ms,80ms
LFXT Oscillator	40 ms,80 ms

Watchdog Timer control
Watchdog timer disable all the time
Watchdog timer enable all the time

Power Edge Detect
PED Disable
PED Enable

Security bit
Security weak Disable
Security Disable
Security Enable

The default EPROM security is weak disable. Once the IC was set in enable or disable, it’s forbidden to set in disable or enable again.

(B) Program Memory

Address	Description
000-1FF	Program memory for MDT2005
1FF	The starting address of the power on, external reset or WDT for MDT2005

7. Reset Condition for all Registers

Register	Address	Power-On Reset	/MCLR or WDT Reset
CPIO A	－－	1111 1111	1111 1111
CPIO B	－－	1111 1111	1111 1111
TMR	－－	--11 1111	--11 1111
IAR	00h	－	－
RTCC	01h	xxxx xxxx	uuuu uuuu
PC	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000# #uuu
MSR	04h	111x xxxx	111u uuuu
PORT A	05h	- - - - xxxx	- - - - uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu

Note : u＝unchanged, x＝unknown, - ＝unimplemented, read as “0”
#＝value depends on the condition of the following table

Condition	Status: bit 4	Status: bit 3
/MCLR reset (not during SLEEP)	u	u
/MCLR reset during SLEEP	1	0
WDT reset (not during SLEEP)	0	1
WDT reset during SLEEP	0	0

8. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000100	RET	Return	Stack→PC	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI I	Load immediate to W	I→W	None

Instruction Code	Mnemonic Operands	Function	Operating	Status
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔ R(4~7)]→t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R – W→t (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R – 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C →R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1),C→ R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
1000nn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
1010nn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110000 nnnnnnnn	CALL n	Call subroutine	n→PC, PC+1→Stack	None
110001 iiiiiiii	RTWI i	Return, place immediate to W	Stack→PC, i→W	None
11001n nnnnnnnn	JUMP n	JUMP to address	n→PC	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register		0	: Working register
CPIO	:	Control I/O port register		1	: General register

TF	:	Timer overflow flag	R	:	General register address
PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter	HC	:	Half carry
OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive '∪'	/	:	Complement
Exclu.	:	Exclusive '⊕'	x	:	Don't care
AND	:	Logic AND '∩'	i	:	Immediate data (8 bits)
			n	:	Immediate address

9. Electrical Characteristics

(A) Operating Voltage & Frequency

V_{dd} ： 2.3V ~ 6.0 V

Frequency：0 Hz ~ 20 MHz

(B) Input Voltage

@ V_{dd}＝5.0 V, Temperature＝25 ℃

	Port	Min.	Max.
V_{il}	PA, PB	V_{ss}	1.0 V
	RTCC, /MCLR	V_{ss}	1.0V
V_{ih}	PA, PB	2.0 V	V_{dd}
	RTCC, /MCLR	3.2 V	V_{dd}

∗Threshold Voltage :

Port A, Port B V_{th}＝1.5V

RTCC, /MCLR V_{il}＝1.2 V, V_{ih}＝2.9 V (Schmitt Trigger)

(C) Output Voltage：

@ V_{dd}＝5.0 V, Temperature＝25 ℃, the typical value as followings :

PA, PB Port	
I_{oh}＝－20.0 mA	V_{oh}＝3.7 V
I_{ol}＝20.0 mA	V_{ol}＝0.5 V
I_{oh}＝－5.0 mA	V_{oh}＝4.7 V
I_{ol}＝5.0 mA	V_{ol}＝0.2 V

(D) Leakage Current

@ V_{dd}＝5.0 V, Temperature＝25 ℃, the typical value as followings :

I_{il}	－ 0.1μA (Max.)
I_{ih}	＋ 0.1μA (Max.)

(E) Sleep Current

@WDT－Disable, Temperature＝25 ℃, the typical value as followings :

V_{dd}＝2.3 V	I_{dd}＜0.1 μA
V_{dd}＝3.0 V	I_{dd}＜0.1 μA
V_{dd}＝4.0 V	I_{dd}＜0.1.μA
V_{dd}＝5.0 V	I_{dd}＜0.1 μA
V_{dd}＝6.0V	I_{dd}＜0.1 μA

@WDT－Enable, Temperature＝25 ℃, the typical value as followings :

V_{dd}＝2.3 V	I_{dd}＜1.0 μA
V_{dd}＝3.0 V	I_{dd}＝3.0 μA
V_{dd}＝4.0 V	I_{dd}＝8.0 μA
V_{dd}＝5.0 V	I_{dd}＝15.0 μA
V_{dd}＝6.0 V	I_{dd}＝25.0 μA

(F) Operating Current

Temperature＝25 ℃, the typical value as followings :

(i) OSC Type＝RC (OSC1&OSC2 Internal Cap about 10P);　WDT－Enable;

The IC may not oscillate properly if the resistance of rext less than 4.7K.

The minimum resistance of rext must be more than 4.7K.

@ V_{dd}＝5.0 V

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
0P	4.7 K	11 M	1.1 mA
	10.0 K	5.2 M	650 μA
	47.0 K	1.37 M	250 μA
	100.0 K	650 K	175 μA
	300.0 K	220 K	135 μA
	470.0 K	140 K	130 μA

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
3P	4.7 K	9.4 M	1.1 mA
	10.0 K	4.45 M	550 μA
	47.0 K	1.1 M	230 μA
	100.0 K	540 K	165 μA
	300.0 K	180 K	135 μA
	470.0 K	115 K	125 μA
20P	4.7 K	5.5 M	660 μA
	10.0 K	2.5 M	365 μA
	47.0 K	615 K	185 μA
	100.0 K	300 K	155 μA
	300.0 K	100 K	135 μA
	470.0 K	63.5 K	125 μA
100P	4.7 K	2.0 M	315 μA
	10.0 K	910 K	200 μA
	47.0 K	222 K	135 μA
	100.0 K	105 K	125 μA
	300.0 K	36 K	120 μA
	470.0 K	22 K	115 μA
300P	4.7 K	870 K	195 μA
	10.0 K	380 K	150 μA
	47.0 K	93 K	120 μA
	100.0 K	44 K	115 μA
	300.0 K	15 K	110 μA
	470.0 K	9.4 K	108 μA

(ii) OSC Type＝LF (OSC1&OSC2 Internal cap.); WDT－Disable ;PED=Enable

Voltage/Frequency	32 K (Ext C=50P)	455 K (Ext C=50P)	1 M	Sleep
2.3 V	10 μA	21 μA	@2.5V 35 μA	＜0.1 μA
3.0 V	18 μA	40 μA	50 μA	＜0.1 μA
4.0 V	35 μA	70 μA	85 μA	＜0.1 μA
5.0 V	60 μA	110 μA	130 μA	＜0.1 μA
6.0 V	120 μA	180 μA	250 μA	＜0.1 μA

(iii) OSC Type＝XT (OSC1&OSC2 Internal cap. about 10P);　WDT－Enable

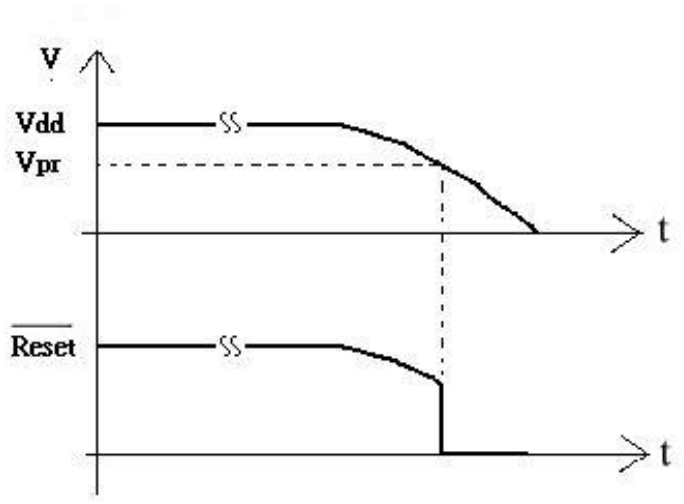
Voltage/Frequency	1 M	4 M	10 M	Sleep
2.1 V	35 μA	105 μA	240 μA	＜1.0 μA
3.0 V	80 μA	185 μA	380 μA	3 μA
4.0 V	155 μA	305 μA	600 μA	8 μA
5.0 V	260 μA	450 μA	880 μA	15 μA
6.0 V	410 μA	700 μA	1.2 mA	25 μA

(iv) OSC Type＝HF (OSC1&OSC2 Internal cap. about 10P);　WDT－Enable

Voltage/Frequency	4 M	10 M	20 M	Sleep
2.1 V	110 μA	240 μA	@2.5V 550μA	＜1.0 μA
3.0 V	210 μA	410 μA	730 μA	3 μA
4.0 V	350 μA	640 μA	1.1 mA	8 μA
5.0 V	530 μA	950 μA	1.6 mA	15 μA
6.0 V	850 μA	1.3 mA	2.3 mA	25 μA

(G) Power Edge-detector Reset Voltage (Not in Sleep Mode), @ V_{dd}＝5.0 V(PED：Enable)

V_{pr}≦1.6~1.8 V　　V_{pr} ： V_{dd} (Power Supply)



PS.IF PED_Enable then Internal Power_on_reset will be off

(H) The basic WDT time-out cycle time

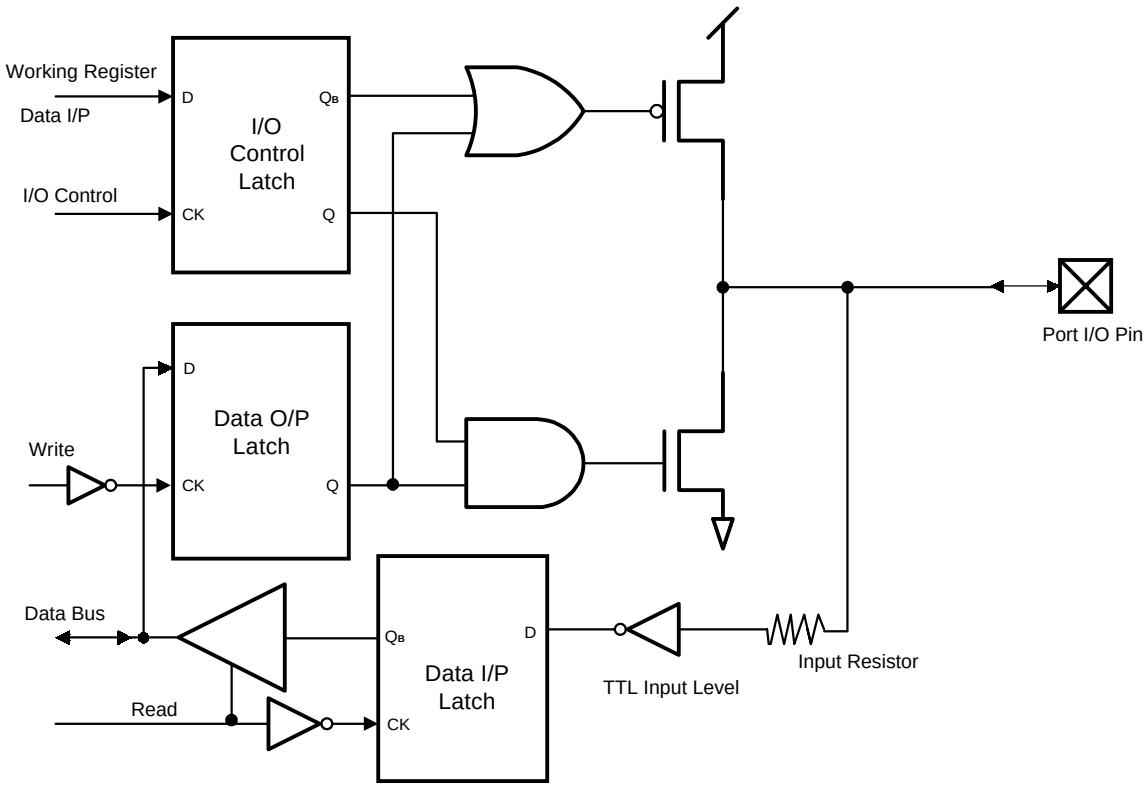
@ V_{dd}=5.0v ,Temperature＝25 ℃, the typical value as followings :

Voltage (V)	Basic WDT time-out cycle time (ms)
2.3	24.0
3.0	22.0
4.0	20.5
5.0	18.5
6.0	18.0

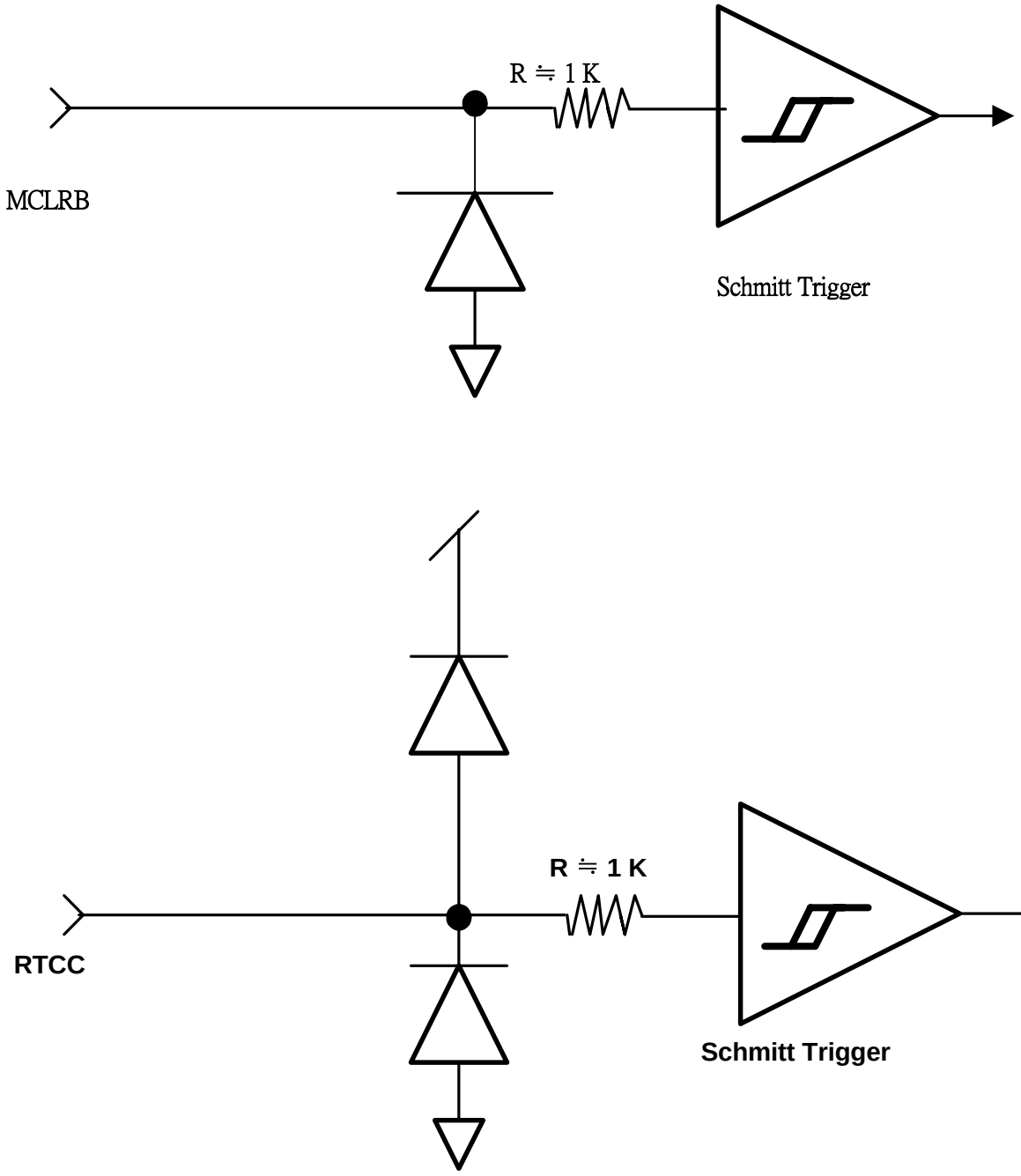
(I) MCLRB Filter：@ V_{dd}=5.0v

Wm ≥1.2us Wm : Filter pulse width (low) in /MCLR pin.

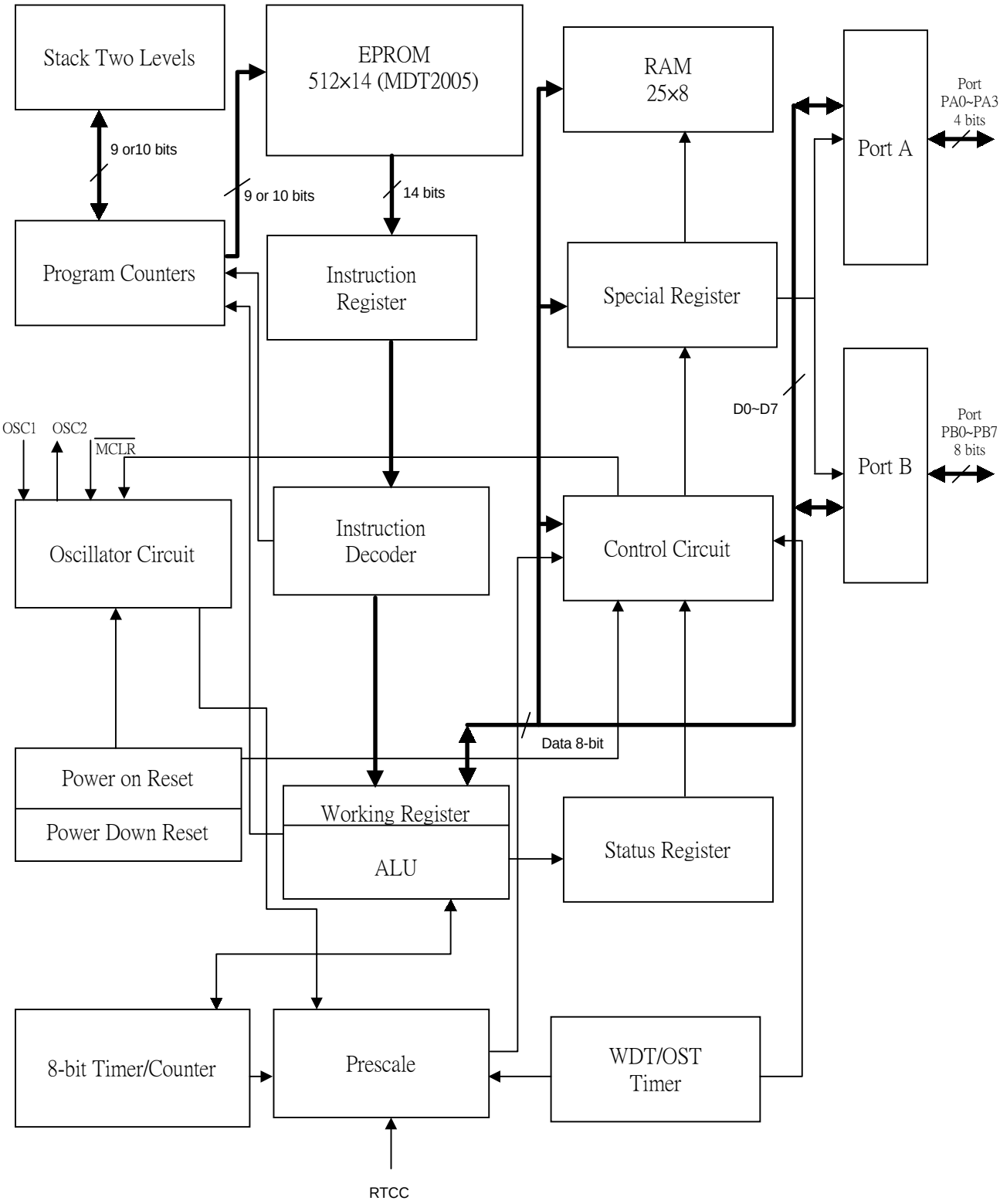
10. Port A and Port B Equivalent Circuit



11. MCLRB and RTCC Input Equivalent Circuit



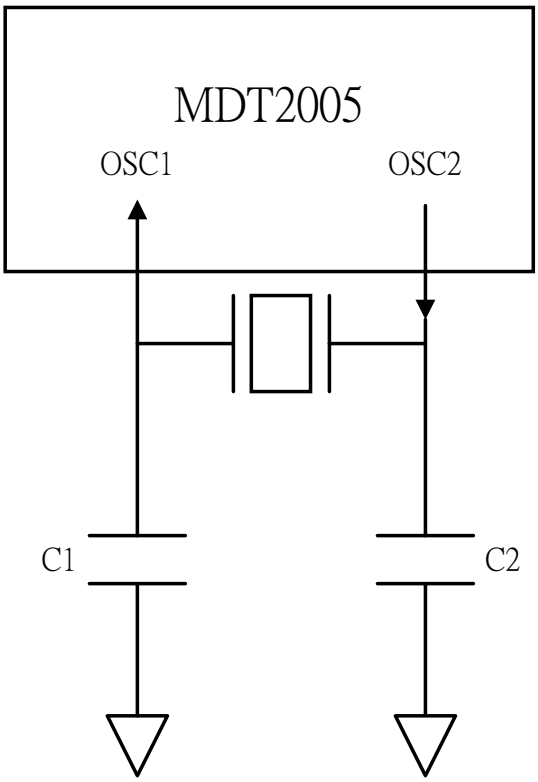
12. Block Diagram



13. External Capacitor Selection For Crystal Oscillator

@ V_{dd}＝3.0V~5.0 V

Osc. Type	Resonator Freq.	C1	C2
HF	20 MHz	0 pF ~10 pF	0 pF ~20 pF
	10 MHz	0 pF ~50 pF	0 pF ~100 pF
	4 MHz	0 pF ~30 pF	0 pF ~100 pF
XT	10 MHz	0 pF ~30 pF	0 pF ~50 pF
	4 MHz	0 pF ~50 pF	0 pF ~100 pF
	1 MHz	0 pF ~30 pF	0 pF ~50 pF
LF	1 MHz	5 pF ~10 pF	5 pF ~10 pF
	455 K	10 pF ~50 pF	10 pF ~50 pF
	32 K	10 pF ~30 pF	20 pF ~50 pF



To increase the stability of oscillator and the ability of anti-noise, the above values of the external capacitor range can be recommended for reference, but the higher capacitance also increases the start-up time.