# 12V, 1.5A Step-Down DC/DC Converter

## General Description

The AAT1162 is an 800kHz high efficiency step-down DC/DC converter. With a wide input voltage range of 4.0V to 13.2V, the AAT1162 is an ideal choice for dual-cell Lithium-ion battery-powered devices and mid-power-range regulated 12V-powered industrial applications. The internal power switches are capable of delivering up to 1.5A to the load.

The AAT1162 is a highly integrated device, simplifying system-level design. Minimum external components are required for the converter.

The AAT1162 optimizes efficiency throughout the entire load range. It operates in a combination PWM/Light Load mode for improved light-load efficiency. The high switching frequency allows the use of small external components. The low current shutdown feature disconnects the load from $V_{IN}$ and drops shutdown current to less than 1μA.

The AAT1162 is available in a Pb-free, space-saving, thermally-enhanced 16-pin TDFN34 packageand is rated over an operating temperature range of -40°C to +85°C.

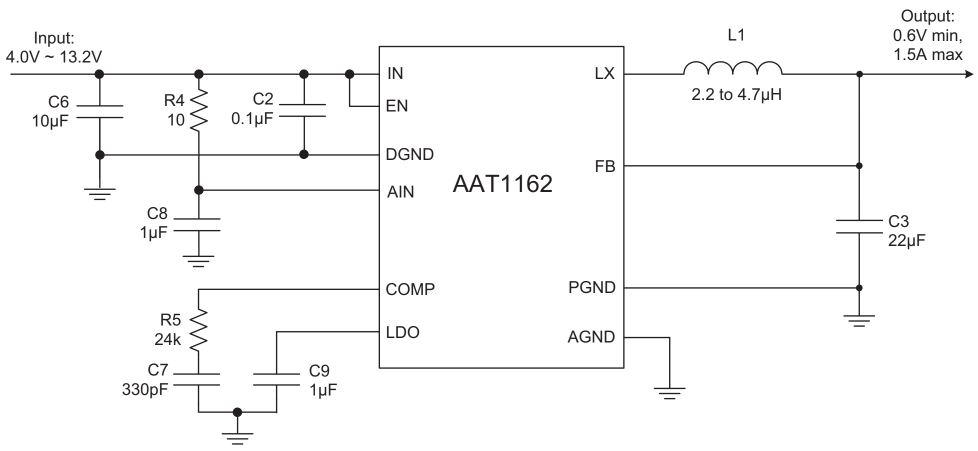
## Features

- Input Voltage Range: 4.0V to 13.2V
- Up to 1.5A Load Current
- Fixed or Adjustable Output:
  - Output Voltage: 0.6V to $V_{IN}$
- Low 115μA No-Load Operating Current
- Less than 1μA Shutdown Current
- Up to 96% Efficiency
- Integrated Power Switches
- 800kHz Switching Frequency
- Soft Start Function
- Short-Circuit and Over-Temperature Protection
- Minimum External Components
- TDFN34-16 Package
- Temperature Range: -40°C to +85°C

## Applications

- Distributed Power Systems
- Industrial Applications
- Laptop Computers
- Portable DVD Players
- Portable Media Players
- Set-Top Boxes
- TFT LCD Monitors and HDTVs

## Typical Application

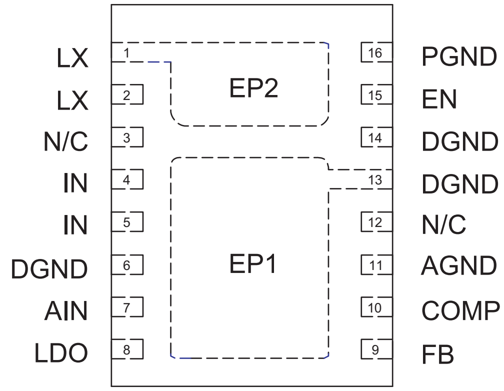


## Pin Descriptions

| Pin # | Symbol | Function |
|---|---|---|
| 1, 2, EP2 | LX | Power switching node. LX is the drain of the internal P-channel switch and N-channel synchronous rectifier. Connect the output inductor to the two LX pins and to EP2. A large exposed copper pad under the package should be used for EP2. |
| 3, 12 | N/C | Not connected. |
| 4, 5 | IN | Power source input. Connect IN to the input power source. Bypass IN to DGND with a 22µF or greater capacitor. Connect both IN pins together as close to the IC as possible. An additional 100nF ceramic capacitor should also be connected between the two IN pins and DGND, pin 6 |
| 6, 13, 14, EP1 | DGND | Exposed Pad 1 Digital Ground, DGND. The exposed thermal pad (EP1) should be connected to board ground plane and pins 6, 13, and 14. The ground plane should include a large exposed copper pad under the package for thermal dissipation (see package outline). |
| 7 | AIN | Internal analog bias input. AIN supplies internal power to the AAT1162. Connect AIN to the input source voltage and bypass to AGND with a 0.1µF or greater capacitor. For additional noise rejection, connect to the input power source through a 10Ω or lower value resistor. |
| 8 | LDO | Internal LDO bypass node. The output voltage of the internal LDO is bypassed at LDO. The internal circuitry of the AAT1162 is powered from LDO. Do not draw external power from LDO. Bypass LDO to AGND with a 1µF or greater capacitor. |
| 9 | FB | Output voltage feedback input. FB senses the output voltage for regulation control. For fixed output versions, connect FB to the output voltage. For adjustable versions, drive FB from the output voltage through a resistive voltage divider. The FB regulation threshold is 0.6V. |
| 10 | COMP | Control compensation node. Connect a series RC network from COMP to AGND, R = 51k and C = 150pF. |
| 11 | AGND | Analog signal ground. Connect AGND to PGND at a single point as close to the IC as possible. |
| 15 | EN | Active high enable input. Drive EN high to turn on the AAT1162; drive it low to turn it off. For automatic startup, connect EN to IN through a 4.7kΩ resistor. EN must be biased high, biased low, or driven to a logic level by an external source. Do not let the EN pin float when the device is powered. |
| 16 | PGND | Power ground. Connect AGND to PGND at a single point as close to the IC as possible. |

## Pin Configuration

**TDFN34-16**
**(Top View)**



## Absolute Maximum Ratings[1]

| Symbol | Description | Value | Units |
|---|---|---|---|
| $V_{IN}$, $V_{AIN}$ | Input Voltage | -0.3 to 14 | V |
| $V_{LX}$ | LX to GND Voltage | -0.3 to $V_{IN}$ + 0.3 | V |
| $V_{FB}$ | FB to GND Voltage | -0.3 to $V_{IN}$ + 0.3 | V |
| $V_{EN}$ | EN to GND Voltage | -0.3 to $V_{IN}$ + 0.3 | V |
| $T_J$ | Operating Junction Temperature Range | -40 to 150 | °C |

## Thermal Information[3]

| Symbol | Description | Value | Units |
|---|---|---|---|
| $P_D$ | Maximum Power Dissipation[4] | 2.7 | W |
| $\theta_{JA}$ | Thermal Resistance | 37 | °C/W |

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Based on long-term current density limitation.
3. Mounted on an FR4 board.
4. Derate 2.7mW/°C above 25°C.

## Electrical Characteristics[1]

4.0V < $V_{IN}$ < 13.2V. $C_{IN}$ = $C_{OUT}$ = 22µF; L = 2.2 or 3.8µH, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = 25°C.

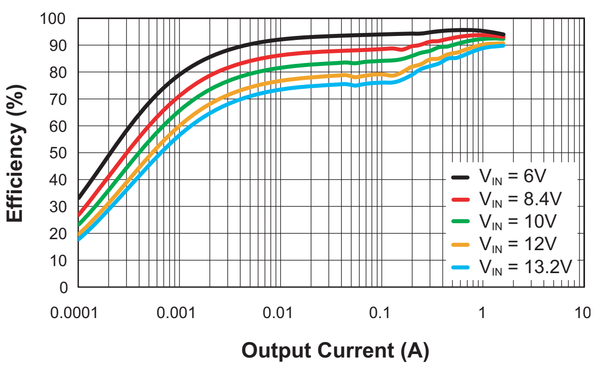
| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage Range | | 4.0 | | 13.2 | V |
| $V_{UVLO}$ | Input Under-Voltage Lockout | Rising | | | 4.0 | V |
| $V_{UVLO}$ | Input Under-Voltage Lockout | Hysteresis | | 0.3 | | V |
| $I_Q$ | Supply Current | No Load | | 150 | 300 | µA |
| $I_{SHDN}$ | Shutdown Current | $V_{EN}$ = GND | | | 1 | µA |
| $V_{OUT}$ | Output Voltage Range | | 0.6 | | 0.94 $V_{IN}$ | V |
| $V_{OUT}$ | Output Voltage Accuracy | $I_{OUT}$ = 0A to 1.5A | -2.5 | | 2.5 | % |
| $\Delta V_{OUT}/V_{OUT}/\Delta V_{IN}$ | Line Regulation | $V_{IN}$ = 4.5V to 13.2V | | 0.023 | 0.100 | %/V |
| $\Delta V_{OUT}/I_{OUT}$ | Load Regulation | $V_{IN}$ = 12V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0A to 1.5A | | 0.4 | | % |
| $V_{FB}$ | Feedback Reference Voltage (adjustable version) | No Load, $T_A$ = 25°C | 0.59 | 0.60 | 0.61 | V |
| $I_{FBLEAK}$ | FB Leakage Current | $V_{OUT}$ = 1.2V, Adjustable Version | | | 0.2 | µA |
| $I_{FBLEAK}$ | FB Leakage Current | $V_{OUT}$ = 1.2V, Fixed Version | | 2 | | µA |
| $F_{OSC}$ | PWM Oscillator Frequency | | 0.6 | 0.8 | 1 | MHz |
| | Foldback Frequency | | | 200 | | kHz |
| DC | Maximum Duty Cycle | | | | 94 | % |
| $T_{ON}$ | Minimum Turn-On Time | | | 100 | | ns |
| $T_S$ | Soft-Start Time | | | 200 | | ms |
| $R_{DS(ON)H}$ | P-Channel On Resistance | $V_{IN}$ = 12V | | 0.12 | | Ω |
| $R_{DS(ON)H}$ | P-Channel On Resistance | $V_{IN}$ = 6V | | 0.15 | | Ω |
| $R_{DS(ON)L}$ | N-Channel On Resistance | $V_{IN}$ = 12V | | 0.06 | | Ω |
| $R_{DS(ON)L}$ | N-Channel On Resistance | $V_{IN}$ = 6V | | 0.08 | | Ω |
| $\eta$ | Efficiency | $V_{IN}$ = 12V, $V_{OUT}$ = 5V, $I_{OUT}$ = 1.5A | | 90 | | % |
| $I_{LIM}$ | PMOS Current Limit | | 4.0 | 6.0 | | A |
| $I_{LXLEAK}$ | LX Leakage Current | $V_{IN}$ = 13.2V, $V_{LX}$ = 0 to $V_{IN}$ | | | 1 | µA |
| $T_{SD}$ | Over-Temperature Shutdown Threshold | | | 140 | | °C |
| $T_{HYS}$ | Over-Temperature Shutdown Hysteresis | | | 25 | | °C |
| $V_{IL}$ | EN Logic Low Input Threshold | | | | 0.4 | V |
| $V_{IH}$ | EN Logic High Input Threshold | | 1.4 | | | V |
| $I_{EN}$ | EN Input Current | $V_{EN}$ = 0V, $V_{EN}$ = 13.2V | -1.0 | | 1.0 | µA |

1. The AAT1162 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

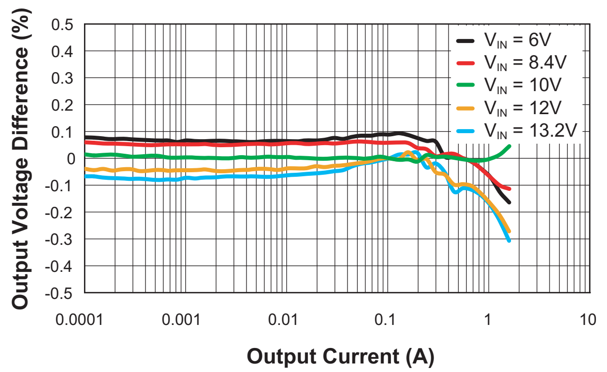
## Typical Characteristics

Test circuit of Figure 2, unless otherwise specified.

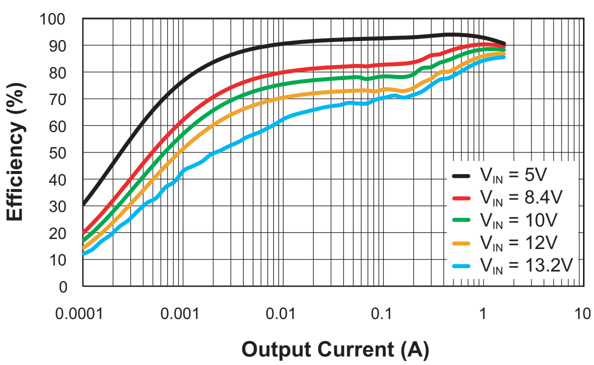
**Efficiency vs. Output Current**
**($V_{OUT}$ = 5V)**



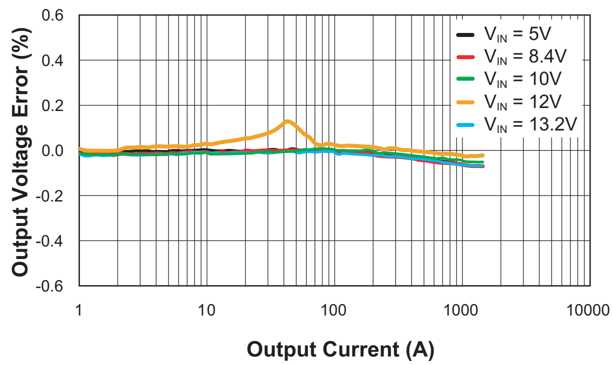

**Load Regulation**
**($V_{OUT}$ = 5V)**



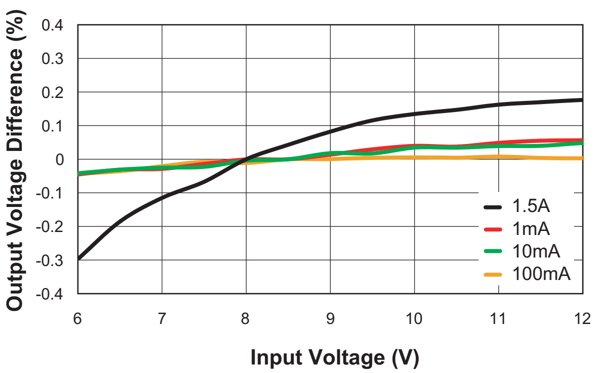

**Efficiency vs. Output Current**
**($V_{OUT}$ = 3.3V)**



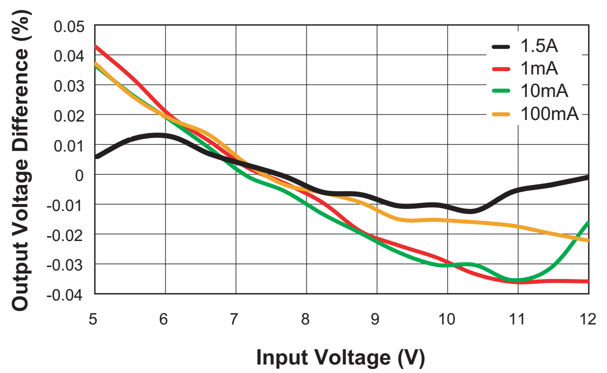

**Load Regulation**
**($V_{OUT}$ = 3.3V)**




**Line Regulation**
**($V_{OUT}$ = 5V)**



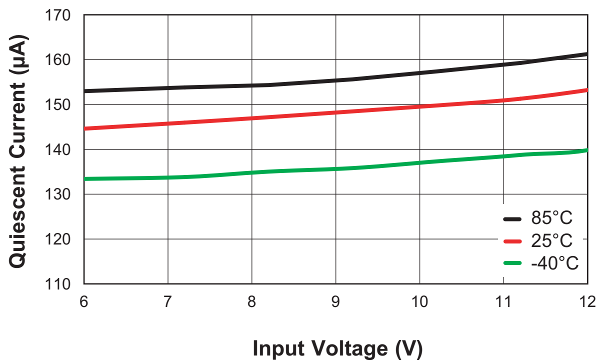

**Line Regulation**
**($V_{OUT}$ = 3.3V)**



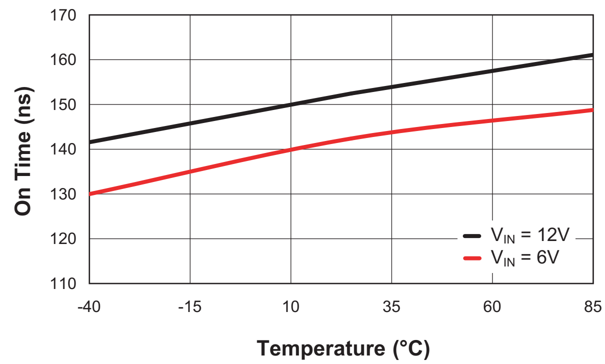
## Typical Characteristics

Test circuit of Figure 2, unless otherwise specified.

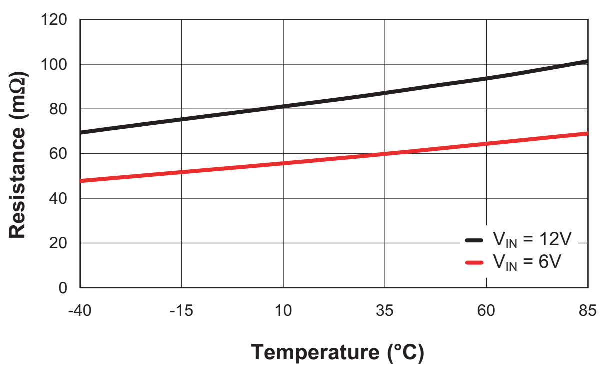
**Supply Current vs. Input Voltage**
**($V_{OUT}$ = 5V)**



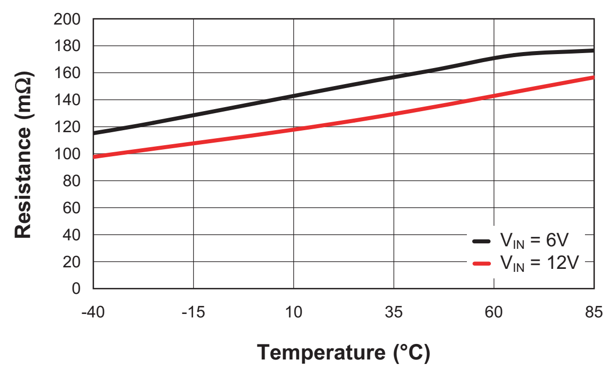

**Switching Current vs. Temperature**
**($V_{OUT}$ = 5V)**



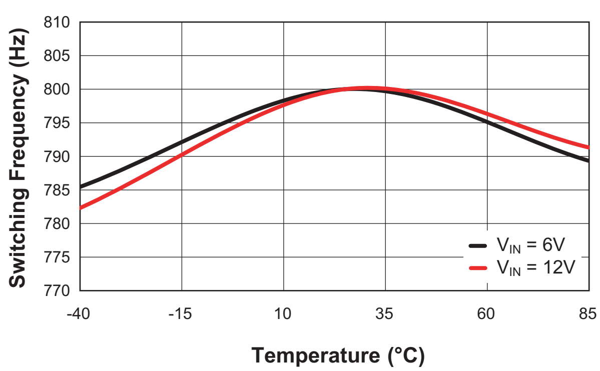

**N-Channel $R_{DS(ON)}$ vs. Temperature**



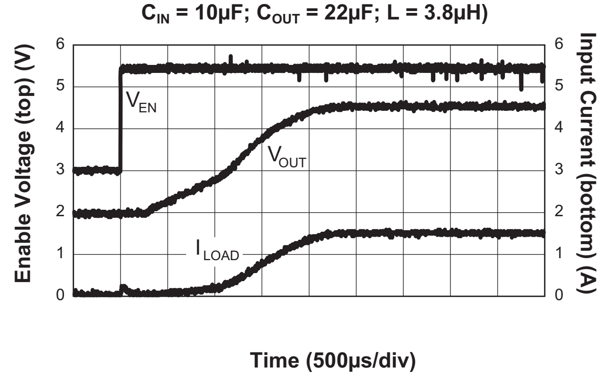

**P-Channel $R_{DS(ON)}$ vs. Temperature**
**($V_{IN}$ = 6V)**




**Switching Frequency vs. Temperature**



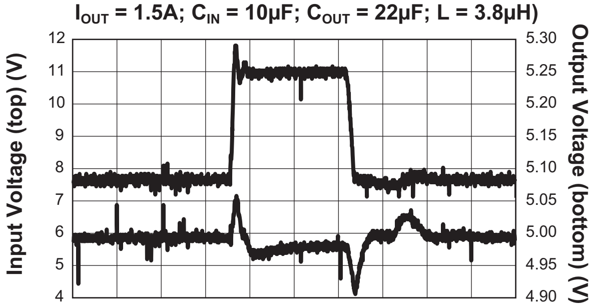

**Start-up Time**
**($V_{OUT}$ = 5.0V; $C_{FF}$ = 100pF; $R_{LOAD}$ = 1.5A;**
**$C_{IN}$ = 10µF; $C_{OUT}$ = 22µF; L = 3.8µH)**



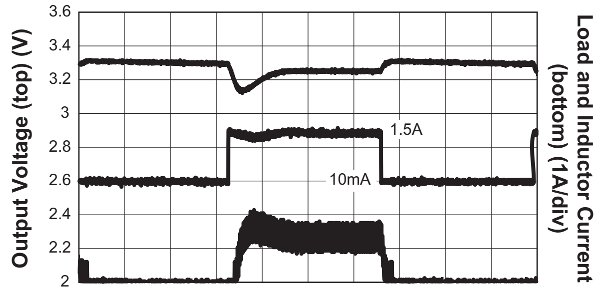
## Typical Characteristics

Test circuit of Figure 2, unless otherwise specified.

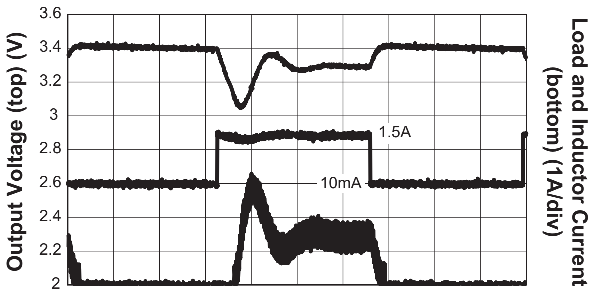
**Line Transient**
**($V_{OUT}$ = 5.0V; $C_{FF}$ = 100pF; $V_{IN}$ = 7.6V to 11V; $I_{OUT}$ = 1.5A; $C_{IN}$ = 10µF; $C_{OUT}$ = 22µF; L = 3.8µH)**



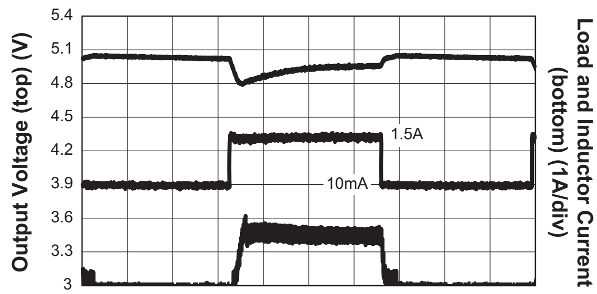

**Load Transient**
**($V_{OUT}$ = 3.3V; $C_{FF}$ = 100pF; $C_{OUT}$ = 66µF)**



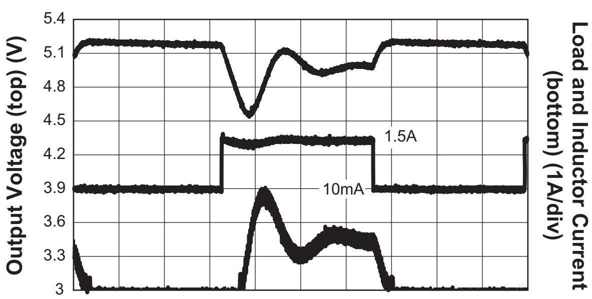

**Load Transient**
**($V_{OUT}$ = 3.3V; $C_{OUT}$ = 66µF; No $C_{FF}$)**



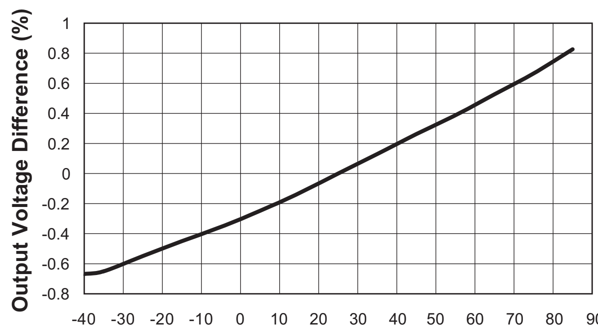

**Load Transient**
**($V_{OUT}$ = 5V; $C_{FF}$ = 100pF; $C_{OUT}$ = 66µF)**




**Load Transient**
**($V_{OUT}$ = 5V; $C_{OUT}$ = 66µF; No $C_{FF}$)**



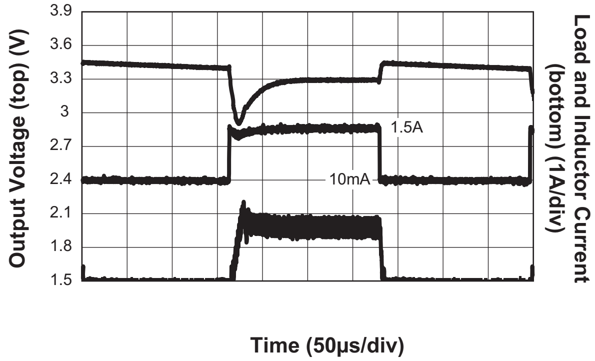

**$V_{OUT}$ vs. Temperature**
**($V_{OUT}$ = 3.3V; $I_{LOAD}$ = 1.5A)**



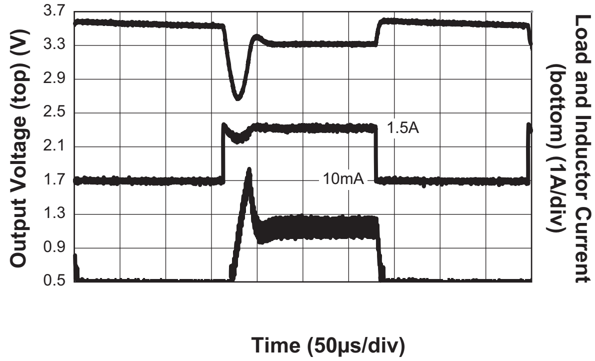
## Typical Characteristics

Test circuit of Figure 2, unless otherwise specified.

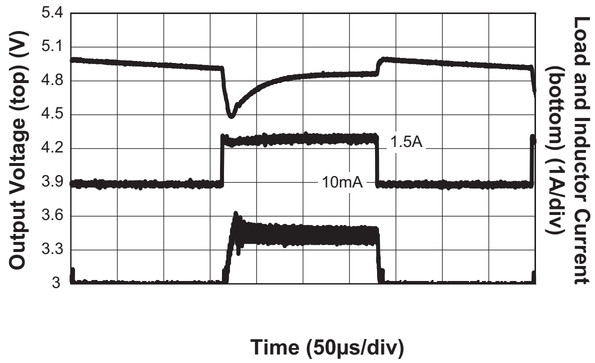
**Load Transient**
**($V_{OUT}$ = 3.3V; $C_{FF}$ = 100pF; $C_{OUT}$ = 22µF)**



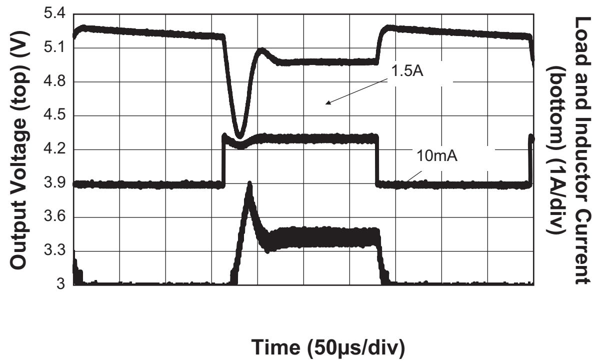

**Load Transient**
**($V_{OUT}$ = 3.3V; $C_{OUT}$ = 22µF; No $C_{FF}$)**



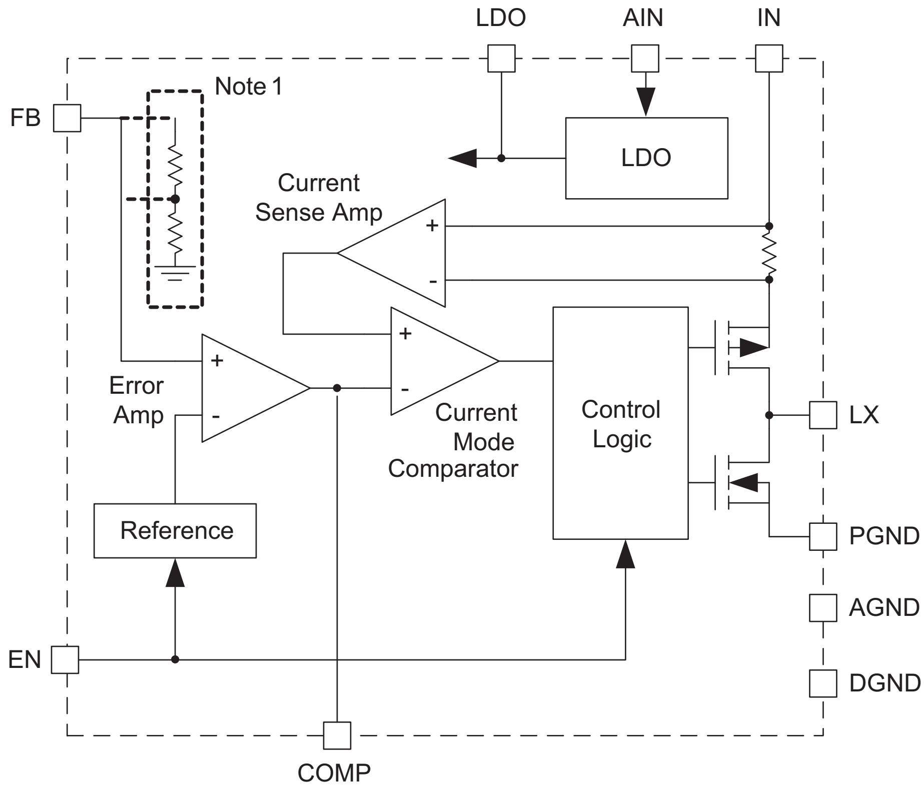

**Load Transient**
**($V_{OUT}$ = 5V; $C_{FF}$ = 100pF; $C_{OUT}$ = 22µF)**




**Load Transient**
**($V_{OUT}$ = 5V; $C_{OUT}$ = 22µF; No $C_{FF}$)**



## Functional Block Diagram




Note 1: For fixed output voltage versions, FB is connected to the error amplifier through the resistive voltage divider shown.

## Functional Description

The AAT1162 is a current-mode step-down DC/DC converter that operates over a wide 4V to 13.2V input voltage range and is capable of supplying up to 1.5A to the load with the output voltage regulated as low as 0.6V. Both the P-channel power switch and N-channel synchronous rectifier are internal, reducing the number of external components required. The output voltage is adjusted by an external resistor divider; fixed output voltage versions are available upon request. The regulation system is externally compensated, allowing the circuit to be optimized for each application. The AAT1162 includes cycle-by-cycle current limiting, frequency foldback for improved short-circuit performance, and thermal overload protection to prevent damage in the event of an external fault condition.

### Control Loop

The AAT1162 regulates the output voltage using constant frequency current mode control. The AAT1162 monitors current through the high-side P-channel MOSFET and uses that signal to regulate the output voltage. This provides improved transient response and eases compensation. Internal slope compensation is included to ensure the current "inside loop" stability.

High efficiency is maintained under light load conditions by automatically switching to variable frequency Light Load control. In this condition, transition losses are reduced by operating at a lower frequency at light loads.

## Short-Circuit Protection

The AAT1162 uses a cycle-by-cycle current limit to protect itself and the load from an external fault condition. When the inductor current reaches the internally set 3.0A current limit, the P-channel MOSFET switch turns off and the N-channel synchronous rectifier is turned on, limiting the inductor and the load current.

During an overload condition, when the output voltage drops below 50% of the regulation voltage (0.3V at FB), the AAT1162 switching frequency drops by a factor of 4. This gives the inductor current ample time to reset during the off time to prevent the inductor current from rising uncontrolled in a short-circuit condition.

## Thermal Protection

The AAT1162 includes thermal protection that disables the regulator when the die temperature reaches 140ºC. It automatically restarts when the temperature decreases by 25ºC or more.

# Applications Information

## Setting the Output Voltage

Figure 1 shows the basic application circuit for the AAT1162 and output setting resistors. Resistors R1 and R2 program the output to regulate at a voltage higher than 0.6V. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2 is 5.9kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 1 summarizes the resistor values for various output voltages with R2 set to either 5.9kΩ for good noise immunity or 59kΩ for reduced no load input current.

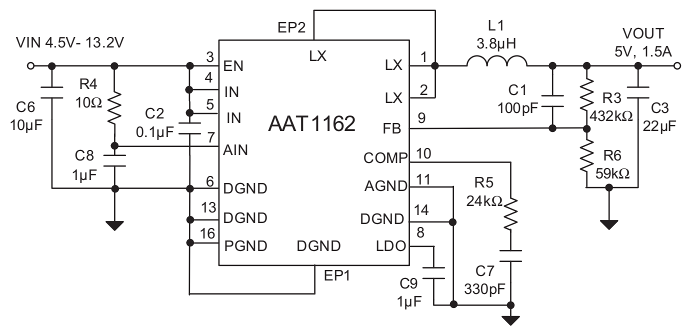



**Figure 1: Typical Application Circuit.**

The adjustable feedback resistors, combined with an external feed forward capacitor (C1 in Figure 1), deliver enhanced transient response for extreme pulsed load applications. The addition of the feed forward capacitor typically requires a larger output capacitor C3 for stability. Larger C1 values reduce overshoot and undershoot during startup and load changes. However, do not exceed 470pF to maintain stable operation.

The external resistors set the output voltage according to the following equation:

$$V_{OUT} = 0.6V\left(1 + \frac{R1}{R2}\right)$$

or

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R2$$

Table 1 shows the resistor selection for different output voltage settings.

| $V_{OUT}$ (V) | R2 = 5.9(kΩ) R1 (kΩ) | R2 = 59(kΩ) R1 (kΩ) |
|---|---|---|
| 0.8 | 1.96 | 19.6 |
| 0.9 | 2.94 | 29.4 |
| 1.0 | 3.92 | 39.2 |
| 1.1 | 4.99 | 49.9 |
| 1.2 | 5.90 | 59.0 |
| 1.3 | 6.81 | 68.1 |
| 1.4 | 7.87 | 78.7 |
| 1.5 | 8.87 | 88.7 |
| 1.8 | 11.8 | 118 |
| 1.85 | 12.4 | 124 |
| 2.0 | 13.7 | 137 |
| 2.5 | 18.7 | 187 |
| 3.3 | 26.7 | 267 |
| 5.0 | 43.2 | 432 |

**Table 1: Resistor Selection for Different Output Voltage Settings. Standard 1% Resistors are Substituted for Calculated Values.**

## Inductor Selection

For most designs, the AAT1162 operates with inductors of 2μH to 4.7μH. Low inductance values are physically smaller, but require faster switching, which results in some efficiency loss. The inductor value can be derived from the following equation:

$$L1 = \frac{V_{OUT}}{3.3} \cdot 3.8\mu H$$

Where $\Delta I_L$ is inductor ripple current. Large value inductors lower ripple current and small value inductors result in high ripple currents. Choose inductor ripple current approximately 32% of the maximum load current 1.5A, or $\Delta I_L$ = 480mA. For output voltages above 3.3V, the minimum recommended inductor is 3.8μH. For 3.3V and below, use a 2 to 3.8μH inductor. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 15mΩ to 20mΩ range. For higher efficiency at heavy loads (above 1A), or minimal load regulation (but some transient overshoot), the resistance should be kept below 18mΩ. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation (1.5A + 280mA). Table 2 lists some typical surface mount inductors that meet target applications for the AAT1162.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor. For example, the 4.7μH WE-TPC series inductor selected from Wurth has an 38mΩ DCR and a 2.4ADC current rating. At full load, the inductor DC loss is 85mW which gives only a 1.1% loss in efficiency for a 1.5A, 5V output.

## Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than the input source impedance to prevent high frequency switching current passing to the input. A low ESR input capacitor sized for maximum RMS current must be used. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 10μF ceramic capacitor is sufficient for most applications.

| Manufacturer | Part Number | L (µH) | Max DCR (mΩ) | Rated DC Current (A) | Size WxLxH (mm) |
|---|---|---|---|---|---|
| Sumida | CDRH103RNP-2R2N | 2.2 | 16.9 | 5.10 | 10.3x10.5x3.1 |
| Sumida | CDR7D43MNNP-3R7NC | 3.7 | 18.9 | 4.3 | 7.6x7.6x4.5 |
| Coilcraft | MSS1038-382NL | 3.8 | 13 | 4.25 | 10.2x7.7x3.8 |
| Cooper Bussman | DR73-4R7-R | 4.7 | 29.7 | 3.09 | 6.0x7.6x3.55 |
| Wurth | 7440530047 | 4.7 | 38 | 2.40 | 5.8x5.8x2.8 |

**Table 2: Typical Surface Mount Inductors.**

To estimate the required input capacitor size, determine the acceptable input ripple level ($V_{PP}$) and solve for C. The calculated value varies with input voltage and is a maximum when $V_{IN}$ is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_{OSC}}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_{OSC}}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 16V, X5R ceramic capacitor with 12V DC applied is actually about 8.5µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current:

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is at maximum when $V_O$ is twice $V_{IN}$. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle. The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT1162. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple. The proper placement of the input capacitor (C6) can be seen in the evaluation board layout in Figure 3. Additional noise filtering for proper operation is accomplished by adding a small 0.1µF capacitor on the IN pins (C2).

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result. Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem. In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR, ESL bypass ceramic. This dampens the high Q network and stabilizes the system.

## Output Capacitor Selection

The output capacitor is required to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and high ripple current. The output ripple $V_{OUT}$ is determined by:

$$\Delta V_{OUT} \le \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot F_{OSC} \cdot L} \cdot \left(ESR + \frac{1}{8 \cdot F_{OSC} \cdot C_{OUT}}\right)$$

The output capacitor limits the output ripple and provides holdup during large load transitions. A 10µF to 47µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple. The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_{OSC}}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients. The internal voltage loop compensation also limits the minimum output capacitor value to 22µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

The maximum output capacitor RMS ripple current is given by:

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_{OSC} \cdot V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot-spot temperature.

## Compensation

The AAT1162 step-down converter uses peak current mode control with slope compensation scheme to maintain stability with lower value inductors for duty cycles greater than 50%. The regulation feedback loop in the IC is stabilized by the components connected to the COMP pin, as shown in Figure 1.

To optimize the compensation components, the following equations can be used. The compensation resistor $R_{COMP}$ (R5) is calculated using the following equation:

$$R_{COMP}\ (R5) = \frac{2\pi V_{OUT} \cdot C_{OUT} \cdot F_{OSC}}{10 G_{EA} \cdot G_{COMP} \cdot V_{FB}}$$

Where $V_{FB}$ = 0.6V, $G_{COMP}$ = 40.1734 and $G_{EA} = 9.091 \cdot 10^{-5}$.

$F_{OSC}$ is the switching frequency and $C_{OUT}$ is based on the output capacitor calculation. The $C_{COMP}$ value can be determined from the following equation:

$$C_{COMP}\ (C7) = \frac{4}{2\pi R_{COMP}\ (R5) \cdot \left(\frac{F_{OSC}}{10}\right)}$$

The feed forward capacitor CFF (C1) provides faster transient response for pulsed load applications. The addition of the feed forward capacitor typically requires a larger output capacitor C1 for stability. Larger C1 values reduce overshoot and undershoot during startup and line/load changes. The CFF value can be from 100pF to 470pF, but do not exceed 470pF to maintain stable operation.

## Layout Guidance

Figure 2 is the schematic for the evaluation board. When laying out the PC board, the following layout guideline should be followed to ensure proper operation of the AAT1162:

1. Exposed pad EP1 must be reliably soldered to PGND/DGND/AGND. The exposed thermal pad should be connected to board ground plane and pins 6, 11, 13, 14 and 16. The ground plane should include a large exposed copper pad under the package for thermal dissipation.
2. The power traces, including GND traces, the LX traces and the VIN trace should be kept short, direct and wide to allow large current flow. The L1 connection to the LX pins should be as short as possible. Use several via pads when routing between layers.
3. Exposed pad pin EP2 must be reliably soldered to the LX pins 1 and 2. The exposed thermal pad should be connected to the board LX connection and the inductor L1 and also pins 1 and 2. The LX plane should include a large exposed copper pad under the package for thermal dissipation.
4. The input capacitors (C9 and C1) should be connected as close as possible to IN (Pins 4 and 5) and DGND (Pin 6) to get good power filtering.
5. Keep the switching node LX away from the sensitive FB node.
6. The feedback trace for the FB pin should be separate from any power trace and connected as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. The feedback resistors should be placed as close as possible to the FB pin (Pin 9) to minimize the length of the high impedance feedback trace.
7. The output capacitors C3, 4, and 5 and L1 should be connected as close as possible and there should not be any signal lines under the inductor.
8. The resistance of the trace from the load return to the PGND (Pin 16) should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.

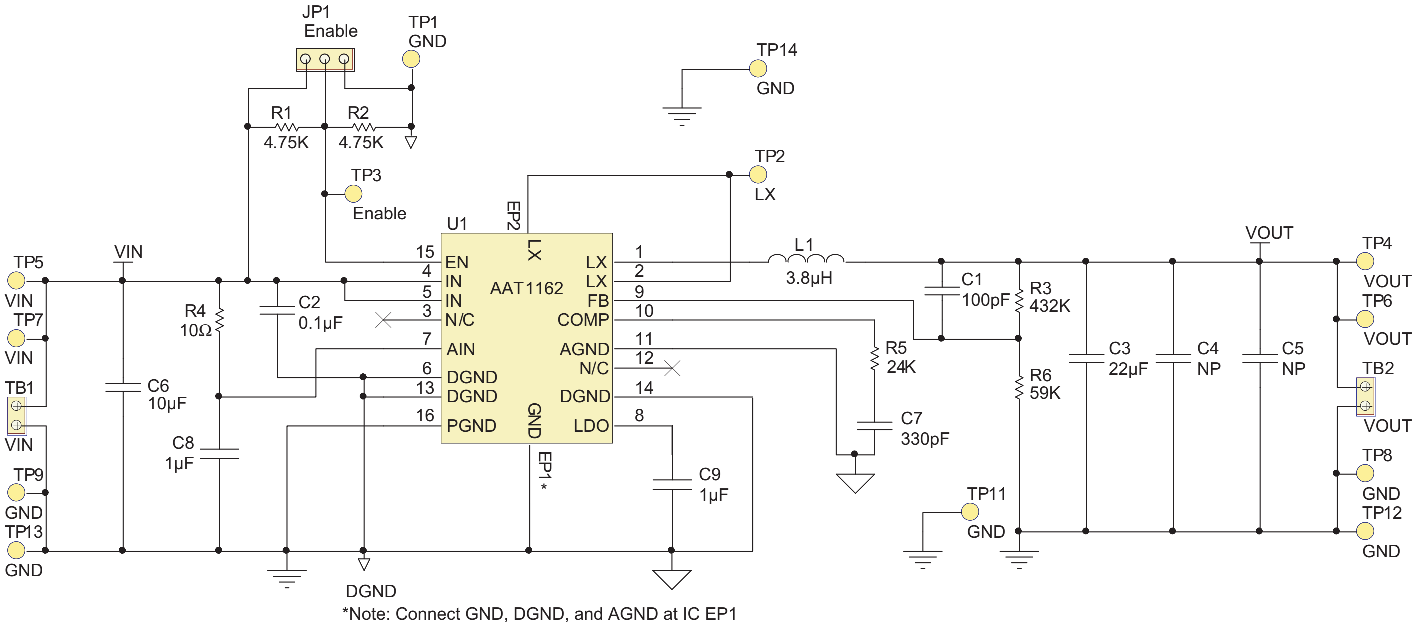



**Figure 2: AAT1162 Evaluation Board Schematic.**

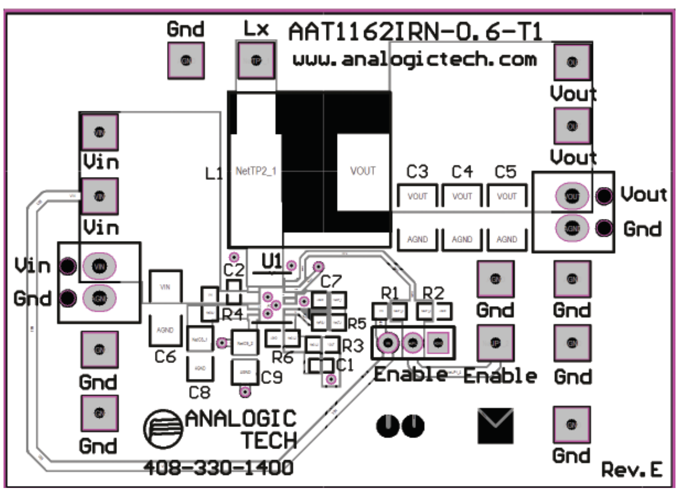



**Figure 3: AAT1162 Evaluation Board Component Side Layout.**

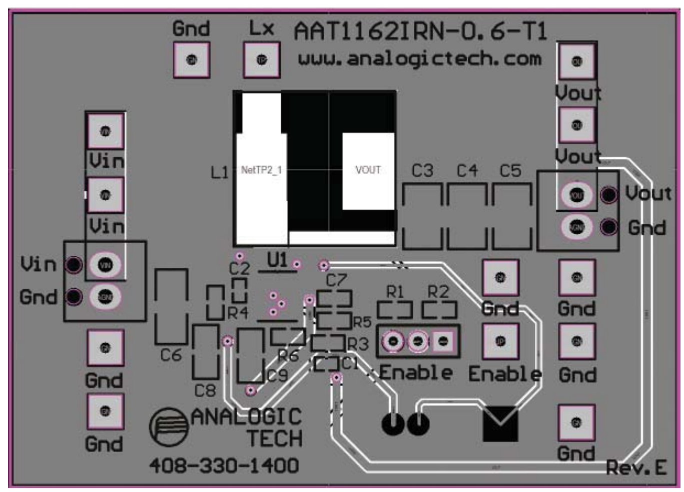



**Figure 4: AAT1162 Evaluation Board Solder Side Layout.**

# Design Example

## Specifications

| | |
|---|---|
| $V_{OUT}$ | 5V @ 1.5A, Pulsed Load $\Delta I_{LOAD}$ = 1.5A |
| $V_{IN}$ | 12V nominal |
| $F_{OSC}$ | 800kHz |
| $T_{AMB}$ | 85°C in TDFN34-16 Package |

## Output Inductor

$$L = \frac{V_{OUT}}{3.3} \cdot 3.8\mu H = 5.75\mu H\text{; use } 4.7\mu H \text{ (see Table 2)}$$

$$\Delta I_L = 0.32 \cdot I_{LOAD} = 480mA$$

For Cooper Bussman inductor DR73-4R7-R 4.7μH DCR = 29.7mW max.

$$\Delta I_1 = \frac{V_{OUT}}{L1 \cdot F_{OSC}} \cdot \left(1 - \frac{V_{O1}}{V_{IN}}\right) = \frac{5V}{4.7\mu H \cdot 800kHz} \cdot \left(1 - \frac{5V}{12V}\right) = 480mA$$

$$I_{PK1} = I_{LOAD} + \frac{\Delta I_1}{2} = 1.5A + 0.480A = 1.98A$$

$$P_{L1} = I_{LOAD}{}^2 \cdot DCR = 3A^2 \cdot 13m\Omega = 117mW$$

## Output Capacitor

$V_{DROOP}$ = 0.2V

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_{OSC}} = \frac{3 \cdot 1.5A}{0.2V \cdot 800kHz} = 28\mu F\text{; use } 22\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_{OUT}) \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_{OSC} \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{5V \cdot (12V - 5V)}{4.7\mu H \cdot 800kHz \cdot 12V} = 139mArms$$

$$P_{esr} = esr \cdot I_{RMS}{}^2 = 5m\Omega \cdot (277mA)^2 = 384\mu W$$

## Input Capacitor

Input Ripple $V_{PP}$ = 50mV

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_{LOAD}} - ESR\right) \cdot 4 \cdot F_{OSC}} = \frac{1}{\left(\frac{50mV}{1.5A} - 5m\Omega\right) \cdot 4 \cdot 800kHz} = 11\mu F\text{; use } 10\mu F$$

$$I_{RMS(MAX)} = \frac{I_{LOAD}}{2} = 0.75Arms$$

$$P = esr \cdot I_{RMS}{}^2 = 5m\Omega \cdot (0.75A)^2 = 2.81mW$$

## AAT1162 Losses

Total losses can be estimated by calculating the dropout ($V_{IN} = V_O$) losses where the power MOSFET $R_{DS(ON)}$ will be at the maximum value. All values assume an 85°C ambient temperature and a 140°C junction temperature with the TDFN 37°C/W package.

$$P_{LOSS} = I_{LOAD}{}^2 \cdot R_{DS(ON)H} = 1.5A^2 \cdot 0.158\Omega = 0.355W$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (37°C/W) \cdot 355mW = 96.6°C$$

The total losses are also investigated at the nominal input voltage (12V). The simplified version of the $R_{DS(ON)}$ losses assumes that the N-channel and P-channel $R_{DS(ON)}$ are equal.

$$P_{TOTAL} = I_{LOAD}{}^2 \cdot R_{DS(ON)} + [(t_{sw} \cdot F_{OSC} \cdot I_{LOAD} + I_Q) \cdot V_{IN}]$$

$$= 1.5A^2 \cdot 100m\Omega + [(5ns \cdot 800kHz \cdot 1.5A + 150\mu A) \cdot 12V] = 299mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (37°C/W) \cdot 299mW = 96°C$$

## Ordering Information

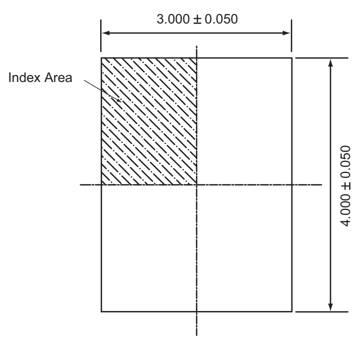
| Package | Marking[1] | Part Number (Tape and Reel)[2] |
|---|---|---|
| TDFN34-16 | YYXYY | **AAT1162IRN-0.6-T1** |

Pb-free

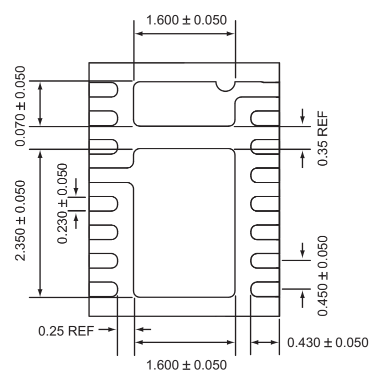
**All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/about/quality.aspx.**

## Package Information

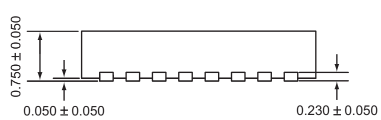
**TDFN34-16**




Top View




Bottom View




Side View

All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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