POLA Point-of-Load Alliance

6-A, 3.3-V Input Non-Isolated
Wide-Output Adjust Power Module

REVISION 00 (01DEC2003)

ADVANCE INFORMATION

NOMINAL SIZE = 0.87 in x 0.5 in (22,1 mm x 12,57 mm)

Features

- Up to 6-A Output Current
- 3.3-V Input Voltage
- Wide-Output Voltage Adjust (0.8 V to 2.5 V)
- Efficiencies up to 94 %
- 103 W/in³ Power Density
- On/Off Inhibit
- Pre-Bias Startup
- Under-Voltage Lockout
- Operating Temp: –40 to +85 °C
- Auto-Track™ Sequencing
- Output Over-Current Protection (Non-Latching, Auto-Reset)
- IPC Lead Free 2
- Safety Agency Approvals (Pending) UL 1950, CSA 22.2 950, & EN60950
- Point-of-Load Alliance (POLA) Compatible

Description

The ATH06T033 series is one of the smallest non-isolated power modules that features Auto-Track™. Auto-Track™ simplifies supply voltage sequencing in power systems by enabling modules to track each other, or any other external voltage, during power up and power down.

Although small in size (0.87 in × 0.5 in), these modules are rated for up to 6 A of output current, and are an ideal choice in applications where space, performance, and a power-up sequencing capability are important attributes.

The product provides high-performance step-down conversion from a 3.3-V input bus voltage. The output voltage of the ATH06T033 can be set to any voltage over the range, 0.8 V to 2.5 V, using a single resistor.

Other operating features include an on/off inhibit, output voltage adjust (trim), and output over-current protection. For high efficiency these parts employ a synchronous rectifier output stage, but a pre-bias hold-off capability ensures that the output will not sink current during startup.

Target applications include telecom, industrial, and general purpose circuits, including low-power dual-voltage systems that use a DSP, microprocessor, ASIC, or FPGA.

Package options include both through-hole and surface mount configurations.

Pin Configuration

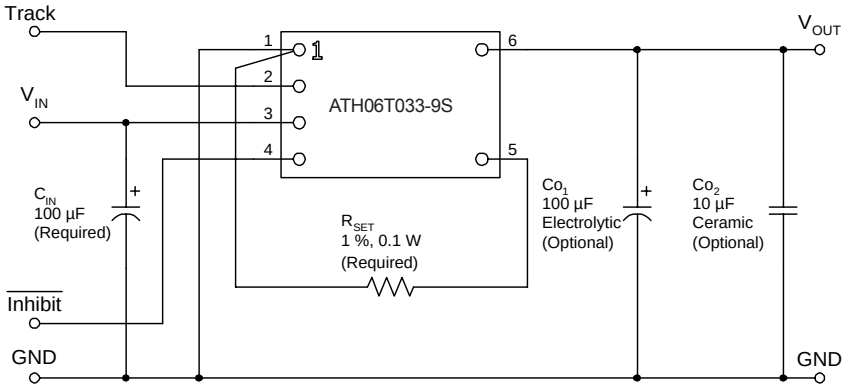
Pin	Function
1	GND
2	Track
3	V_{in}
4	Inhibit *
5	V_o Adjust
6	V_{out}

* *Denotes negative logic:*
Open = Normal operation
Ground = Function active

Auto-Track™ Sequencing

Standard Application

R_{set} = Required to set the output voltage to a value higher than 0.8 V. (See spec. table for values)
C_{in} = Required 100 µF
Co_1 = Optional 100 µF capacitor
Co_2 = Optional 10 µF ceramic capacitor for reduced output ripple.



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Ordering Information

Input Voltage	Output Voltage	Output Current	Model Number
2.95V to 3.65V	**0.8[1] to 2.5V**	**6A**	**ATH06T033-9(S)(J)**

Options:

"-J" - Through-hole Termination, Tray Packaging
"-SJ" - SMT Termination, Tray Packaging
"-S" - SMT Termination, T&R Packaging

Notes:
[1]Preset output voltage is 0.8V; externally adjustable to 2.5V through the Vo,Adjust pin

Pin Descriptions

Vin: The positive input voltage power node to the module, which is referenced to common *GND*.

Vout: The regulated positive power output with respect to the *GND* node.

GND: This is the common ground connection for the *Vin* and *Vout* power connections. It is also the 0 VDC reference for the control inputs.

Vo Adjust: A 0.1 W 1 % resistor must be directly connected between this pin and *GND* to set the output voltage to a value higher than 0.8 V. The temperature stability of the resistor should be 100 ppm/°C (or better). The set-point range for the output voltage is from 0.8 V to 2.5 V. The resistor value required for a given output voltage may be calculated from the following formula. If this pin is left open circuit, the output voltage will default to its lowest value. For further information on output voltage adjustment consult the related application note.

$$R_{set} = 10\ k\Omega \cdot \frac{0.8\ V}{V_{out} - 0.8\ V} - 2.49\ k\Omega$$

The specification table gives the preferred resistor values for a number of standard output voltages.

Inhibit: The Inhibit pin is an open-collector/drain negative logic input that is referenced to *GND*. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the *Inhibit* control is active, the input current drawn by the regulator is significantly reduced. If the *Inhibit* pin is left open-circuit, the module will produce an output whenever a valid input source is applied.

Track: This is an analog control input that allows the output voltage to follow another voltage during power-up and power-down sequences. The pin is active from 0 V up to the nominal set-point voltage. Within this range the module's output will follow the voltage at the *Track* pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its nominal output voltage. If unused, this input may be left unconnected. For further information consult the related application note.

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Environmental & Absolute Maximum Ratings (Voltages are with respect to GND)

Characteristics	Symbols	Conditions	Min	Typ	Max	Units
Track Input Voltage	V_{track}		–0.3	—	V_{in} + 0.3	V
Operating Temperature Range	T_a	Over V_{in} Range	–40 (i)	—	85	°C
Solder Reflow Temperature	T_{reflow}	Surface temperature of module body or pins			235 (ii)	°C
Storage Temperature	T_s	—	–40	—	125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted	—	TBD	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 Suffix H 20-2000 Hz Suffix S	— —	TBD TBD	— —	G's
Weight	—		—	2.9	—	grams
Flammability	—	Meets UL 94V-O				

Notes: *(i) For operation below 0 °C the external capacitors m ust have stable characteristics. use either a low ESR tantalum, Os-Con®, or ceramic capacitor.*
(ii) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

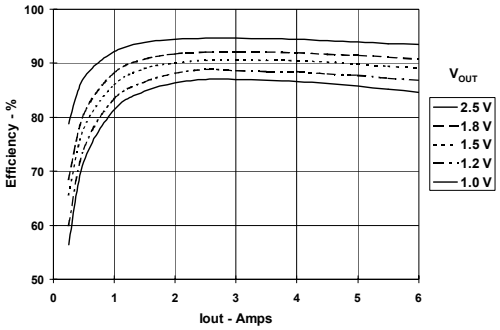
Specifications (Unless otherwise stated, T_a =25 °C, V_{in} =3.3 V, V_o =2.5 V, Co_{in} =100 µF, Co_1 =0 µF, Co_2 =0 µF, and I_o =$I_o$max)

			ATH06T033			
Characteristics	Symbols	Conditions	Min	Typ	Max	Units
Output Current	I_o	0.8 V ≤ V_o ≤ 2.5 V, 85 °C, natural convection	0	—	6 (1)	A
Input Voltage Range	V_{in}	Over I_o range	2.95	—	3.65	V
Set-Point Voltage Tolerance	V_o tol		—	—	±2 (2)	%V_o
Temperature Variation	ΔReg_{temp}	–40 °C <T_a < +85 °C	—	±0.5	—	%V_o
Line Regulation	ΔReg_{line}	Over V_{in} range	—	±10	—	mV
Load Regulation	ΔReg_{load}	Over I_o range	—	±12	—	mV
Total Output Variation	ΔReg_{tot}	Includes set-point, line, load, –40 °C ≤ T_a ≤ +85 °C	—	—	±3 (2)	%V_o
Efficiency	η	I_o =4 A R_{SET} = 2.21 kΩ V_o = 2.5 V R_{SET} = 4.12 kΩ V_o = 2.0 V R_{SET} = 5.49 kΩ V_o = 1.8 V R_{SET} = 8.87 kΩ V_o = 1.5 V R_{SET} = 17.4 kΩ V_o = 1.2 V R_{SET} = 36.5 kΩ V_o = 1.0 V	— — — — — —	94 92 91 90 88 87	— — — — — —	%
V_o Ripple (pk-pk)	V_r	20 MHz bandwidth, Co_2 =10 µF ceramic	—	20 (3)	—	mVpp
Over-Current Threshold	I_o trip	Reset, followed by auto-recovery	—	12	—	A
Transient Response		1 A/µs load step, 50 to 100 % $I_o$max, Co_1 =100 µF				
	t_{tr}	Recovery Time	—	70	—	µSec
	ΔV_{tr}	V_o over/undershoot	—	100	—	mV
Track Input Current (pin 2)	I_{IL} track	Pin to GND	—	—	–130 (4)	µA
Track Slew Rate Capability	dV_{track}/dt	$\lvert V_{track} - V_o \rvert$ ≤ 50 mV and V_{track} < V_o(nom)	5	—	—	V/ms
Under-Voltage Lockout	UVLO	V_{in} increasing V_{in} decreasing	— 3.4	4.3 3.7	4.45 —	V
Inhibit Control (pin4)		Referenced to GND				
Input High Voltage	V_{IH}		V_{in} –0.5	—	Open (4)	V
Input Low Voltage	V_{IL}		–0.2	—	0.6	
Input Low Current	I_{IL} inhibit	Pin to GND	—	–130	—	µA
Input Standby Current	I_{in} inh	Inhibit (pin 4) to GND, Track (pin 2) open	—	10	—	mA
Switching Frequency	f_s	Over V_{in} and I_o ranges	550	600	650	kHz
External Input Capacitance	C_{in}		100 (5)	—	—	µF
External Output Capacitance	C_{out}		0	100 (6)	TBD	µF
Reliability	MTBF	Per Bellcore TR-332 50 % stress, T_a =40 °C, ground benign	TBD	—	—	10^6 Hrs

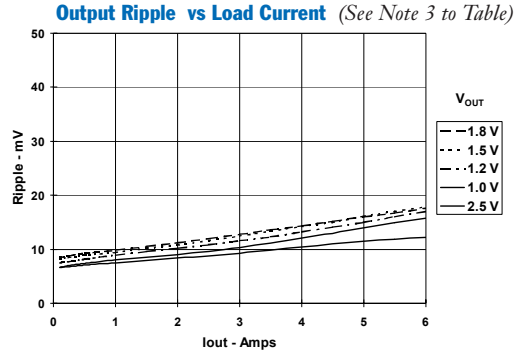
Notes: *(1) No derating is required when the module is soldered directly to a 4-layer PCB with 1 oz. copper.*
(2) The set-point voltage tolerance is affected by the tolerance and stability ofR_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1 % with 100 ppm/°C or better temperature stability.
(3) The pk-pk output ripple voltage is measured with an external 10 µF ceramic capacitor. See the standard application schematic.
(4) This control pin has an internal pull-up to the input voltage Vin. If it is left open-circuit the module will operate when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult the related application note.
(5) A 100 µF input capacitor is required for proper operation. The capacitor must be rated for a minimum of 300 mA rms of ripple current.
(6) An external output capacitor is not required for basic operation. Adding 100 µF of distributed capacitance at the load will improve the transient response.

Characteristic Data; V_{in} =3.3 V *(See Note A)*

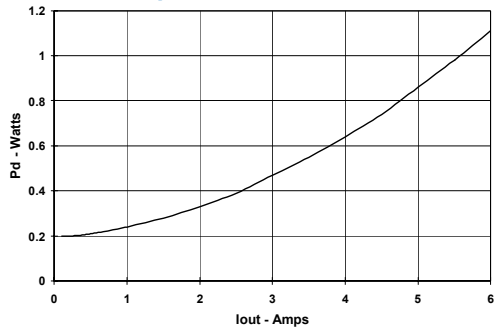
Efficiency vs Load Current



Output Ripple vs Load Current *(See Note 3 to Table)*



Power Dissipation vs Load Current



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The products listed hereunder are prototype or pre-production devices which have not been fully qualified to Astec's specifications. Product specifications are subject to change without notice. Astec makes no warranty, either expressed, implied, or statutory, including implied warranty of merchantability or fitness for a specific purpose, of these products.

Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*

Adjusting the Output Voltage of the ATH06T033 & ATH06T05 Wide-Output Adjust Power Modules

The V_o *Adjust* control (pin 5) sets the output voltage to a value higher than 0.8 V. The adjustment range of the ATH06T033 (3.3-V input) is from 0.8 V to 2.5 V [1], and the ATH06T05-9xx (5-V input) from 0.8 V to 3.6 V. The adjustment method requires the addition of a single external resistor, R_{set}, that must be connected directly between the V_o *Adjust* and *GND* pins [2]. Table 1-1 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

For other output voltages the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 1-2. Figure 1-1 shows the placement of the required resistor.

$$R_{set} = 10\,k\Omega \cdot \frac{0.8\ V}{V_{out} - 0.8\ V} - 2.49\,k\Omega$$

Table 1-1; Preferred Values of R_{set} for Standard Output Voltages

V_{out} (Standard)	R_{set} (Pref'd Value)	V_{out} (Actual)
3.3 V [1]	698 Ω	3.309V
2.5 V	2.21 kΩ	2.502 V
2 V	4.12 kΩ	2.010 V
1.8 V	5.49 kΩ	1.803 V
1.5 V	8.87 kΩ	1.504 V
1.2 V	17.4 kΩ	1.202 V
1 V	36.5 kΩ	1.005 V
0.8 V	Open	0.8 V

Figure 1-1; V_o Adjust Resistor Placement

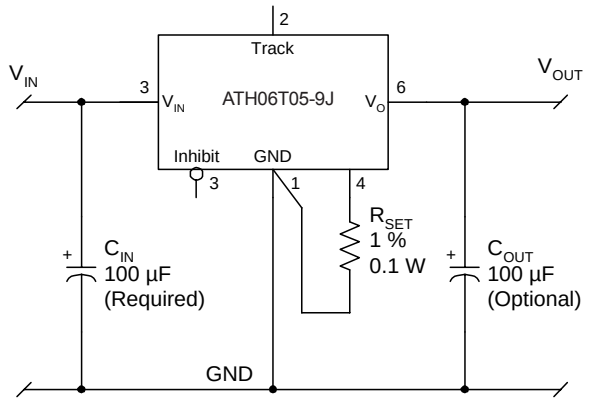


Table 1-2; Output Voltage Set-Point Resistor Values

V_a Req'd	R_{set}	V_a Req'd	R_{set}
0.800	Open	2.00	4.18 kΩ
0.825	318 kΩ	2.05	3.91 kΩ
0.850	158 kΩ	2.10	3.66 kΩ
0.875	104 kΩ	2.15	3.44 kΩ
0.900	77.5 kΩ	2.20	3.22 kΩ
0.925	61.5 kΩ	2.25	3.03 kΩ
0.950	50.8 kΩ	2.30	2.84 kΩ
0.975	43.2 kΩ	2.35	2.67 kΩ
1.000	37.5 kΩ	2.40	2.51 kΩ
1.025	33.1 kΩ	2.45	2.36 kΩ
1.050	29.5 kΩ	2.50	2.22 kΩ
1.075	26.6 kΩ	2.55	2.08 kΩ
1.100	24.2 kΩ	2.60	1.95 kΩ
1.125	22.1 kΩ	2.65	1.83 kΩ
1.150	20.4 kΩ	2.70	1.72 kΩ
1.175	18.8 kΩ	2.75	1.61 kΩ
1.200	17.5 kΩ	2.80	1.51 kΩ
1.225	16.3 kΩ	2.85	1.41 kΩ
1.250	15.3 kΩ	2.90	1.32 kΩ
1.275	14.4 kΩ	2.95	1.23 kΩ
1.300	13.5 kΩ	3.00	1.15 kΩ
1.325	12.7 kΩ	3.05	1.07 kΩ
1.350	12.1 kΩ	3.10	988 Ω
1.375	11.4 kΩ	3.15	914 Ω
1.400	10.8 kΩ	3.20	843 Ω
1.425	10.3 kΩ	3.25	775 Ω
1.450	9.82 kΩ	3.30	710 Ω
1.475	9.36 kΩ	3.35	647 Ω
1.50	8.94 kΩ	3.40	587 Ω
1.55	8.18 kΩ	3.45	529 Ω
1.60	7.51 kΩ	3.50	473 Ω
1.65	6.92 kΩ	3.55	419 Ω
1.70	6.4 kΩ	3.60	367 Ω
1.75	5.93 kΩ		
1.80	5.51 kΩ		
1.85	5.13 kΩ		
1.90	4.78 kΩ		
1.95	4.47 kΩ		

Notes:

1. Modules that operate from a 3.3-V input bus should not be adjusted higher than 2.5 V.
2. Use a 0.1 W resistor. The tolerance should be 1 %, with temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.
3. Never connect capacitors from V_o *Adjust* to either *GND* or V_{out}. Any capacitance added to the V_o *Adjust* pin will affect the stability of the regulator.

ATH06T033/T05: Capacitor Recommendations

Input Capacitor

The recommended input capacitance is determined by 100 µF minimum capacitance, and 300 mA (rms) minimum ripple current rating.

Ripple current and less than 300 mΩ equivalent series resistance (ESR) values are the major considerations, along with temperature, when designing with different types of capacitors.

Tantalum capacitors have a recommended minimum voltage rating of twice 2× (the maximum DC voltage + AC ripple). This is standard practice for tantalum capacitors to insure reliability.

Output Capacitors (Optional)

The ESR of the recommended capacitors is equal to or less than 300 mΩ. Electrolytic capacitors have marginal ripple performance at frequencies greater than 400 kHz but excellent low frequency transient response. Above the ripple frequency, ceramic capacitors are necessary to improve the transient response and reduce any high frequency noise components apparent during higher current excursions.

Tantalum/ Ceramic Capacitors

Tantalum capacitors are acceptable on the output bus. Tantalum, Os-con, or ceramic capacitor types are recommended for applications where ambient temperatures fall below 0 °C. Ceramic capacitors may be used instead of electrolytic types on both the input and output bus. The input bus must have the minimum amount of capacitance. A single 10 µF ceramic capacitor may also be used on the output bus to reduce output ripple.

Capacitor Table

Table 2-1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR are the critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Table 2-1: Recommended Input/Output Capacitors

Capacitor Vendor/ Component Series	Capacitor Characteristics					Quantity		
	Working Voltage	Value (µF)	(ESR) Equivalent Series Resistance	Max Ripple at 85 °C Current (Irms)	Physical Size (mm)	Input Bus	Output Bus	Vendor Number
Panasonic FC (SMT WA (SMT)	25 V 10 V	100 µF 120 µF	0.300 Ω 0.035 Ω	450 mA 2800 mA	8×10 8.3×6.9	1 1	1 1	EEVFC1E101P EEFWA1A121P
Panasonic FC FK (SMT)	16 V 16 V	220 µF 330 µF	0.150 Ω 0.160 Ω	555 mA 600 mA	10×10.2 8×10.2	1 1	1 1	EEUFC1C221 EEVFK1C331P
United Chemi–Con FS PXA (SMT) MVZ (SMT) PS	 10 V 10 V 16 V 10 V	 100 µF 120 µF 220 µF 270 µF	 0.040 Ω 0.027 Ω 0.170 Ω 0.014 Ω	 2100 mA 2430 mA 450 mA 4420 mA	 6.3×9.8 8×6.7 8×10 8×11.5	 1 1 1 1	 1 1 1 1	 10FS100M PXA10VC121MH80TP MVZ25VC221MH10TP 10PS270MH11
Nichicon WG (SMT) F55 PM	 35 V 10 V 25 V	 100 µF 100 µF 150 µF	 0.150 Ω 0.055 Ω 0.160 Ω	 670 mA 2000 mA 460 mA	 10×10 7,7x4,3 10×11.5	 1 1 1	 1 1 1	 UWG1V101MNR1GS F551A107MN UPM1E151MPH
Sanyo Os-con® SVP (SMT) SP TPA	 10 V 16 V 10 V	 120 µF 100 µF 100 µF	 0.040 Ω 0.025 Ω 0.080 Ω	 >2500 mA >2800 mA >1200 mA	 7×8 6.3×9.8 7.3×4.8	 1 1 1	 1 1 1	 10SVP120M 16SPS100M 10TPA100M
AVX Tantalum TPS	10 V 10 V	100 µF 220 µF	0.100 Ω 0.100 Ω	>1090 mA >1414 mA	7.3L ×4.3W ×4.1H	1 1	1 1	TPSD107M010R0100 TPSV227M010R0100
Kemet T520 T495	10 V 10 V	100 µF 100 µF	0.080 Ω 0.100 Ω	1200 mA >1100 mA	7.3L ×5.7W ×4.0H	1 1	1 1	T520D107M010AS T495X107M010AS
Sprague 594D/595D	10 V 10 V	150 µF 120 µF	0.090 Ω 0.140 Ω	1100 mA >1000 mA	7.3L ×6.0W ×4.1H	1 1	1 1	594D157X0010C2T 595D127X0010D2T
TDK- Ceramic X5R Murata Ceramic X5R 1210 Case	6.3 V 6.3 V	47 µF 47 µF	0.002 Ω 0.002 Ω	>1400 mA >1000 mA	3.6L ×2.8W ×2.8H	2 2	2 2	C3225X5R0J476KT/MT GRM32ER60J476M/6.3

Features of the ATH Family of Non-Isolated Wide Output Adjust Power Modules

Point-of-Load Alliance

The ATH family of non-isolated, wide-output adjust power modules are optimized for applications that require a flexible, high performance module that is small in size. These products are part of the "Point-of-Load Alliance" (POLA), which ensures compatible footprint, interoperability and true second sourcing for customer design flexibility. The POLA is a collaboration between Texas Instruments, Artesyn Technologies, and Astec Power to offer customers advanced non-isolated modules that provide the same functionality and form factor. Product series covered by the alliance includes the ATH06 (6 A), ATH10 (10 A), ATH12/15 (12/15 A), ATH18/22 (18/22 A), and the ATH26/30 (26/30 A).

From the basic, "Just Plug it In" functionality of the 6-A modules, to the 30-A rated feature-rich ATH30 Series, these products were designed to be very flexible, yet simple to use. The features vary with each product. Table 3-1 provides a quick reference to the available features by product and input bus voltage.

Table 3-1; Operating Features by Series and Input Bus Voltage

Series	Input Bus	I_{OUT}	Adjust (Trim)	On/Off Inhibit	Over-Current	Pre-Bias Startup	Auto-Track™	Margin Up/Down	Output Sense	Thermal Shutdown
ATH06	3.3 V	6 A	•	•	•	•	•			
	5 V	6 A	•	•	•	•	•			
	12 V	6 A	•	•	•		•			
ATH10	3.3 V / 5 V	10 A	•	•	•	•	•	•	•	
	12 V	10 A	•	•	•		•	•	•	
ATH12/15	3.3 V / 5 V	15 A	•	•	•	•	•	•	•	
	12 V	12 A	•	•	•		•	•	•	
ATH18/22	3.3 V / 5 V	22 A	•	•	•	•	•	•	•	•
	12 V	18 A	•	•	•		•	•	•	•
ATH26/30	3.3 V / 5 V	30 A	•	•	•	•	•	•	•	•
	12 V	26 A	•	•	•	•	•	•	•	•

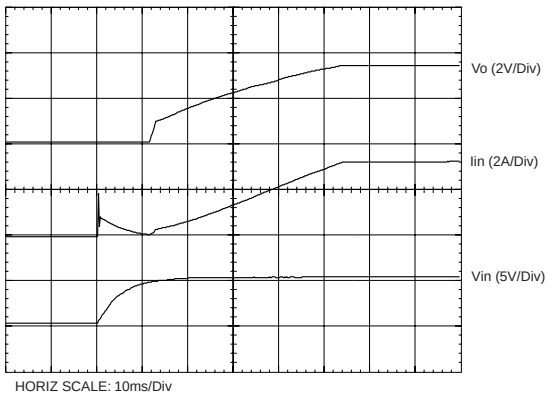
For simple point-of-use applications, the ATH06 (6A) provides operating features such as an on/off inhibit, output voltage trim, pre-bias startup (3.3/5-V input only), and over-current protection. The ATH10 (10 A), and ATH12/15 (12/15 A) include an output voltage sense, and margin up/down controls. Then the higher output current, ATH18/22 (18/22A) and ATH26/30 (26/30A) products incorporate over-temperature shutdown protection. All of the products referenced in Table 3-1 include Auto-Track™.

This is a feature unique to the ATH family, and was specifically designed to simplify the task of sequencing the supply voltage in a power system. These and other features are described in the following sections.

Power-Up Characteristics

When configured per their standard application all the ATH products will produce a regulated output voltage following the application of a valid input source voltage. All the modules include soft-start circuitry. This slows the initial rate in which the output voltage can rise, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry also introduces a short time delay (typically 5 ms-10 ms) into the power-up characteristic. This delay is from the point that a valid input source is recognized, to the initial rise of the output voltage. Figure 3-1 shows the power-up characteristic of the 22-A output product (ATH22T05-9xx), operating from a 5-V input bus and configured for a 3.3-V output. The waveforms were measured with a 5-A resistive load. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors.

Figure 3-1



Over-Current Protection

For protection against load faults, all modules incorporate output over-current protection. Applying a load that exceeds the regulator's over-current threshold will cause the regulated output to shut down. Following shutdown a module will periodically attempt to recover by initiating a soft-start power-up. This is described as a "hiccup" mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Output On/Off Inhibit

For applications requiring output voltage on/off control, each series of the ATH family incorporates an output *Inhibit* control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the *Inhibit* pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_{in} with respect to *GND*.

Figure 3-2 shows the typical application of the inhibit function. Note the discrete transistor (Q_1). The *Inhibit* control has its own internal pull-up to V_{in} potential. The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

Turning Q_1 on applies a low voltage to the *Inhibit* control pin and disables the output of the module. If Q_1 is then turned off, the module will execute a soft-start power-up sequence. A regulated output voltage is produced within 20 msec. Figure 3-3 shows the typical rise in both the output voltage and input current, following the turn-off of Q_1. The turn off of Q_1 corresponds to the rise in the waveform, Q_1 V_{ds}. The waveforms were measured with a 5-A load.

Figure 3-2

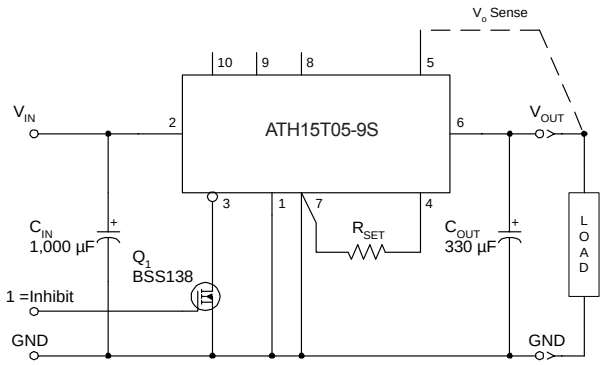
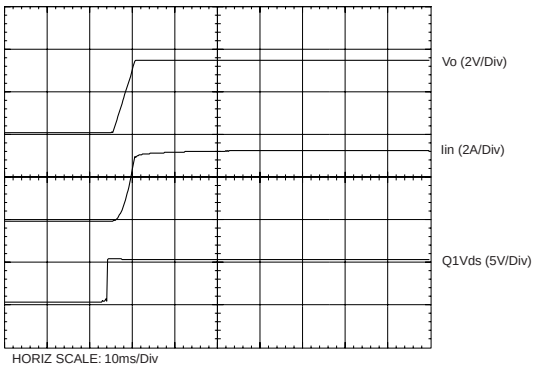


Figure 3-3



Remote Sense

The ATH10, ATH12/15, ATH18/22, and ATH26/30 products incorporate an output voltage sense pin, *V_o Sense*. The *V_o Sense* pin should be connected to V_{out} at the load circuit (see data sheet standard application). A remote sense improves the load regulation performance of the module by allowing it to compensate for any 'IR' voltage drop between itself and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance. Use of the remote sense is optional. If not used, the *V_o Sense* pin can be left open-circuit. An internal low-value resistor (15-Ω or less) is connected between the *V_o Sense* and V_{out}. This ensures the output voltage remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the V_{out} and *GND* pins, and that measured from *V_o Sense* to *GND*, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

Note: The remote sense feature is not designed to compensate for the forward drop of non-linear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

Over-Temperature Protection

The ATH18/22 and ATH26/30 series of products have over-temperature protection. These products have an on-board temperature sensor that protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's *Inhibit* control is automatically pulled low. This turns the output off. The output voltage will drop as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the the sensed temperature decreases by about 10 °C below the trip point.

Note: The over-temperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and will reduce the long-term reliability of the module. Always operate the regulator within the specified Safe Operating Area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

Auto-Track™ Function

The Auto-Track™ function is unique to the ATH family, and is available with the all "Point-of-Load Alliance" (POLA) products. Auto-Track™ was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications, that use dual-voltage VLSI ICs such as DSPs, micro-processors, and ASICs.

How Auto-Track™ Works

Auto-Track™ works by forcing the module's output voltage to follow a voltage presented at the *Track* control pin. This control range is limited to between 0 V and the module's set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module's output remains at its set-point [1]. As an example, if the Track pin of a 2.5-V regulator is at 1 V, the regulated output will be 1 V. But if the voltage at the Track pin rises to 3 V, the regulated output will not go higher than 2.5 V.

When under track control, the regulated output from the module follows the voltage at its Track pin on a volt-for-volt basis. By connecting the Track pin of a number of these modules together, the output voltages will follow a common signal during power-up and power-down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit [3]. The Track control also incorporates an internal RC charge circuit. This operates off the module's input voltage to produce a suitable rising waveform at power up.

Typical Application

The basic implementation of Auto-Track™ allows for simultaneous voltage sequencing of a number of Auto-Track™ compliant modules. Connecting the Track control pins of two or more modules forces the Track control of all modules to follow the same collective RC ramp waveform, and allows them to be controlled through a single transistor or switch; Q_1 in Figure 3-4.

To initiate a power-up sequence, it is recommended that the Track control be first pulled to ground potential. This should be done at or before input power is applied to the modules, and then held for at least 10 ms thereafter. This brief period gives the modules time to complete their internal soft-start initialization. Applying a logic-level high signal to the circuit's On/Off Control turns Q_1 on and applies a ground signal to the Track pins. After completing their internal soft-start intialization, the output of all modules will remain at zero volts while Q_1 is on.

10 ms after a valid input voltage has been applied to the modules, Q_1 may be turned off. This allows the track control voltage to automatically rise toward to the modules' input voltage. During this period the output voltage of each module will rise in unison with other modules, to its respective set-point voltage.

Figure 3-5 shows the output voltage waveforms from the circuit of Figure 3-4 after the On/Off Control is set from a high to a low-level voltage. The waveforms, Vo_1 and Vo_2 represent the output voltages from the two power modules, U_1 (3.3 V) and U_2 (2.0 V) respectively. Vo_1 and Vo_2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. Power down is the reverse of power up, and is accomplished by lowering the track control voltage back to zero volts. The important constraint is that a valid input voltage must be maintained until the power down is complete. It also requires that Q_1 be turned off relatively slowly. This is so that the Track control voltage does not fall faster than Auto-Track's slew rate capability, which is 5 V/ms. The components R_1 and C_1 in Figure 3-4 limit the rate at which Q_1 can pull down the Track control voltage. The values of 100 k-ohm and 0.047 µF correlate to a decay rate of about 0.6 V/ms.

The power-down sequence is initiated with a low-to-high transition at the On/Off Control input to the circuit. Figure 3-6 shows the power-down waveforms. As the Track control voltage falls below the nominal set-point voltage of each power module, then its output voltage decays with all the other modules under Auto-Track™ control.

Notes on Use of Auto-Track™

1. The Track pin voltage must be allowed to rise above the module's set-point voltage before the module can regulate at its adjusted set-point voltage.
2. The Auto-Track™ function will track almost any voltage ramp during power up, and is compatible with ramp speeds of up to 5 V/ms.
3. The absolute maximum voltage that may be applied to the Track pin is V_{in}.
4. The module will not follow a voltage at its Track control input until it has completed its soft-start initialization. This takes about 10 ms from the time that the module has sensed that a valid voltage has been applied its input. During this period, it is recommended that the Track pin be held at ground potential.
5. Once its soft-start initialization is complete, the module is capable of both sinking and sourcing current when following the voltage at the Track pin.
6. The Auto-Track™ function can be disabled by connecting the *Track* pin to the input voltage (V_{in}) through a 1-kΩ resistor. When Auto-Track™ is disabled, the output voltage will rise faster following the application of input power.

***Auto-Track is a trademark of Texas Instruments, Inc.*

Figure 3-4; Sequenced Power Up & Power Down Using Auto-Track

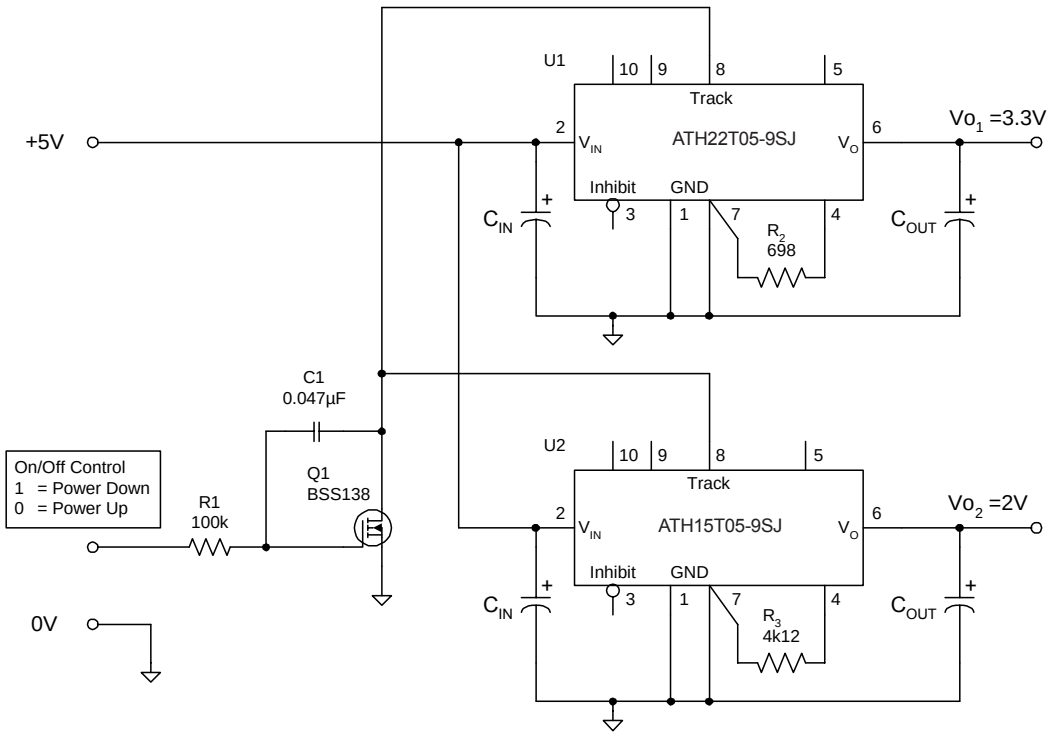


Figure 3-5; Simultaneous Power Up with Auto-Track Control

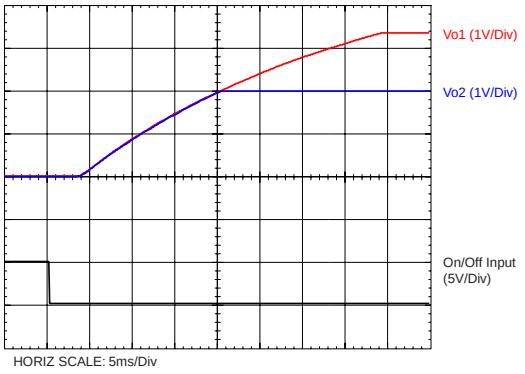
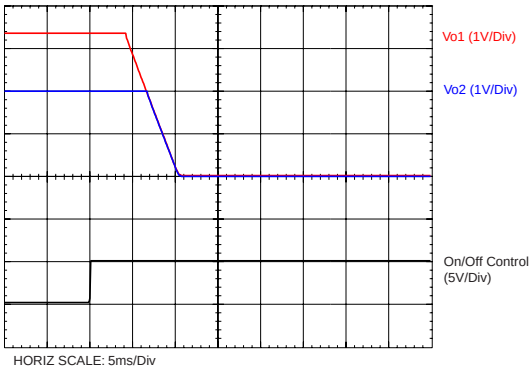


Figure 3-6; Simultaneous Power Down with Auto-Track Control



Margin Up/Down Controls

The ATH10 (10A), ATH12/15 (12/15A), ATH18/22 (18/22A) and ATH26/30 (26/30A) products incorporate *Margin Up* and *Margin Down* control inputs. These controls allow the output voltage to be momentarily adjusted [1], either up or down, by a nominal 5 %. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. The ±5 % change is applied to the adjusted output voltage, as set by the external resistor, R_{set} at the *V_o Adjust* pin.

The 5 % adjustment is made by pulling the appropriate margin control input directly to the *GND* terminal [2]. A low-leakage open-drain device, such as an n-channel MOSFET or p-channel JFET is recommended for this purpose [3]. Adjustments of less than 5 % can also be accommodated by adding series resistors to the control inputs (See Figure 3-4). The value of the resistor can be selected from Table 3-2, or calculated using the following formula.

Up/Down Adjust Resistance Calculation

To reduce the margin adjustment to something less than 5 %, series resistors are required (See R_D and R_U in Figure 3-7). For the same amount of adjustment, the resistor value calculated for R_U and R_D will be the same. The formulas is as follows.

$$R_U \text{ or } R_D = \frac{499}{\Delta\%} - 99.8 \quad k\Omega$$

Where $\Delta\%$ = The desired amount of margin adjust in percent.

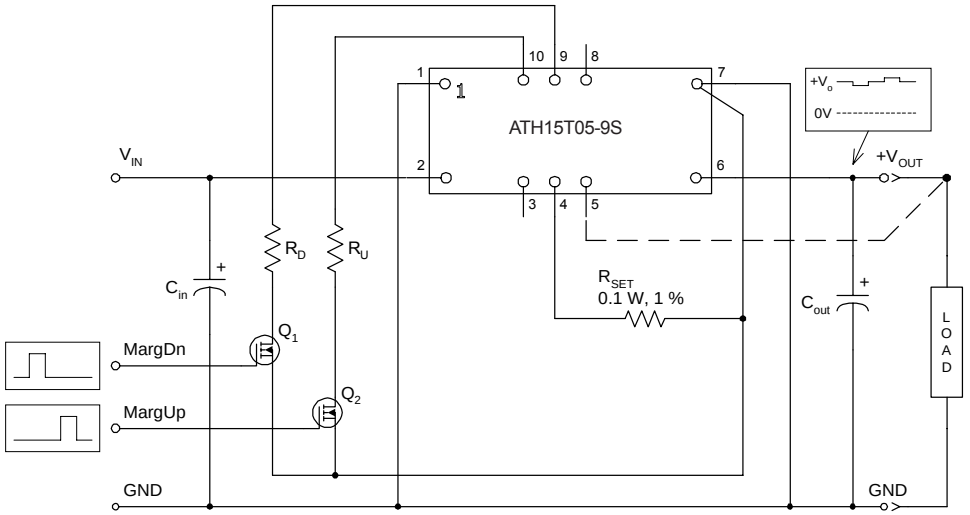
Notes:

1. The *Margin Up** and *Margin Dn** controls were not intended to be activated simultaneously. If they are their affects on the output voltage may not completely cancel, resulting in the possibility of a slightly higher error in the output voltage set point.
2. The ground reference should be a direct connection to the module *GND* at pin 7 (pin 1 for the ATH06). This will produce a more accurate adjustment at the load circuit terminals. The transistors Q_1 and Q_2 should be located close to the regulator.
3. The Margin Up and Margin Dn control inputs are not compatible with devices that source voltage. This includes TTL logic. These are analog inputs and should only be controlled with a true open-drain device (preferably a discrete MOSFET transistor). The device selected should have low off-state leakage current. Each input sources 8 µA when grounded, and has an open-circuit voltage of 0.8 V.

Table 3-2; Margin Up/Down Resistor Values

% Adjust	R_U / R_D
5	0.0 kΩ
4	24.9 kΩ
3	66.5 kΩ
2	150.0 kΩ
1	397.0 kΩ

Figure 3-7; Margin Up/Down Application Schematic



Pre-Bias Startup Capability

Only selected products in the ATH family incorporate this capability. Consult Table 3-1 to identify which products are compliant.

A pre-bias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, these types of modules can sink as well as source output current.

The ATH family of power modules incorporate synchronous rectifiers, but will not sink current during startup [1], or whenever the *Inhibit* pin is held low. However, to ensure satisfactory operation of this function, certain conditions must be maintained. [2] Figure 3-7 shows an application demonstrating the pre-bias startup capability. The start-up waveforms are shown in Figure 3-9. Note that the output current from the ATH15T033-9xx (I_o) shows negligible current until its output voltage rises above that backfed through diodes D_1 and D_2.

Note: The pre-bias start-up feature is not compatible with Auto-Track. When the module is under Auto-Track control, it is fully active and will sink current if the output voltage is below that of a back-feeding source. Therefore to ensure a pre-bias hold-off, one of two approaches must be followed when input power is applied to the module. The Auto-Track function must either be disabled [3], or the module's output held off using the Inhibit pin. The latter allows Auto-Track's internal (RC) voltage ramp to rise above the set-point voltage.

Notes

1. Startup is the relatively short period (approx. 10 ms) prior to the output voltage rising. The startup period immediately follows either the application of a valid input source voltage, or the release of a ground signal at the *Inhibit* pin.
2. To ensure that the regulator does not sink current when power is first applied (even with a ground signal applied to the *Inhibit* control pin), the input voltage must always be greater than the output voltage throughout the power-up and power-down sequence.
3. The Auto-Track function can be disabled at power up by immediately applying a voltage to the module's *Track* pin that is greater than its set-point voltage. This can be easily accomplished by connecting the *Track* pin to V_{in} through a 1-kΩ resistor.

Figure 3.9; Pre-Bias Startup Waveforms

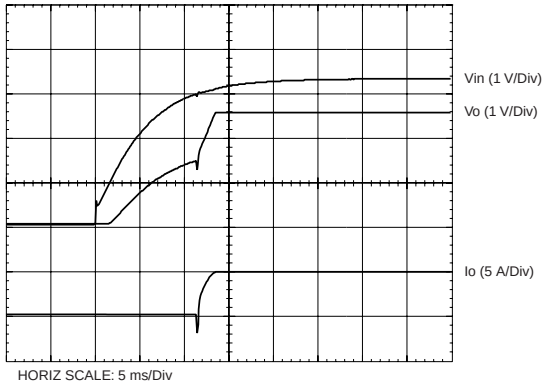
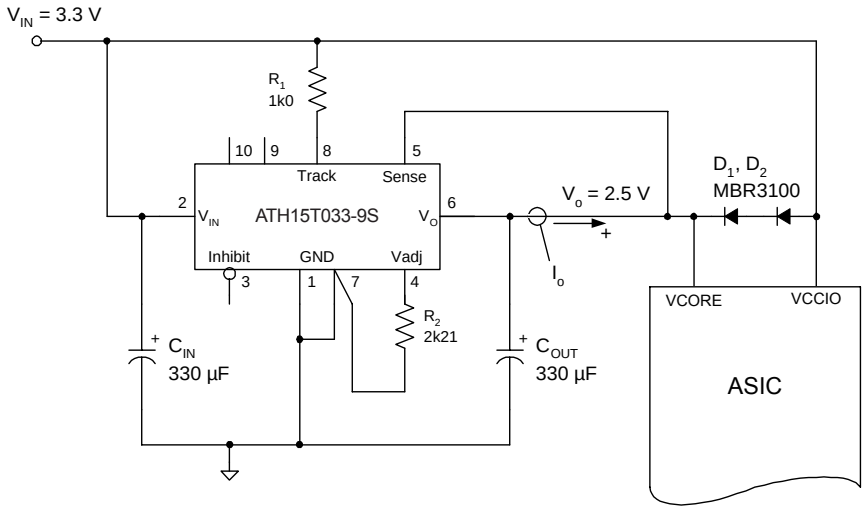
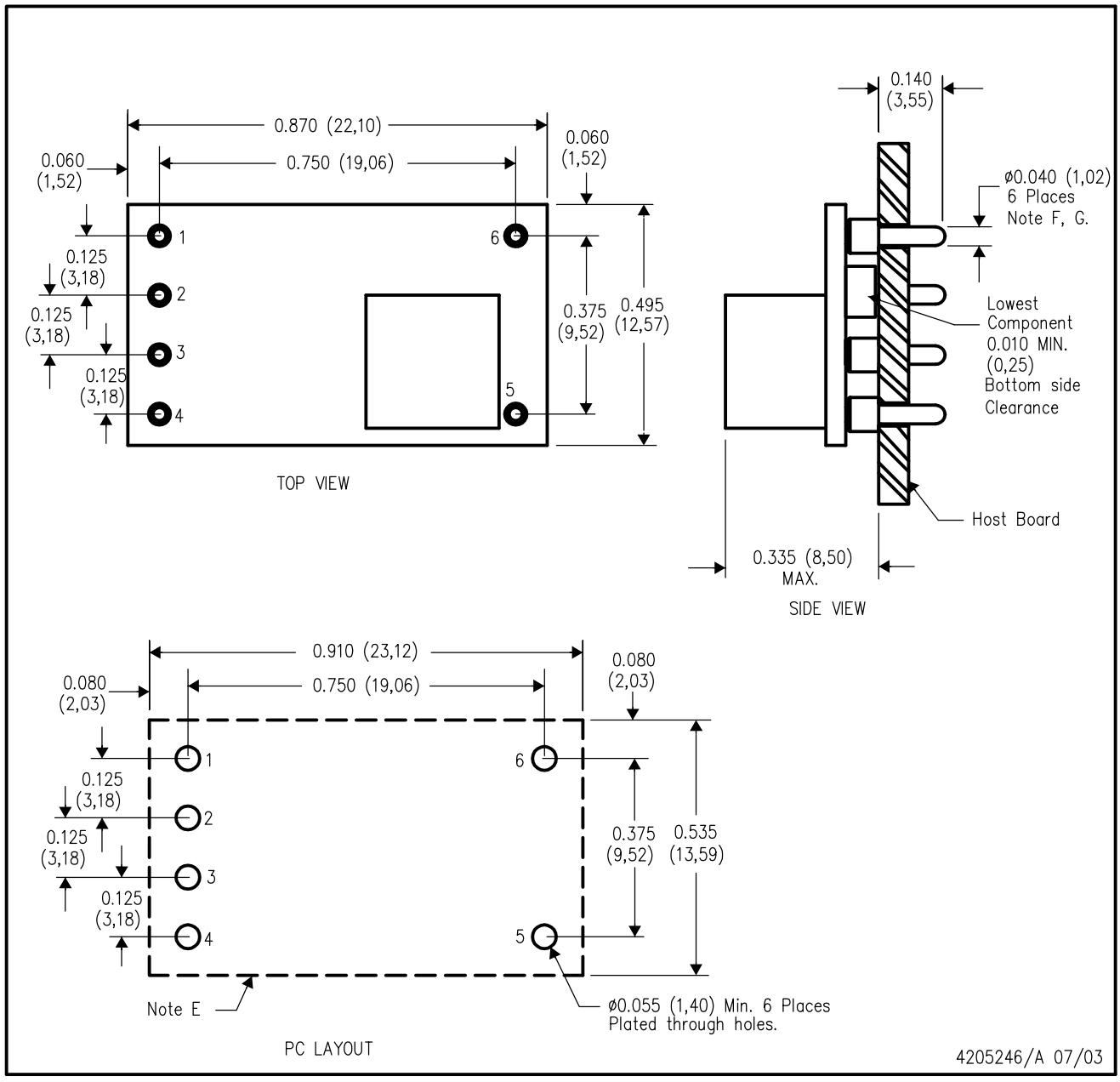


Figure 3.8; Application Circuit Demonstrating Pre-Bias Startup

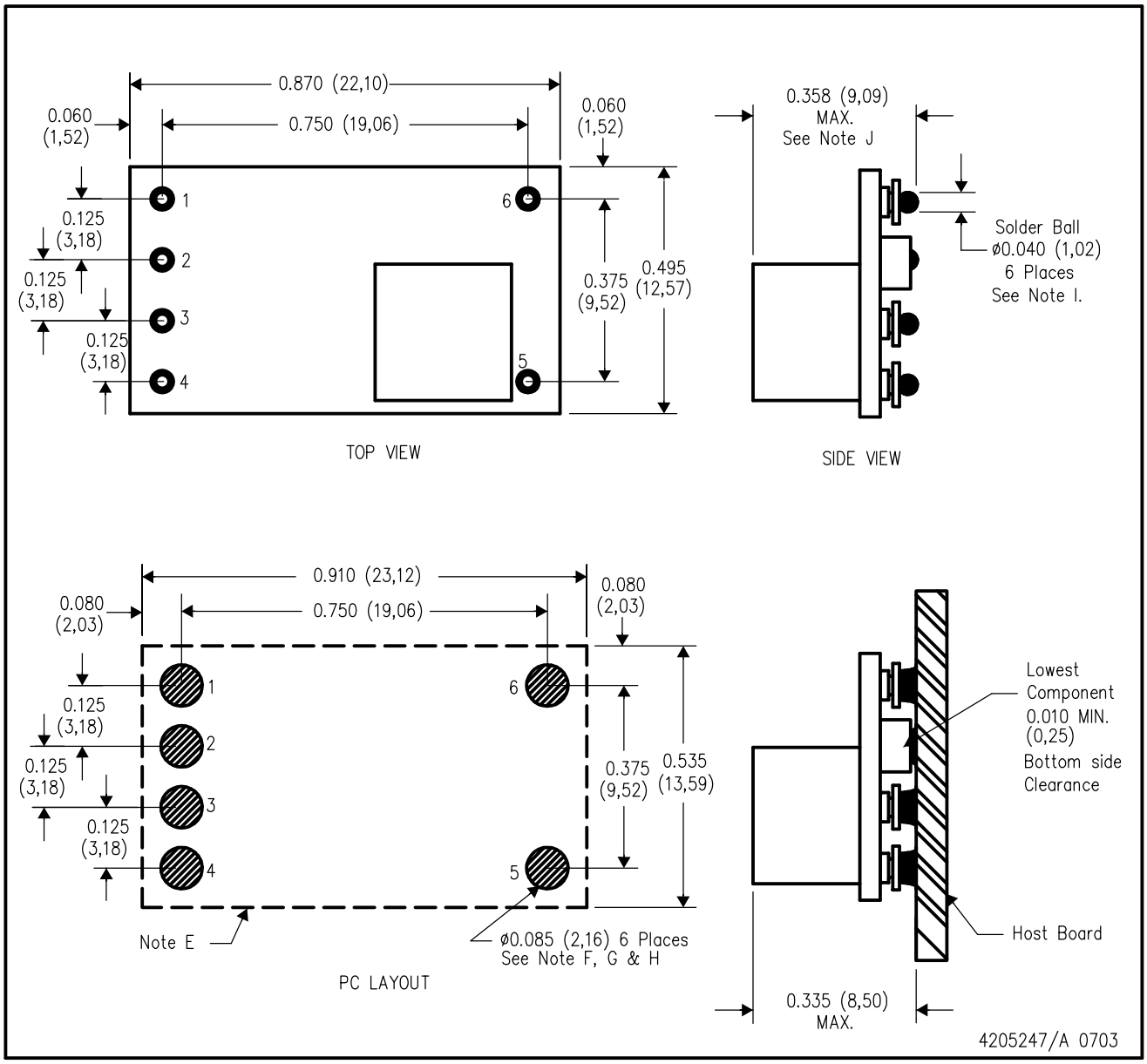


Through Hole Termination



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

Surface Mount Termination



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.