# HD49815TF

## Digital Camera Signal Processor

REJ03F0138-0100
(Previous: ADE-207-316)
Rev.1.00
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### Description

The HD49815TF is a CMOS IC that has been developed as a digital signal-processing IC for CCD-camera digital-signal-processing systems.

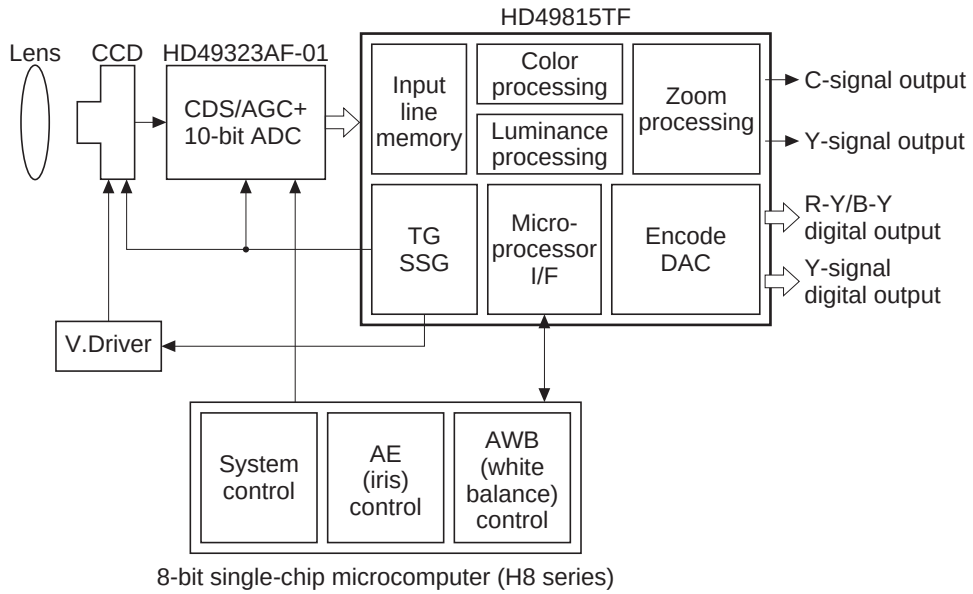
### Functions

- CCD-sensor drive-pulse generation (TG)
- Digital AGC (automatic gain control)
- Color signal separation circuit
- RGB matrix
- RGB gain
- RGB and Y gamma
- Color-difference matrix
- Enhancer
- RGB and Y setup
- Digital I/F (4:2:2)
- Zoom control
- Mirror reversal
- Synchronization signal generator for encoding (SSG)
- AWB, AE, and AF detection
- Two-channel 8-bit D/A converter

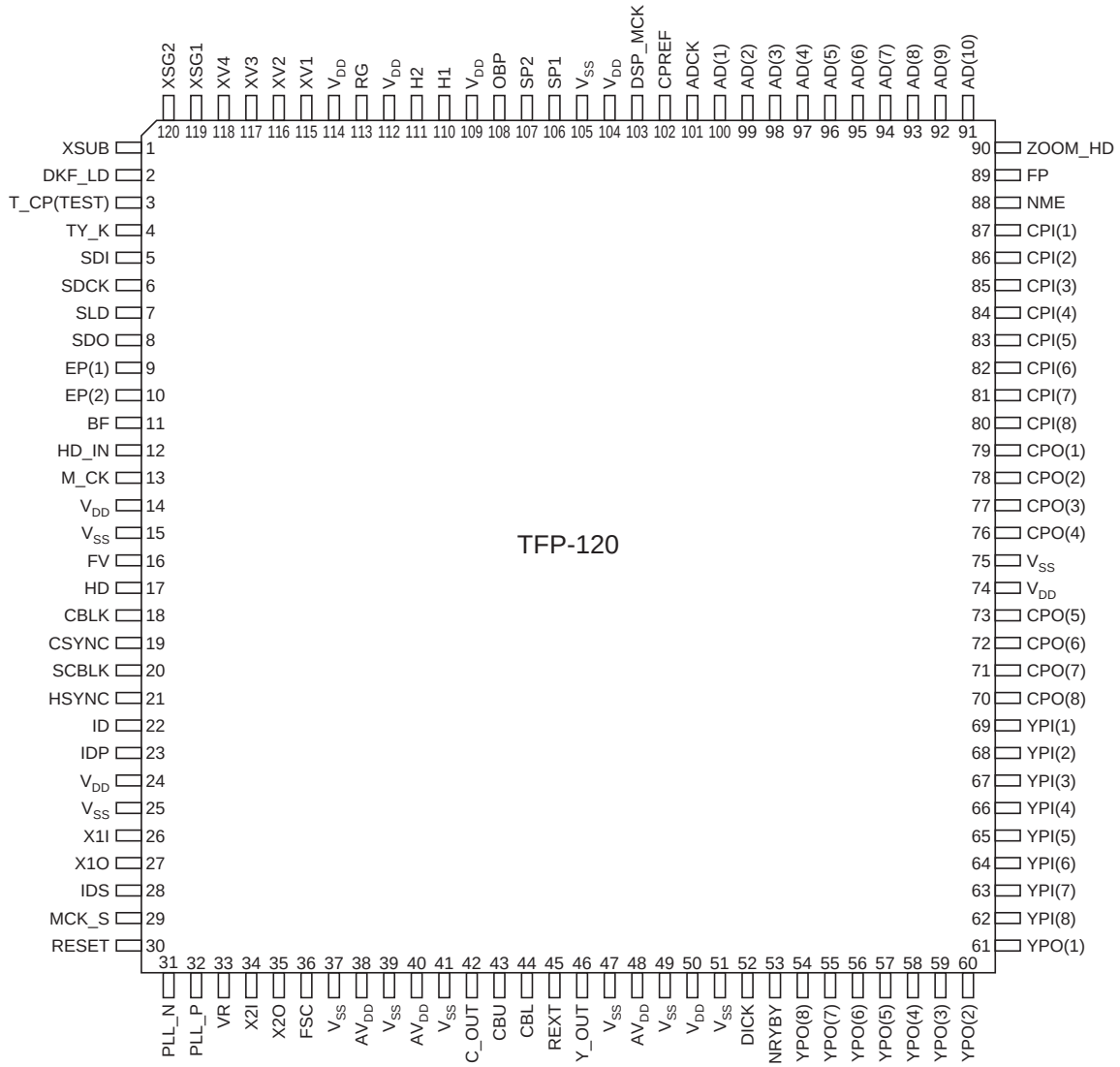
### Features

- The HD49815TF provides camera-signal processing, TG, SSG, zoom, and D/A functions and other functions in a single chip and supports high system-integration level.
- In conjunction with the HD49323AF-01 (CDS/AGC + 10-bit ADC) and the control microcomputer, the HD49815TF forms a three-chip kit that can implement an optimal CCD-camera digital-signal-processing system.
- The HD49815TF provides the zoom function and controls the 1- to 256- times linear zoom. It also provides the half-mirror function.
- Since the HD49815TF can be made compatible with the former product, HD49811TFA, through software, a shorter development term is enabled.
- Since software controls AWB, AE, and AF, any protocol can be prepared according to the camera shooting conditions.
- Programmable TG enables use of any CCD device.

## System Block Diagram



## Pin Arrangement




(Top view)

## Pin Description

| Pin No. | Symbol | Pin Name | I/O | Description | I/O Format |
|---|---|---|---|---|---|
| 1 | XSUB | CCD shutter pulse | O | CCD control pulse | ZC2R |
| 2 | DKF_LD | Line input LD | I | Line input dedicated load | ICS |
| 3 | T_CP | Test | I | Test pin (GND input) | IC |
| 4 | TY_K | Title SW | I | Title-killer SW (1 = On, 0 = Off) | ICD |
| 5 | SDI | State data input | I | State data-setting data input | IC |
| 6 | SDCK | State data clock | I | State data-setting clock | ICS |
| 7 | SLD | State data load pulse | I | State data-latch pulse | ICS |
| 8 | SDO | AWB, AE, data output | O | AWB, AE, and AF detection-data output | ZC2R |
| 9 | EP (1) | AE window pulse 1 | O | Iris detection-area-setting pulse: SP-A7 [8] output changeover | ICZC2R |
| 10 | EP (2) | AE window pulse 2 | O | Iris detection-area-setting pulse: SP-A7 [8] output changeover | ICZC2R |
| 11 | BF | Burst flag | O | Burst flag output | ICZC2R |
| 12 | HD_IN | External CSYNC input | I | External CSYNC input | ICSD |
| 13 | M_CK | Microprocessor clock | O | Microprocessor clock output (1/2 or 1/4 dividing of X'tal 1) | OC2R |
| 14 | $V_{DD}$ | $V_{CC}2$ | — | 3.3 V power supply | VCCI |
| 15 | $V_{SS}$ | GND | — | GND | GNDI |
| 16 | FV | Field vertical output | O | Vertical synchronization pulse | ICZC2R |
| 17 | HD | HD output | O | Horizontal synchronization pulse | ICZC2R |
| 18 | CBLK | Blanking pulse | O | Blanking pulse | ICZC2R |
| 19 | CSYNC | SYNC output | O | SYNC pulse | ICZC2R |
| 20 | SCBLK | SC blanking pulse | O | Subcarrier blanking pulse (SECAM) | ICZC2R |
| 21 | HSYNC | Horizontal SYNC | O | Horizontal SYNC pulse (SECAM) | OC2R |
| 22 | ID | Identity | O | SECAM determination pulse | OC2R |
| 23 | IDP | Identity pulse | O | SECAM determination pulse | ICZC2R |
| 24 | $V_{DD}$ | $V_{CC}2$ | — | 3.3 V power supply | VCCC |
| 25 | $V_{SS}$ | GND | — | GND | GNDC |
| 26 | X1I | X'tal 1 input | I | 2fsc oscillator input | IQ3 |
| 27 | X1O | X'tal 1 output | O | 2fsc oscillator output | OQ3 |
| 28 | IDS | Line ID reset input | I | Line-determination-signal input | ICD |
| 29 | MCK_S | MCK output SW | I | Pin 13 MCK dividing setting SW (1 = 1/2, 0 = 1/4) | IC |
| 30 | RESET | Reset | I | Reset: to restore the initial data settings | ICS |
| 31 | PLL_N | PLL negative | O | PLL signal output | ZC2 |
| 32 | PLL_P | PLL positive | O | PLL signal output | ZC2 |
| 33 | VR | Vertical reset | I | Vertical synchronization signal input | ICSD |
| 34 | X2I | X'tal 2 input | I | 4fsc oscillator input | IQ2 |
| 35 | X2O | X'tal 2 output | O | 4fsc oscillator output | OQ2 |
| 36 | FSC | Sub carrier frequency | O | fsc output | ICZC2R |
| 37 | $V_{SS}$ | GND | — | GND | GNDA |
| 38 | $AV_{DD}$ | Analog $V_{CC}2$ | — | Analog system power supply: 3.3 V | VCCA |
| 39 | $V_{SS}$ | GND | — | GND | GNDA |
| 40 | $AV_{DD}$ | Analog $V_{CC}2$ | — | Analog system power supply: 3.3 V | VCCA |
| 41 | $V_{SS}$ | GND | — | GND | GNDA |
| 42 | C_OUT | C analog signal output | O | Chrominance-signal analog output | OA |
| 43 | CBU | Current buffer upper | I | D/A upper current source | IA |
| 44 | CBL | Current buffer lower | I | D/A lower current source | IA |
| 45 | REXT | Reference resister EXT | I | Reference voltage input | IA |

## Pin Description (cont.)

| Pin No. | Symbol | Pin Name | I/O | Description | I/O Format |
|---|---|---|---|---|---|
| 46 | Y_OUT | Y analog signal output | O | Luminance-signal analog output | OA |
| 47 | $V_{SS}$ | GND | — | GND | GNDA |
| 48 | $AV_{DD}$ | Analog $V_{CC}2$ | — | Analog system power supply: 3.3 V | VCCA |
| 49 | $V_{SS}$ | GND | — | GND | GNDA |
| 50 | $V_{DD}$ | $V_{CC}2$ | — | Digital system power supply: 3.3 V | VCCI |
| 51 | $V_{SS}$ | GND | — | GND | GNDI |
| 52 | DICK | Digital interface clock | O | Digital interface clock output | ICZC2R |
| 53 | NRYBY | R-Y, B-Y phase output | O | Color-difference signal phase clock | ICZC2R |
| 54 | YPO (8) | Y parallel output (8); MSB | O | Luminance-signal digital output MSB | OC2R |
| 55 | YPO (7) | Y parallel output (7) | O | Luminance-signal digital output | OC2R |
| 56 | YPO (6) | Y parallel output (6) | O | Luminance-signal digital output | OC2R |
| 57 | YPO (5) | Y parallel output (5) | O | Luminance-signal digital output | OC2R |
| 58 | YPO (4) | Y parallel output (4) | O | Luminance-signal digital output | OC2R |
| 59 | YPO (3) | Y parallel output (3) | O | Luminance-signal digital output | OC2R |
| 60 | YPO (2) | Y parallel output (2) | O | Luminance-signal digital output | OC2R |
| 61 | YPO (1) | Y parallel output (1) ; LSB | O | Luminance-signal digital output LSB | OC2R |
| 62 | YPI (8) | Y parallel input (8); MSB | I | Luminance-signal digital input MSB | ICD |
| 63 | YPI (7) | Y parallel input (7) | I | Luminance-signal digital input | ICD |
| 64 | YPI (6) | Y parallel input (6) | I | Luminance-signal digital input | ICD |
| 65 | YPI (5) | Y parallel input (5) | I | Luminance-signal digital input | ICD |
| 66 | YPI (4) | Y parallel input (4) | I | Luminance-signal digital input | ICD |
| 67 | YPI (3) | Y parallel input (3) | I | Luminance-signal digital input | ICD |
| 68 | YPI (2) | Y parallel input (2) | I | Luminance-signal digital input | ICD |
| 69 | YPI (1) | Y parallel input (1); LSB | I | Luminance-signal digital input LSB | ICD |
| 70 | CPO (8) | C parallel output (8); MSB | O | Chrominance-signal digital output MSB | OC2R |
| 71 | CPO (7) | C parallel output (7) | O | Chrominance-signal digital output | OC2R |
| 72 | CPO (6) | C parallel output (6) | O | Chrominance-signal digital output | OC2R |
| 73 | CPO (5) | C parallel output (5) | O | Chrominance-signal digital output | OC2R |
| 74 | $V_{DD}$ | $V_{CC}2$ | — | 3.3 V power supply | VCCO |
| 75 | $V_{SS}$ | GND | — | GND | GNDO |
| 76 | CPO (4) | C parallel output (4) | O | Chrominance-signal digital output | OC2R |
| 77 | CPO (3) | C parallel output (3) | O | Chrominance-signal digital output | OC2R |
| 78 | CPO (2) | C parallel output (2) | O | Chrominance-signal digital output | OC2R |
| 79 | CPO (1) | C parallel output (1); LSB | O | Chrominance-signal digital output LSB | OC2R |
| 80 | CPI (8) | C parallel input (8); MSB | I | Chrominance-signal digital input MSB | ICD |
| 81 | CPI (7) | C parallel input (7) | I | Chrominance-signal digital input | ICD |
| 82 | CPI (6) | C parallel input (6) | I | Chrominance-signal digital input | ICD |
| 83 | CPI (5) | C parallel input (5) | I | Chrominance-signal digital input | ICD |
| 84 | CPI (4) | C parallel input (4) | I | Chrominance-signal digital input | ICD |
| 85 | CPI (3) | C parallel input (3) | I | Chrominance-signal digital input | ICD |
| 86 | CPI (2) | C parallel input (2) | I | Chrominance-signal digital input | ICD |
| 87 | CPI (1) | C parallel input (1); LSB | I | Chrominance-signal digital input LSB | ICD |
| 88 | NME | Memory HD output | O | Line memory control output | ICZC2DR |
| 89 | FP | Field pulse | O | Field pulse | ICZC2R |
| 90 | ZOOM_HD | Zoom HD output | O | Horizontal synchronization signal | ICZC2R |
| 91 | AD (10) | AD input (10); MSB | I | A/D data input MSB | IC |
| 92 | AD (9) | AD input (9) | I | A/D data input | IC |
| 93 | AD (8) | AD input (8) | I | A/D data input | IC |
| 94 | AD (7) | AD input (7) | I | A/D data input | IC |

## Pin Description (cont.)

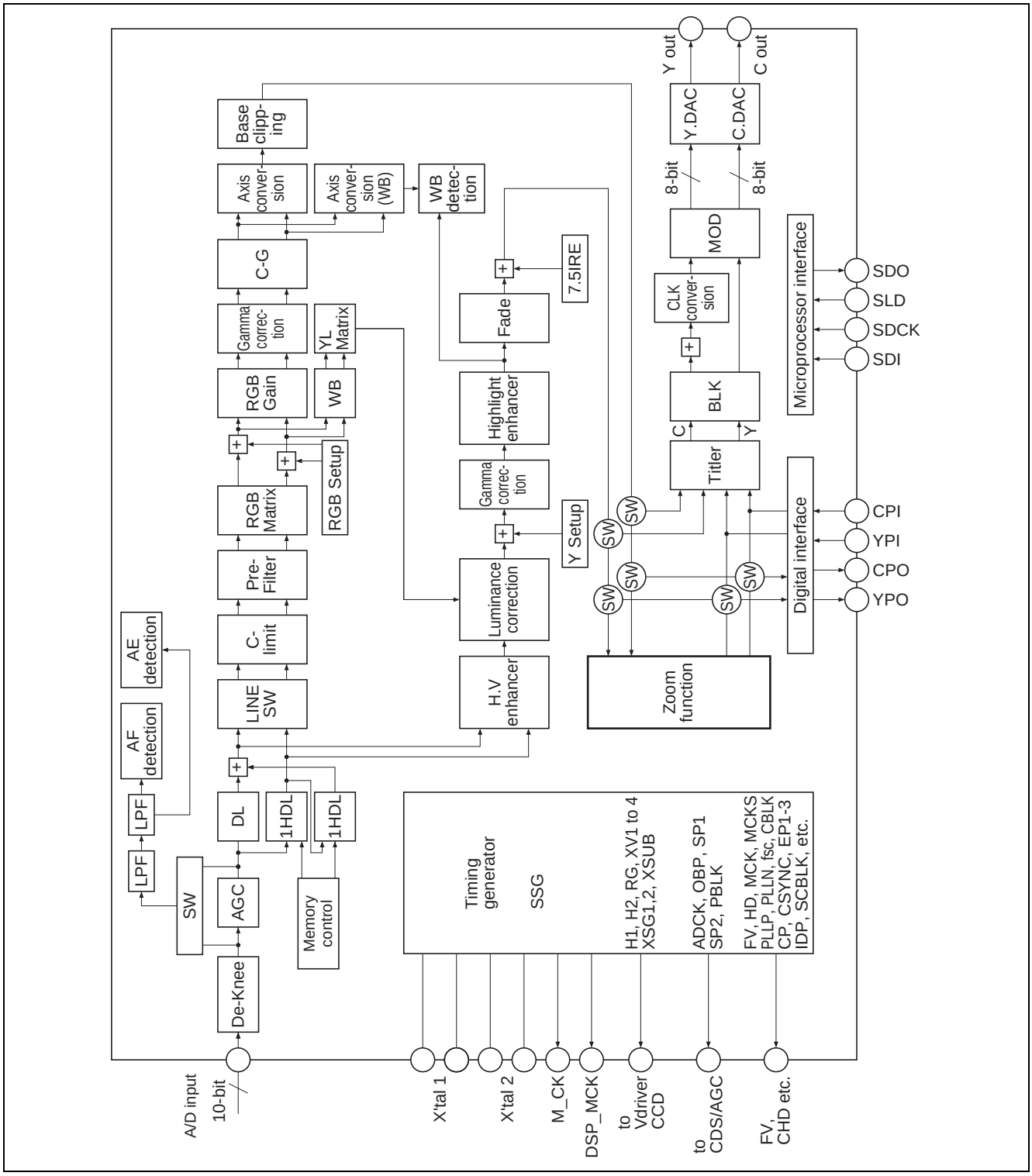
| Pin No. | Symbol | Pin Name | I/O | Description | I/O Format |
|---|---|---|---|---|---|
| 95 | AD (6) | AD input (6) | I | A/D data input | IC |
| 96 | AD (5) | AD input (5) | I | A/D data input | IC |
| 97 | AD (4) | AD input (4) | I | A/D data input | IC |
| 98 | AD (3) | AD input (3) | I | A/D data input | IC |
| 99 | AD (2) | AD input (2) | I | A/D data input | IC |
| 100 | AD (1) | AD input (1); LSB | I | A/D data input LSB | IC |
| 101 | ADCK | AD clock | O | A/D converter clock | ICZC2R |
| 102 | CPREF | Clamp reference output | O | Clamp reference pulse | 2C3 |
| 103 | DSP_MCK | Microprocessor clock output | O | Microprocessor clock output: SP-A7 [8] output changeover | ICZC2R |
| 104 | $V_{DD}$ | $V_{CC}2$ | — | 3.3 V power supply | VCCO |
| 105 | $V_{SS}$ | GND | — | GND | GNDO |
| 106 | SP1 | Sampling pulse 1 | O | Sampling pulse for the AGC/CDS IC | ICZC2 |
| 107 | SP2 | Sampling pulse 2 | O | Sampling pulse for the AGC/CDS IC | ICZC2 |
| 108 | OBP | OBP pulse | O | Optical black-pulse output | ICZC2R |
| 109 | $V_{DD}$ | $V_{CC}1$ | — | 3 V or 5 V power supply (H1/H2 power supply) | VCCC35 |
| 110 | H1 | H1 | O | CCD-sensor horizontal drive pulse | OC3R |
| 111 | H2 | H2 | O | CCD-sensor horizontal drive pulse | OC3R |
| 112 | $V_{DD}$ | $V_{CC}1$ | — | 5 V power supply (RG power supply) | VCCC5 |
| 113 | RG | Reset gate | O | CCD-sensor control reset gate | ZC3R |
| 114 | $V_{DD}$ | $V_{CC}2$ | — | 3.3 V power supply | VCCO |
| 115 | XV1 | XV1 | O | CCD-sensor vertical control pulse | ICZC2R |
| 116 | XV2 | XV2 | O | CCD-sensor vertical control pulse | ICZC2R |
| 117 | XV3 | XV3 | O | CCD-sensor vertical control pulse | ICZC2R |
| 118 | XV4 | XV4 | O | CCD-sensor vertical control pulse | ICZC2R |
| 119 | XSG1 | XSG1 | O | CCD-sensor vertical control pulse | ZC2R |
| 120 | XSG2 | XSG2 | O | CCD-sensor vertical control pulse | ZC2R |

## Description of I/O Format

| I/O Format | Contents |
|---|---|
| IC | CMOS level input |
| ICD | CMOS level input with pull-down resistor |
| ICS | CMOS level schmitt input |
| ICSD | CMOS level input with pull-down resistor |
| ICZC2 | CMOS level common I/O (4 mA) |
| ICZC2DR | CMOS level common I/O with pull-down resistor and through-put control (4 mA) |
| ICZC2R | CMOS level common I/O with through-put control (4 mA) |
| OC2R | CMOS level output with through-put control (4 mA) |
| OC3R | CMOS level output with through-put control (8 mA) |
| IQ2 | Crystal oscillator input |
| OQ2 | Crystal oscillator output |
| IQ3 | Crystal oscillator input |
| OQ3 | Crystal oscillator output |
| ZC2 | CMOS-level three-state output (4 mA) |
| ZC2R | CMOS-level three-state output with through-put control (4 mA) |
| ZC3 | CMOS-level three-state output (8 mA) |
| ZC3R | CMOS-level three-state output with through-put control (8 mA) |
| VCCI | Core system power supply: 3 V |
| VCCO | Puddling system power supply: 3 V |
| VCCC | Common power supply: 3 V |
| VCCC5 | Common power supply: 5 V for pin 112 |
| VCCC35 | Common power supply: 3 or 5 V for pin 109 |
| GNDI | Core system GND |
| GNDO | Puddling system GND |
| GNDC | Common GND |
| IA | Analog input |
| OA | Analog output |
| VCCA | Analog power supply |
| GNDA | Analog GND |

Notes: 1. Pin 113 is used for 5 V system output.
2. Pins 110 and 111 are used for 3 V or 5 V system output. They depend on the voltage of pin 109.

## Block Diagram



## Absolute Maximum Ratings

(Ta = 25°C)

| Item | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Power supply voltage | | $V_{CC}$ | –0.2 to +6.8 | V |
| Pin voltage (5 V operation block) | | Vt5V | –0.2 to $V_{CC}1$ +0.2 | V |
| Pin voltage (3 V operation block) | | Vt3V | –0.2 to $V_{CC}2$ +0.2 | V |
| Output current | Per output | Io | –32 to +32 | mA |
| | Per GND-$V_{CC}$ pair | Iot | –72 to +72 | mA |
| Allowable power dissipation | | Popr | 450 | mW |
| Operating temperature | | Topr | –10 to +75 | °C |
| Storage temperature | With bias | Tbias | –10 to +75 | °C |
| | Without bias | Tstg | –40 to +125 | °C |

Notes: 1. Using this LSI at values in excess of the absolute maximum ratings may permanently damage the LSI. The LSI should normally be operated under the conditions specified for the electrical characteristics. Exceeding these conditions may lead to incorrect operation and may adversely affect LSI reliability.

2. All voltage values are referenced to GND = 0 V.
3. The pin voltage ratings also apply to the NC pins.
4. $V_{CC}1$ indicates the 5 V system power supply and $V_{CC}2$ indicates the 3 V system power supply.

## Electrical Characteristics

($V_{CC}1$ = 4.75 V to 5.25 V, $V_{CC}2$ = 2.85 V to 3.15 V, $AV_{CC}$ = 2.85 V to 3.15 V, Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|---|
| CMOS-level input voltage | $V_{IHC}$ | $V_{CC}2\times0.75$ | — | $V_{CC}2$ | V | | |
| | $V_{ILC}$ | 0.0 | — | $V_{CC}2\times0.20$ | V | | |
| CMOS schmitt input voltage | $V_{TC}$+ | 2.50 | — | $V_{CC}2$ | V | $V_{CC}1$ = 5 V<br>$V_{CC}2$ = 3 V | |
| | $V_{TC}$– | 0.0 | — | 0.60 | V | | |
| Output voltage | $V_{OHC1}$ | $V_{CC}1$–0.5 | — | — | V | $I_{OH}$ = –200 µA<br>5 V system pin | 1 |
| | $V_{OLC1}$ | — | — | 0.4 | V | $I_{OL}$ = 200 µA<br>5 V system pin | |
| | $V_{OHC2}$ | $V_{CC}2$–0.5 | — | — | V | $I_{OH}$ = –200 µA<br>3 V system pin | 1, 5 |
| | $V_{OLC2}$ | — | — | 0.4 | V | $I_{OL}$ = 200 µA<br>3 V system pin | 1, 6 |
| Input leakage current | $I_{LI}$ | — | — | 1.0 | µA | $V_{IN}$ = 0 V to $V_{CC}$ | 2 |
| Output leakage current | $I_{LO}$ | — | — | 1.0 | µA | Output Hi-Z conditions | 2 |
| Pull-down current | $I_{PD}$ | 5 | — | 100 | µA | $V_{IN}$ = $V_{CC}2$ = 3 V | |
| Power dissipation | Popr | — | — | 450 | mW | $V_{CC}1$ = 5 V,<br>$V_{CC}2$ = 3 V,<br>$AV_{CC}$ = 3 V | 3 |
| Analog output voltage (full scale) | Vfull | 0.80 | 1.00 | 1.20 | V | | 3, 4 |
| Analog output voltage (zero scale) | Vzero | –0.20 | 0.00 | 0.20 | V | | |
| Differential linearity | DNL | –2.0 | — | 2.0 | LSB | | |

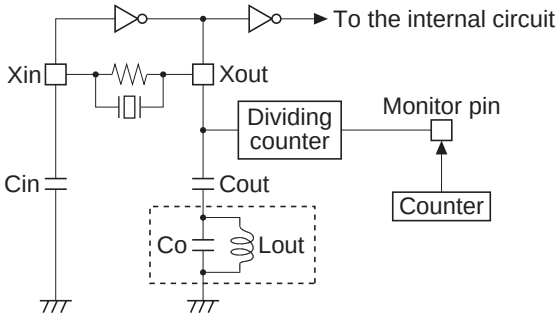
Notes:
1. Output voltage must be measured in the steady state.
2. Except for pins that include a pull-down resistor.
3. Guaranteed at CBU = 0.1 µF, CBL = 0.1 µF, REXT = 3.4 kΩ, analog output load resistance = 500 Ω, and Ta = 25°C.
4. Applied to pins indicated as OA in the I/O format column of the pin-functions table.
5. Because $V_{OH}$ of pin 31 cannot be measured logically, it was not tested.
6. Because $V_{OL}$ of pin 32 cannot be measured logically, it was not tested.
7. $V_{CC}1$, $V_{CC}2$, and $AV_{CC}$ indicate the 5 V system power supply, the 3 V system power supply, and the analog system power supply, respectively. $V_{CC}$ indicates $V_{CC}1$, $V_{CC}2$, and $AV_{CC}$.
8. The voltage range of pin 109 (VCCC35) is $V_{CC}$ = 2.85 V to 5.25 V.

## Crystal Oscillation Circuit

1. Measuring conditions
   The oscillation frequency was measured under the following conditions
   $V_{CC}1$ = 5.0 V
   $V_{CC}2$ = 3 V
   Ta = 25°C
   8 MHz, 20 MHz, and 24 MHz:
      Rf = 1 to 10 MΩ
      Cin, Cout = 20 pF (±20 pF)
   32 MHz:
      Rf = 1 to 10 MΩ
      Cin = 20 pF (±20 pF)
      Cout = 100 pF (±20 pF), Co = 15 pF (±5 pF), Lout = 1 µH
   The conditions above may be changed within the range of measuring conditions.
2. Measuring method
   Under the measuring conditions above, two methods were tested.
   fmin. = 20 MHz, and fmax. = 32 MHz (applied to pins 26 and 27)
   fmin. = 8 MHz, and fmax. = 24 MHz (applied to pins 34 and 35)

Note: The oscillation start time tosc is max. = 200 ms.

3. Measuring circuit




Note: The part enclosed by the dotted line in the above circuit is used when measuring at 32 MHz.

**Figure 1 Measuring Circuit**

# Built-in Functions and System Configuration

## System Configuration

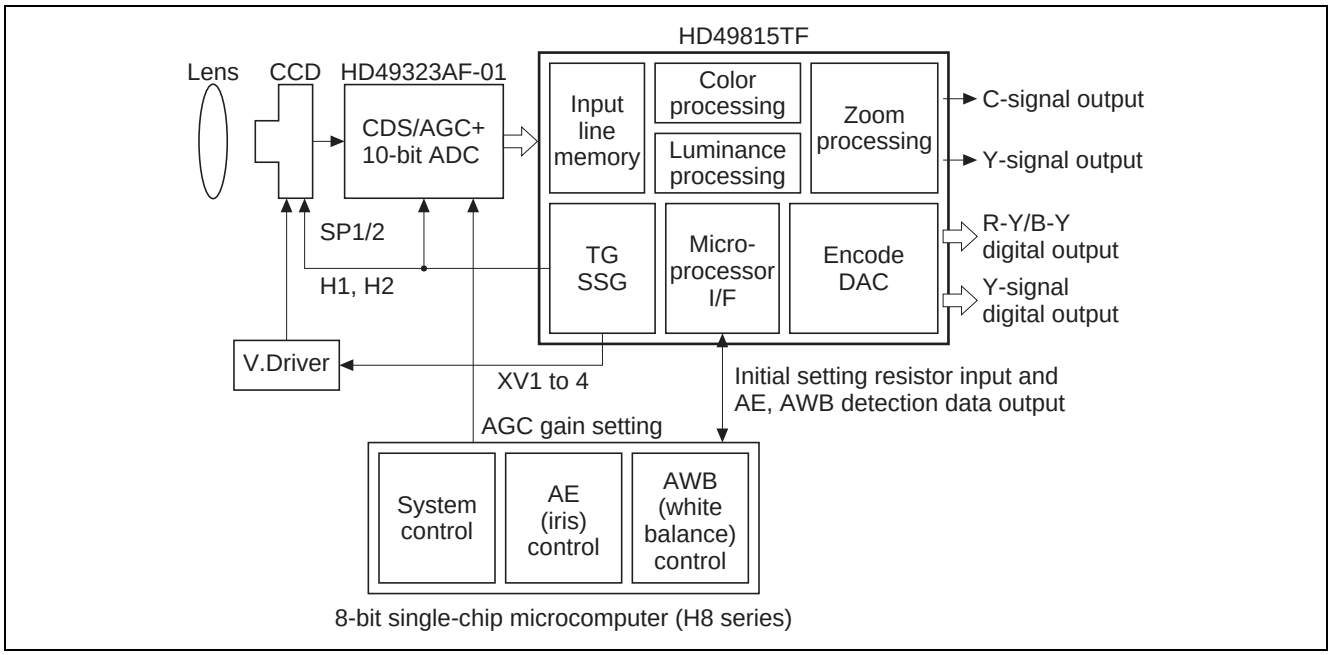



**Figure 2 System Configuration**

## System Description

1. CCD
   The following lists the pixels of the CCD sensors that can be used with the HD49815TF. For other pixel numbers, contact our sales dept.
   512 (H) × 492 (V) NTSC
   512 (H) × 582 (V) PAL
   682 (H) × 492 (V) NTSC
   681 (H) × 582 (V) PAL
2. CDS/AGC + 10-bit ADC
   The HD49323AF-01 (manufactured by Renesas) is recommended as an optimal CDS/AGC + 10-bit ADC IC for the HD49815TF. Since the HD49323AF-01 provides a correlated double sampling circuit that realizes high S/N and an automatic gain control (AGC) circuit that implements programmable control of 0 dB to 34.7 dB, it enables a high-image-quality camera system when used in conjunction with the HD49815TF.
3. 8-bit single-chip microcomputer
   The 8-bit single-chip microcomputer controls the system. It receives the image detection data that the HD49815TF is gathering and implements automatic iris control (AE), automatic white balance control (AWB), and automatic focus control (AF).
   When setting the power on, this microcomputer implements the initial setting to the state data of the HD49815TF. For details on the state data, see “Renesas Camera DSP (HD49815TF) State Data”.

## Built-in Functions

1. Input line memory block

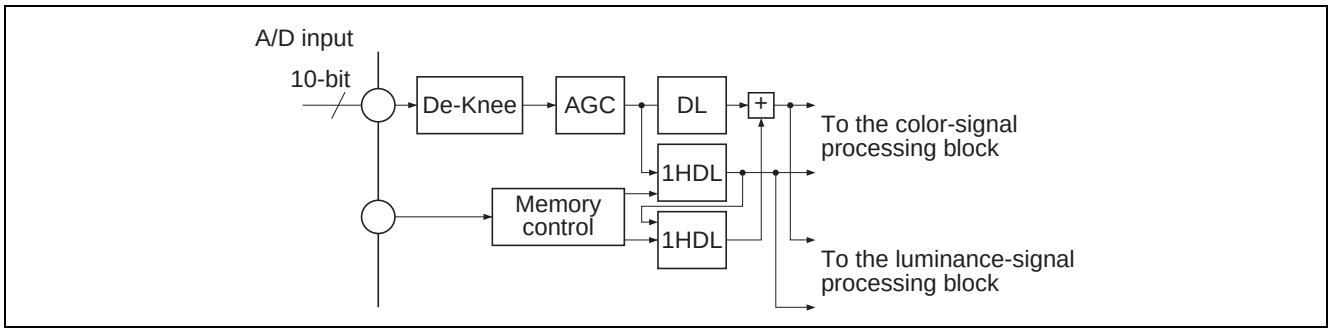



**Figure 3 Input Line Memory Block**

a. De-knee function
When the CDS/AGC IC at the pre-stage or the external circuit uses the knee circuit to expand the dynamic range of the signal, the de-knee (inverse knee) circuit returns the signal converted by the knee circuit to the original state.
The de-knee point can be set in State Data SP_A0 [1]. The gain of the high-luminance block is 1/2.

b. AGC function
A digital AGC circuit is provided. The AGC gain can be set in State Data SP_A0 [2] from 1 to 16 times.

c. 1H delay line (1HDL) function
This circuit obtains horizontal efficient pixels of the CCD output signal. The number of efficient pixels is set in State Data SP_A0 [9, 10] and TM_A0 [14] MCSET.

2. Color-signal processing block

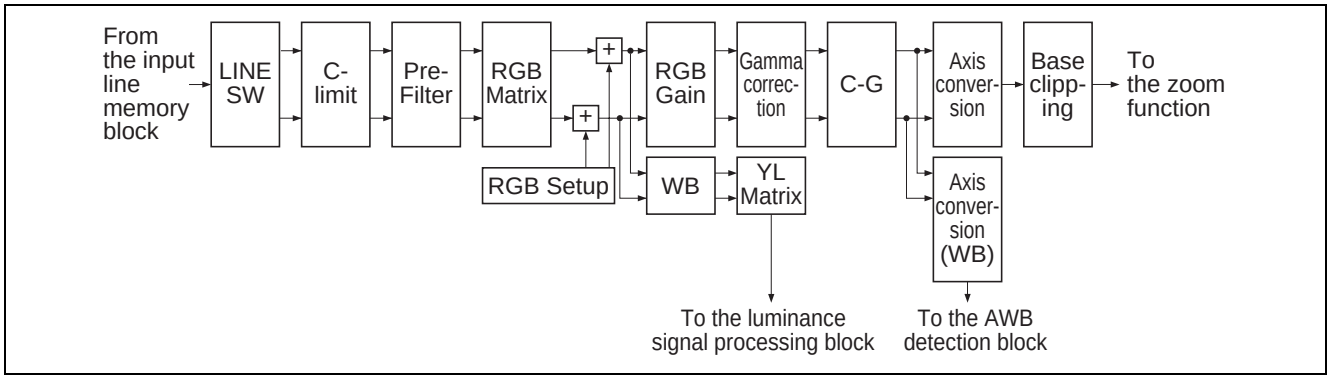



**Figure 4 Color-Signal Processing Block**

a. C-limit (complementary color clipping level) function
High clipping processing is performed on the complementary color signals independently. High clipping is set in State Data SP_A2 [0 to 3].
The complementary color signal indicates Gb: (G + Cy), Wr: (Ye + Mg), Wb: (Mg + Cy), and Gr: (G + Ye).

b. RGB-matrix block
The three primary colors (red, green, and blue) are acquired in the RGB matrix by multiplying arbitrary coefficients by the four complementary colors (Gb, Wr, Wb, and Gr) and taking the total of those results. The RGB matrix is designed to support the minimum color moire and to enable free color reproduction. Arbitrary coefficients are set in State Data SP_A2 [4 to 15]. The following shows the formula.

$$\begin{pmatrix} R \\ B \\ G \end{pmatrix} = \begin{pmatrix} KRa & KRb & KRc & KRd \\ KBa & KBb & KBc & KBd \\ KGa & KGb & KGc & KGd \end{pmatrix} \begin{pmatrix} Gb \\ Wr \\ Wb \\ Gr \end{pmatrix}$$

State Data SP_A2 [4 to 15]

c. RGB-setup block

The black level of the color signals is variable according to the coefficients of the RGB matrix. The value calculated by the formula below is subtracted from the color signal to correct the black level. The subtracted value can be set externally and is set in State Data SP_A3 [0 to 2].

$$\text{Formula} = -[48 \times \Sigma\,(\text{Matrix data}) \times 2^3]$$

d. RGB-gain block

The RGB gain value acquired in the AWB control is set in the RGB gain circuit to improve the white reproduction performance. As it is set prior to the gamma correction, it changes the gamma correction amount. The RGB gain can be set in State Data SP_A3 [3 to 5] from 1 to 256 times. (The G gain is set from 1 to 128 times.)

e. C gamma (γ) correction block

The C gamma correction circuit performs gamma processing on the RGB signal. It is set in State Data SP_A3 [6 to 9]. Four kinds of values can be set independently, according to the input-signal level, to acquire optimal gamma characteristics: the C gamma dark (to reduce the gain of the small signals for improving S/N), C gamma coefficient (to control the expansion of the gamma curve), C gamma knee (to decide the slope of the large signals), and C gamma limit (to perform high-clipping processing for the input signal of the C gamma circuit).

f. YL matrix block

The luminance level changes according to the color temperature of the imaged object. Set State Data SP_A5 [12, 13] for the luminance correction. To correct the luminance, create YL from the three primary colors (R, G, and B) and convert it to the luminance signal level. The YL matrix circuit creates the YL level from the RGB signal. The YL matrix is set in State Data SP_A3 [11 to 13].

g. The axis-conversion (C-Y matrix) block

The C-Y (color-difference) matrix takes R-G and B-G as its input signals, and creates the R-Y and B-Y color-difference signals by setting coefficients for those inputs.

The axis-conversion (C-Y matrix) circuits are set in State Data SP_A8 [0 to 5].

h. Base-clipping block

Since base clipping is performed on the color-difference signals, the base-clipping circuit has the characteristics of clipping the sections near axes on a vector scope.

This circuit is set in State Data SP_A8 [8].

3. Luminance-signal-processing block

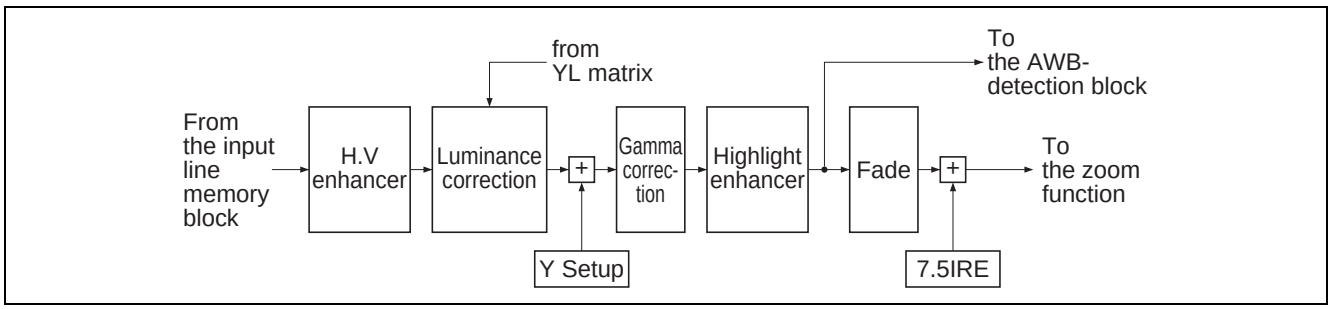



**Figure 5 Luminance-Signal-Processing Block**

a. H-enhancer function

The H-enhancer circuit allows the core level, the enhancer gain, and the noise coefficient to be set independently to acquire optimal characteristics.

This circuit is set in State Data SP_A4 [4 to 7].

b. V-enhancer function

The V-enhancer circuit allows the enhancer coefficient to be set and can control the gain for only those signal components that exceed the set core level.

This circuit is set in State Data SP_A4 [8 to 10].

c. Luminance correction

The ratio of the red and blue levels changes according to the color temperature of the imaged object. For example, if a red object is imaged at a low color temperature, the luminance level increases and the object appears to have a lower chrominance. Therefore, the luminance correction circuit performs luminance-correction processing to implement color depth reproduction.

The luminance-correction circuit is set in State Data SP_A5 [12, 13].

d. Y setup
Since the OB clamp processes the signal, the black level of the 10-bit signal input to the HD49815TF is fixed to 48/1024. The Y-setup circuit subtracts 48 at the black level. However, when 48 at the black level differs due to the noise mixed in the analog signal, the Y-setup circuit subtracts that value.
The Y-setup circuit is set in State Data SP_A5 [6].

e. Gamma correction
The gamma-correction circuit implements the gamma-correction processing for the separated Y signal. Four kinds of values can be set independently, according to the input-signal level, to acquire optimal gamma characteristics: the gamma input limit, the gamma knee coefficient, the gamma coefficient, and the gamma black clipping.
The gamma correction circuit is set in State Data SP_A5 [1 to 4].

f. Highlight enhancer
For input-Y signal levels in excess of 100 IRE, the highlight enhancer implements highlight enhancer processing.
This circuit is set in State Data SP_A5 [0, 5, and 14].

g. Fade
The fade circuit amplifies the luminance signal by a factor of 0 to 1.
This circuit is set in State Data SP_A5 [9].

4. Zoom, encode block, TG, SSG, and AWB and AE detection blocks

a. Zoom processing
The Y, R-Y, and B-Y signals completed the color-signal processing and the luminance-signal processing can be electronically zoomed by a factor of 1 to 256.
After clipping CCD signals for V direction, zoom circuit clips these signals for H direction, and expand these signals for H and V directions.
The zooming times and the read starting position for the V and H directions are set in State Data TM_A2 [3, 4, 5, 6, 8, and 9] and ZM_A0 to 6.

b. Encode block
This circuit encodes the signals completed the color-signal processing, the luminance-signal processing, and the zoom processing as the NTSC/PAL TV-monitor method.
A DAC that converts the digital signal to an analog signal is provided. The DAC has two channels: one for R-Y signals and one for B-Y signals.

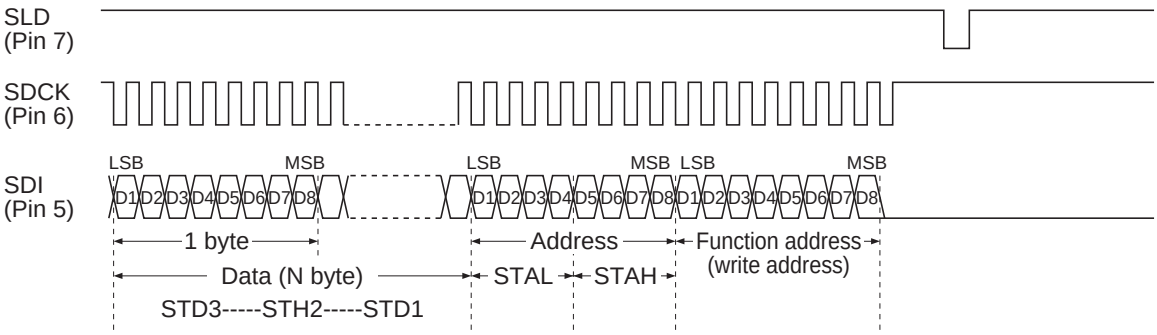
c. TG and SSG
The TG generates the signals required to drive the CCD sensor (H1, H2, RG, SG1/2, and the V transfer pulse), and the CDS/AGC control signals (SP1 and SP2).
In addition, the SSG generates the signals to synchronize with the TV monitor (the Sync signal).
The drive timing of the generated signals differs according to the manufacturer and the specifications of the CCD sensor. Setting the state data enables setting of any timing.
The state data of TG and SSG can be set in TM_A0, A1, A2, A3, and A8.

d. AWB- and AE-detection blocks
The HD49815TF provides automatic white-balance (AWB) and automatic-iris (AE) detection circuits that are indispensable for a camera.
The AWB-detection block takes the R-Y and B-Y color-difference signals completed the color-signal processing, and converts to the R-B and MG-G axes. The converted signals are sent to circuits for the white detection to obtain white signal components only, and the white-color difference value is detected. The 8-bit single-chip microcomputer acquires this detection data, and controls the R and B gains to produce the true white.
The State Data of the AWB detection is AWB_A0 and A8.

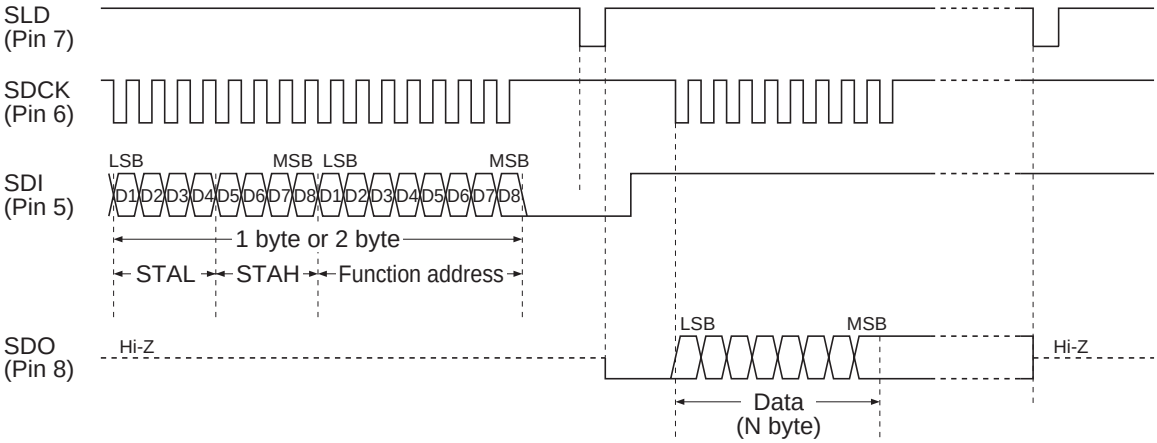
The AE-detection block divides the CCD output signal converted to digital by the 10-bit ADC to six arbitrary areas, and performs integration processing. This function enables detection of the lighting level of the image signal.
The 8-bit single-chip microcomputer acquires this detection data, and controls the accumulation amount (the shutter) of the CCD sensor or the iris motor of the lens to maintain the proper lighting.
The State Data of the AF detection is AE_A0 to A7 and A8.

## Microcomputer Interface Specifications

• Write format




• Read format




Notes: 1. Synchronous serial transfer (The microcomputer serial port can be used.)
2. Transfer frequency: 3.58 MHz or lower
3. Data and address are handled in a byte unit.
4. The clock and load pulse are used in common for read/write.

## Data Transfer Specification

For data transfer between the HD49815TF and the microcomputer, two types (N and E for write, and R1 and R2 for read) are available. The following table shows the relationship between the function block and the transfer specifications. On the next page, the details of the transfer specifications are described.

| Function Block | Transfer Mode | Transfer Specifications *1 | Related Address |
|---|---|---|---|
| Signal processing | W | N | SP_A0, 2 to 5, 7 to 10, 15 |
| TM | W | N | TM_A3, 15 |
| | | E | TM_A0 to 2, 8, 10 to 12 |
| | R | R1 | TMR_A0 |
| Iris | W | N | AE_A0 to 7 |
| | R | R2 | AE_A8 |
| White balance | W | N | AWB_A0 |
| | R | R1 | AWB_A8 |
| AF | W | N | AF_A0 to 3 |
| | R | R1 | AF_A8 to 13 |
| ZOOM | W | N | ZM_A0 to 6 |

Note: 1. Transfer specifications

Type N : Normal transfer from the microcomputer to the DSP

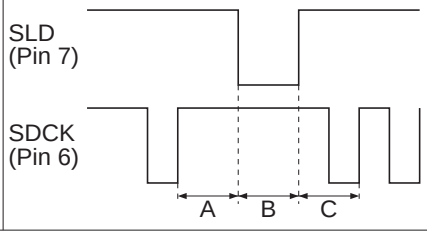
Type E : Transfer using the set pulse (synchronous with VD) or the reset signal (used as a synchronous pulse in the DSP) sent from the microcomputer to the RS latch in the DSP

Note: This cannot be set during the standby mode.

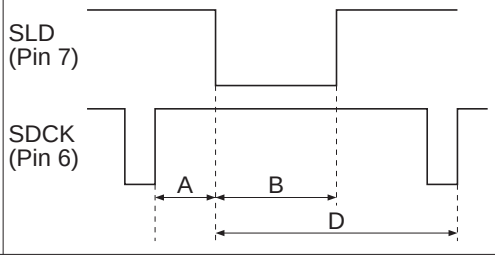
Type R1 : Data transfer (1) from the DSP to microcomputer

Type R2 : Data transfer (2) from the DSP to microcomputer

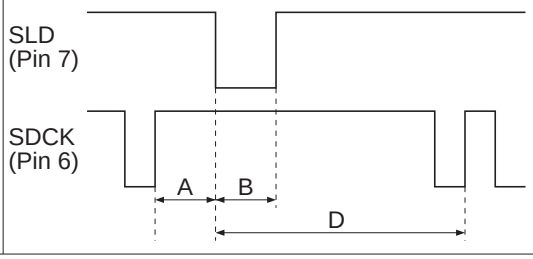
- Type N

| Transfer specification | Pulse Timing | Conditions |
|---|---|---|
| N |  | A = 100 ns or more<br>B = 100 ns or more<br>C = 100 ns or more |

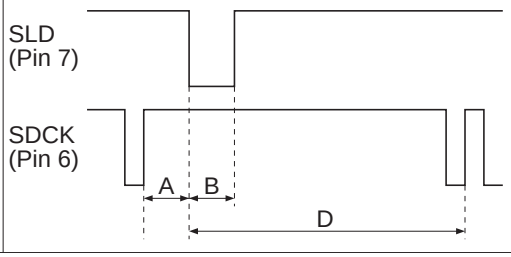
- Type E

| Transfer specification | Pulse Timing | | | Conditions | |
|---|---|---|---|---|---|
| | | | | 270,000 pixels | 410,000 pixels |
| E |  | A | 0.5 / fs + 100 ns or more | 150 ns or more | 135 ns or more |
| | | B | 2 / fs + 100 ns or more | 300 ns or more | 240 ns or more |
| | | D | 5.5 / fs + 100 ns or more | 650 ns or more | 485 ns or more |
| | | fs | Sensor clock | 100 ns | 70 ns |

- Type R1

| Transfer specification | Pulse Timing | Conditions |
|---|---|---|
| R1 |  | A = 100 ns or more<br>B = 100 ns or more<br>D = 400 ns or more<br><br>Do not read the white balance data and the AF read data within the 1H period from the start of the V blanking. |

- Type R2

| Transfer specification | Pulse Timing | | | Conditions | |
|---|---|---|---|---|---|
| | | | | A = 100 ns or more<br>B = 100 ns or more | |
| | | | | 270,000 pixels | 410,000 pixels |
| R2 |  | D | {1 / fs × (32 + 5) + 400 ns} or more | 4.1 µs or more | 2.99 µs or more |
| | | fs | Sensor clock | 100 ns | 70 ns |

Note: 2 to 9. Function addresses

The following table shows the function addresses for each function block (during state data transfer) and the data to be transferred from the microcomputer.

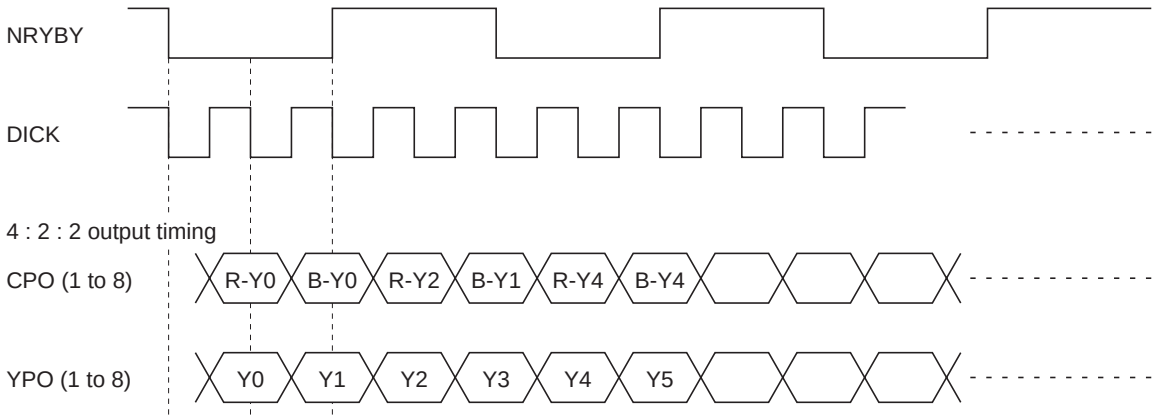
**Table 2 Function Addresses for each Function Block and State Data**

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | List of Data Transferred | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 Signal processing (Setting example) | | Function Address | | | | | | | | STAH | | | | STAL | | | | STD1 | | | | | | | | STD2 | | | | | | | | This example is related to SP-A0[9]. |
| | | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | — | — | — | — | — | — | — | D9 | |
| 3 TM write (Setting example) | | Function Address | | | | | | | | STAH | | | | STAL | | | | STD1 | | | | | | | | STD2 | | | | | | | | This example is related to TM-A0 [14]. |
| | | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | * | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | — | — | — | — | — | — | — | — | |
| 4 TM read | | Function Address | | | | | | | | Data read for automatic phase adjustment for SP1, SP2, and RG | | | | | | | | | | | | | | | | | | | | | | | | |
| | | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | |
| AE | 5 W | Function Address | | | | | ADATA | | | STAH | | | | STAL | | | | STD1 | | | | | | | | STD2 | | | | | | | | This example is related to the IRIS peak detection area. |
| | | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | |
| | | 0 | 0 | 0 | 1 | 0 | * | * | * | * | * | * | * | * | * | * | * | — | — | — | — | * | * | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | — | — | — | — | — | D3 | D2 | D1 | — | — | — | — | — | — | — | — | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | 5 W | Function Address | | | | | ADATA | | | STAH | | | | STAL | | | | STD1 | | | | | | | | STD2 | | | | | | | | This example is related to the window H count 3. |
| | | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | * | * | * | * | * | * | * | — | — | — | * | * | * | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | — | — | — | D5 | D4 | D3 | D2 | D1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | 6 R | Function Address | | | | | | | | STAH | | | | STAL | | | | Read area setting by STAL (4 bits) | | | | | | | | | | | | | | | | |
| | | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | | | | | | | | | | | | | | | | |
| | | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | — | — | — | — | * | * | * | * | | | | | | | | | | | | | | | | | |
| AWB | 7 W | Function Address | | | | | ADATA | | | STAH | | | | STAL | | | | STD1 | | | | | | | | STD2 | | | | | | | | This example is related to the offset R-B. |
| | | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | |
| | | 0 | 0 | 1 | 0 | 0 | — | — | — | — | — | — | * | * | * | * | * | * | * | * | * | * | * | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | 0 | 0 | 1 | 0 | 0 | — | — | — | — | — | — | 0 | 0 | 0 | 0 | 1 | — | — | D6 | D5 | D4 | D3 | D2 | D1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | 7 W | Function Address | | | | | ADATA | | | STAH | | | | STAL | | | | STD1 | | | | | | | | Window setting for white balance WB detection axis phase setting | | | | | | | | This example is related to the V count 2. |
| | | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | | | | | | | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | * | * | * | * | * | — | — | — | * | * | * | * | * | | | | | | | | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | | | | | | | | |
| | 8 R | Function Address | | | | | | | | White balance read | | | | | | | | | | | | | | | | | | | | | | | | |
| | | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | |
| AF | 9 W | Function Address | | | | | ADATA | | | STAH | | | | STAL | | | | HPF bandwidth selection<br>Base-clip quantity setting, etc. | | | | | | | | | | | | | | | | This example is related to the HRF bandwidth selection. |
| | | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | | | | | | | | | | | | | | | | |
| | | 0 | 0 | 1 | 1 | 0 | * | * | * | * | * | * | * | * | * | * | * | | | | | | | | | | | | | | | | | |
| | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | — | — | — | — | D4 | D3 | D2 | D1 | | | | | | | | | | | | | | | | | |
| | 9 W | Function Address | | | | | ADATA | | | STAH | | | | STAL | | | | STD1 | | | | | | | | Setting for integration and display gate | | | | | | | | This example is related to the differential gate of V-end. |
| | | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | | | | | | | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | * | * | * | * | * | * | * | * | * | * | * | | | | | | | | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | | | | | | | | |
| | 10 R | Function Address | | | | | | | | Vf fetch address (read_cycle) | | | | | | | | | | | | | | | | | | | | | | | | |
| | | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0 | 0 | 1 | 1 | 1 | * | * | * | | | | | | | | | | | | | | | | | | | | | | | | | |
| ZOOM | W | Header | | | | | | | | Data 1 | | | | | | | | Data 2 | | | | | | | | Data 3 | | | | | | | | |
| | | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | 0 | 1 | 1 | 0 | * | * | * | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | Data 4 | | | | | | | | Data 5 | | | | | | | | Data 6 | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

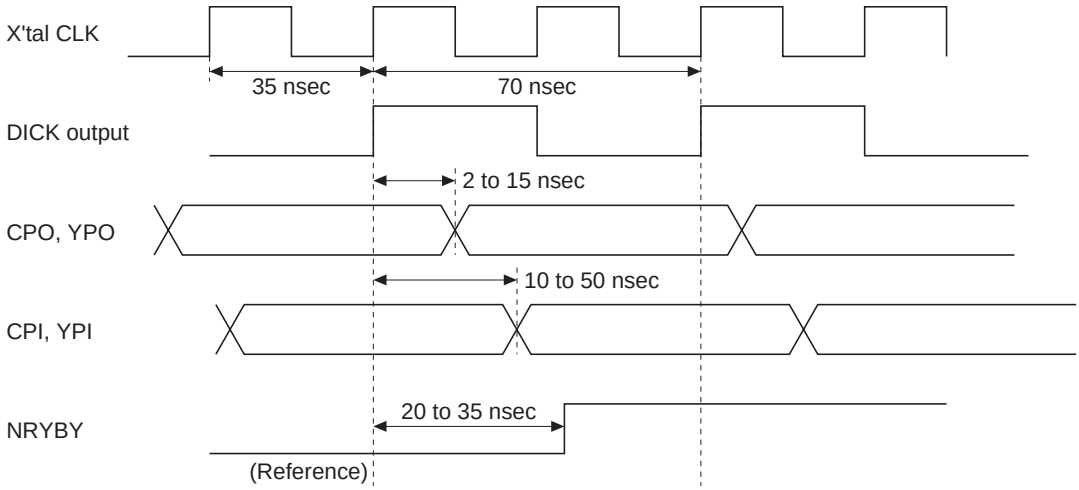
Note: For the ZOOM, the transfer of in total of seven bytes is required for the header and data 1 to 6.

## Digital Interface Timing

• The output specification and timing of the digital interface output (Y, R-Y, B-Y)



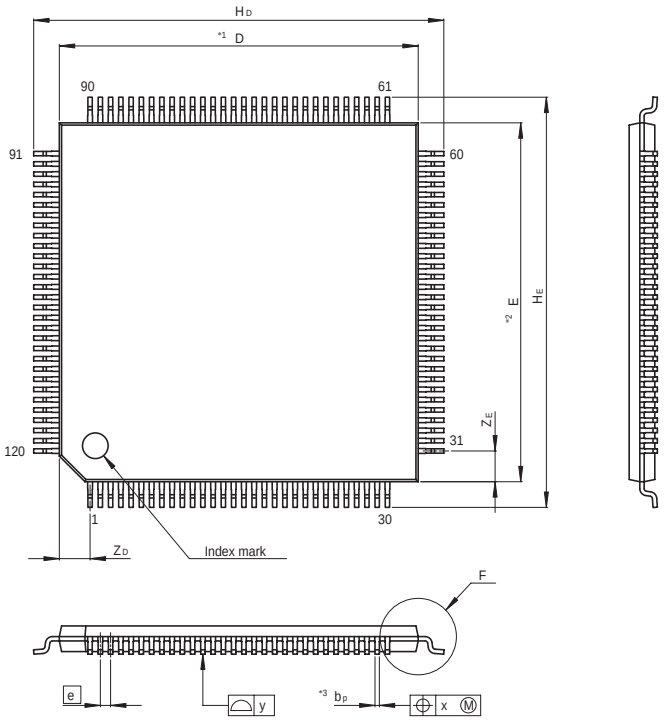

• Detailed specifications of digital interface timing



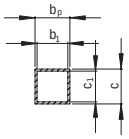

NRYBY : R-Y/B-Y determination pulse
DICK : Clock dedicated to the digital interface (The clock generated from the external X'tal.)
CPO, YPO : Digital interface output terminal
CPI, YPI : Digital interface input terminal

# Package Dimensions

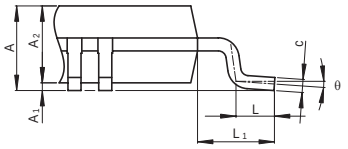
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TQFP120-14x14-0.40 | PTQP0120LA-A | TFP-120/TFP-120V | 0.5g |




NOTE)
1. DIMENSIONS"*1"AND"*2"
   DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT
   INCLUDE TRIM OFFSET.




Terminal cross section




Detail F

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | —— | 14 | —— |
| E | —— | 14 | —— |
| $A_2$ | —— | 1.00 | —— |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | —— | —— | 1.20 |
| $A_1$ | 0.00 | 0.10 | 0.20 |
| $b_p$ | 0.12 | 0.17 | 0.22 |
| $b_1$ | —— | 0.15 | —— |
| c | 0.12 | 0.17 | 0.22 |
| $c_1$ | —— | 0.15 | —— |
| θ | 0° | —— | 8° |
| e | —— | 0.4 | —— |
| x | —— | —— | 0.07 |
| y | —— | —— | 0.10 |
| $Z_D$ | —— | 1.20 | —— |
| $Z_E$ | —— | 1.20 | —— |
| L | 0.4 | 0.5 | 0.6 |
| $L_1$ | —— | 1.0 | —— |

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan



## RENESAS SALES OFFICES

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**Renesas Technology America, Inc.**
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited**
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

**Renesas Technology Hong Kong Ltd.**
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

**Renesas Technology Taiwan Co., Ltd.**
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology (Shanghai) Co., Ltd.**
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

**Renesas Technology Singapore Pte. Ltd.**
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001



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