OC-35 Series

3.2X5X1.2mm / 3.3V / SMD / HCMOS/TTL Oscillator

Lead-Free
RoHS Compliant

C A L I B E R
Electronics Inc.

PART NUMBERING GUIDE

Environmental/Mechanical Specifications on page F5

OC-35A- 100 48 A T - 30.000MHz

Package
OC-35 = 3.3Vdc
OC-35A = 1.8Vdc
OC-35B = 2.5Vdc

Inclusive Stability
100= +/-100ppm, 50= +/-50ppm, 30= +/-30ppm, 25= +/-25ppm, 20= +/-20ppm **(25,20 = 0°C-70°C Only)**

Operating Temperature Range
Blank = -10°C to 70°C, 27 = -20°C to 70°C, 48 = -40°C to 85°C

Output Symmetry
Blank = 40/60%, A = 45/55%

Pin One Connection
T = Tri State Enable High

ELECTRICAL SPECIFICATIONS

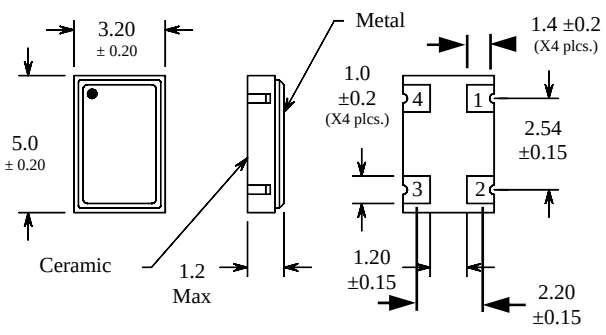
Revision: 2003-B

Frequency Range		1.544MHz to 156.250MHz / **32.768kHz @ 3.3V)**
Operating Temperature Range		-10°C to 70°C / -20°C to 70°C / -40°C to 85°C
Storage Temperature Range		-55°C to 125°C
Supply Voltage		A=1.8Vdc / B=2.5Vdc / BLANK=3.3Vdc ±10%
Input Current	1.544MHz to 36.000MHz **and 32.768kHz** 36,001MHz to 70.000MHz 70.001MHz to 125.000MHz	2mA Maximum 5mA Maximum 7mA Maximum
Frequency Tolerance / Stability	Inclusive of Operating Temperature Range, Supply Voltage and Load	±100ppm, ±50ppm, ±30ppm, ±25ppm, ±20ppm **(±50ppm for 32.768kHz only)**
Output Voltage Logic High (Voh)	w/HCMOS or TTL Load	90% of Vdd Min. / Ioh=-8mA
Output Voltage Logic Low (Vol)	wHCMOS or TTL Load	10% of Vdd Max. / Iol=8mA
Rise / Fall Time	10% to 90% of Waveform w/HCMOS Load; 0.4Vdc to 2.4V w/TTL Load / 6nSec Max.	
Duty Cycle	@1.4Vdc w/TTL Load; @50% w/HCMOS Load @1.4Vdc w/TTL Load or w/HCMOS Load	50 ±10% (Standard) 50±5% (Optional)
Load Drive Capability	</= 70.000MHz >70.000MHz </=70.000MHz (Optional)	10LSTTL Load or 15pF HCMOS Load 15pF HCMOS Load 10TTL Load or 50pF HCMOS Load
Pin 1 Tristate Input Voltage	No Connection VIH VIL	Enables Output 2.2Vdc Minimum to Enable Output +0.8Vdc Maximum to Disable Output
Aging (@ 25°C)		±5ppm / year Maximum
Start Up Time		10mSeconds Maximum
Absolute Clock Jitter		±250pSeconds Maximum
One Sigma Clock Jitter		±50pSeconds Maximum

MECHANICAL DIMENSIONS

All Dimensions in mm.

Application Note:
A 0.01uF bypass capacitor should be placed between Vdd (pin 4) and GND (pin 2) to minimize power supply line noise.



Marking Guide

Line 1: A, B or Blank - Frequency
Line 2: CEI YM

A = Voltage designator
CEI = Caliber Electronics Inc.
YM = Date Code (Year / Month)

Pin 1: Tri-State
Pin 2: Case Ground
Pin 3: Output
Pin 4: Supply Voltage