# CAT1320, CAT1321

## Supervisory Circuits with I²C Serial 32K CMOS EEPROM

## FEATURES

- **Precision power supply voltage monitor**
  - **— 5V, 3.3V and 3V systems**
    - **+5.0V (+/- 5%, +/- 10%)**
    - **+3.3V (+/- 5%, +/- 10%)**
    - **+3.0V (+/- 10%)**
- **Active low reset, CAT1320**
- **Active high reset, CAT1321**
- **Valid reset guaranteed at $V_{CC}$=1V**
- **400kHz I²C bus**
- **3.0V to 5.5V operation**
- **Low power CMOS technology**
- **64-Byte page write buffer**
- **1,000,000 Program/Erase cycles**
- **100 year data retention**
- **8-pin DIP, SOIC, TSSOP and TDFN packages**
- **Industrial temperature range**

## DESCRIPTION

The CAT1320 and CAT1321 are complete memory and supervisory solutions for microcontroller-based systems. A 32kbit serial EEPROM memory and a system power supervisor with brown-out protection are integrated together in low power CMOS technology. Memory interface is via a 400kHz I²C bus.

The CAT1320 provides a precision $V_{CC}$ sense circuit and drives an open drain output, $\overline{\text{RESET}}$ low whenever $V_{CC}$ falls below the reset threshold voltage.

The CAT1321 provides a precision VCC sense circuit that drives an open drain output, RESET high whenever $V_{CC}$ falls below the reset threshold voltage.

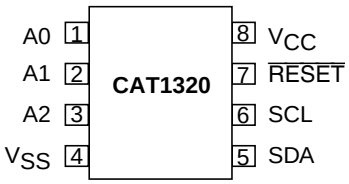
The power supply monitor and reset circuit protect memory and system controllers during power up/down and against brownout conditions. Five reset threshold voltages support 5V, 3.3V and 3V systems. If power supply voltages are out of tolerance reset signals become active, preventing the system microcontroller, ASIC or peripherals from operating. Reset signals become inactive typically 200 ms after the supply voltage exceeds the reset threshold level. With both active high and low reset options, interface to microcontrollers and other ICs is simple. In addition, the $\overline{\text{RESET}}$ (CAT1320) pin can be used as an input for push-button manual reset capability.

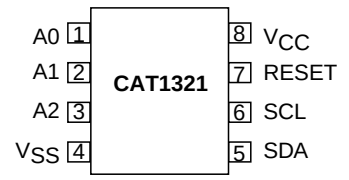
The CAT1320/21 memory features a 64-byte page. In addition, hardware data protection is provided by a $V_{CC}$ sense circuit that prevents writes to memory whenever $V_{CC}$ falls below the reset threshold or until $V_{CC}$ reaches the reset threshold during power up.

Available packages include an 8-pin DIP, SOIC, TSSOP and 4.9 x 3mm TDFN.

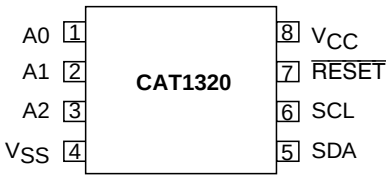
## PIN CONFIGURATION

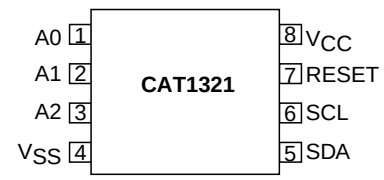
**PDIP (L) SOIC (W)**



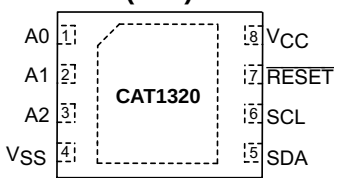



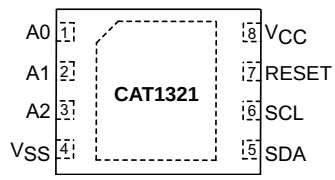

**TSSOP (Y)**




**TDFN PACKAGE: 4.9MM X 3MM (ZD2)**



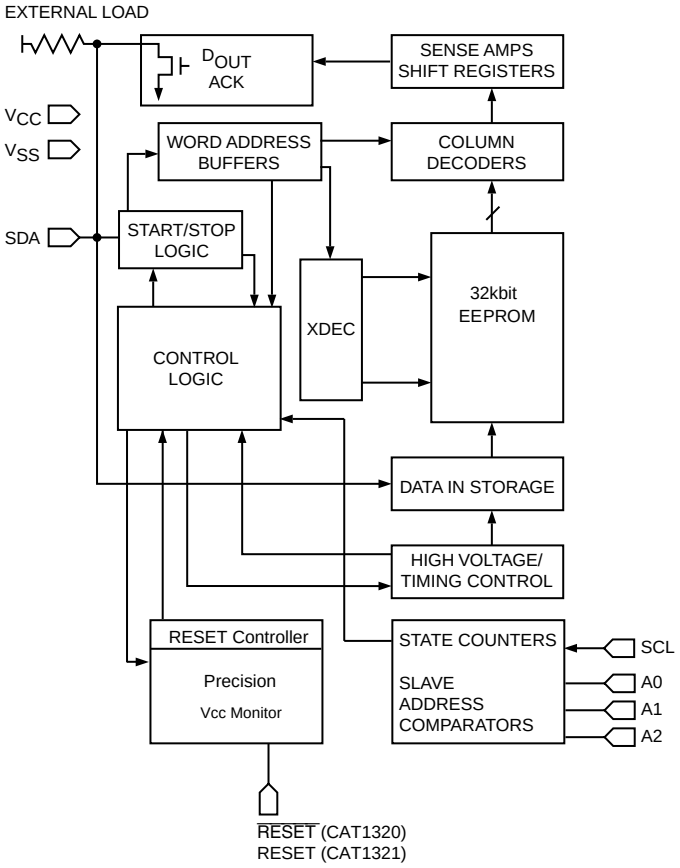








Doc. No. MD-3014, Rev. B.

## BLOCK DIAGRAM — CAT1320, CAT1321




## Threshold Voltage Options

| Part Dash Number | Minimum Threshold | Maximum Threshold |
|---|---|---|
| -45 | 4.50 | 4.75 |
| -42 | 4.25 | 4.50 |
| -30 | 3.00 | 3.15 |
| -28 | 2.85 | 3.00 |
| -25 | 2.55 | 2.70 |

### OPERATING TEMPERATURE RANGE

| | |
|---|---|
| Industrial | -40˚C to 85˚C |

### PIN FUNCTIONS

| Pin Name | Function |
|---|---|
| $\overline{\text{RESET}}$ | Active Low Reset Input/Output (CAT1320) |
| $V_{SS}$ | Ground |
| SDA | Serial Data/Address |
| SCL | Clock Input |
| RESET | Active High Reset Output (CAT1321) |
| $V_{CC}$ | Power Supply |

## PIN DESCRIPTION

**RESET/$\overline{\text{RESET}}$:** RESET OUTPUTS
These are open-drain pins and $\overline{\text{RESET}}$ can also be used as a manual reset trigger input. By forcing a reset condition on the pin the device will initiate and maintain a reset condition. The RESET pin must be connected through a pull-down resistor and the $\overline{\text{RESET}}$ pin must be connected through a pull-up resistor.

**SDA:** SERIAL DATA ADDRESS
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

**SCL:** SERIAL CLOCK
Serial clock input.

**A0, A1, A2:** DEVICE ADDRESS INPUTS
When hardwired, up to eight CAT1320/21 devices may be addressed on a single bus system (refer to Device Addressing). When the pins are left unconnected, the default values are zeros.

## ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -40°C to +85°C

Storage Temperature ..... -65°C to +105°C

Voltage on any Pin with Respect to Ground(1) ..... -0.5V to +$V_{CC}$ +2.0V

$V_{CC}$ with Respect to Ground ..... -0.5V to +7.0V

Package Power Dissipation Capability ($T_A$ = 25°C) ..... 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(1) ..... 100 mA

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

Note:
(1) Output shorted for no more than one second. No more than one output shorted at a time.

## D.C. OPERATING CHARACTERISTICS

$V_{CC}$ = +3.0V to +5.5V and over the recommended temperature conditions unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = GND to Vcc | -2 | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{IN}$ = GND to Vcc | -10 | | 10 | µA |
| $I_{CC1}$ | Power Supply Current (Write) | $f_{SCL}$ = 400kHz<br>$V_{CC}$ = 5.5V | | | 3 | mA |
| $I_{CC2}$ | Power Supply Current (Read) | $f_{SCL}$ = 400kHz<br>$V_{CC}$ = 5.5V | | | 1 | mA |
| $I_{SB}$ | Standby Current | Vcc = 5.5V,<br>$V_{IN}$ = GND or Vcc | | | 40 | µA |
| $V_{IL}$[2] | Input Low Voltage | | -0.5 | | 0.3 x Vcc | V |
| $V_{IH}$[2] | Input High Voltage | | 0.7 x Vcc | | Vcc + 0.5 | V |
| $V_{OL}$ | Output Low Voltage (SDA, $\overline{\text{RESET}}$) | $I_{OL}$ = 3mA<br>$V_{CC}$ = 3.0V | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage (RESET) | $I_{OH}$ = -0.4mA<br>$V_{CC}$ = 3.0V | Vcc - 0.75 | | | V |
| $V_{TH}$ | Reset Threshold | CAT132x-45 ($V_{CC}$ = 5V) | 4.50 | | 4.75 | V |
| | | CAT132x-42 ($V_{CC}$ = 5V) | 4.25 | | 4.50 | |
| | | CAT132x-30 ($V_{CC}$ = 3.3V) | 3.00 | | 3.15 | |
| | | CAT132x-28 ($V_{CC}$ = 3.3V) | 2.85 | | 3.00 | |
| | | CAT132x-25 ($V_{CC}$ = 3V) | 2.55 | | 2.70 | |
| $V_{RVALID}$[1] | Reset Output Valid $V_{CC}$ Voltage | | 1.00 | | | V |
| $V_{RT}$[1] | Reset Threshold Hysteresis | | 15 | | | mV |

Notes:
1. This parameter is tested initially and after a design or process change that affects the parameter. Not 100% tested.
2. $V_{IL}$ min and $V_{IH}$ max are reference values only and are not tested.

## CAPACITANCE

$T_A$ = 25°C, f = 1.0 MHz, $V_{CC}$ = 5V

| Symbol | Test | Test Conditions | Max | Units |
|---|---|---|---|---|
| $C_{OUT}$(1) | Output Capacitance | $V_{OUT}$ = 0V | 8 | pF |
| $C_{IN}$(1) | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |

## A.C. CHARACTERISTICS

$V_{CC}$ = 3.0V to 5.5V and over the recommended temperature conditions, unless otherwise specified.

### Memory Read & Write Cycle[2]

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{SCL}$ | Clock Frequency | | 400 | kHz |
| $t_{SP}$[1] | Input Filter Spike Suppression (SDA, SCL) | | 100 | ns |
| $t_{LOW}$ | Clock Low Period | 1.3 | | µs |
| $t_{HIGH}$ | Clock High Period | 0.6 | | µs |
| $t_R$[1] | SDA and SCL Rise Time | | 300 | ns |
| $t_F$[1] | SDA and SCL Fall Time | | 300 | ns |
| $t_{HD;STA}$ | Start Condition Hold Time | 0.6 | | µs |
| $t_{SU;STA}$ | Start Condition Setup Time (for a Repeated Start) | 0.6 | | µs |
| $t_{HD;DAT}$ | Data Input Hold Time | 0 | | ns |
| $t_{SU;DAT}$ | Data Input Setup Time | 100 | | ns |
| $t_{SU;STO}$ | Stop Condition Setup Time | 0.6 | | µs |
| $t_{AA}$ | SCL Low to Data Out Valid | | 900 | ns |
| $t_{DH}$ | Data Out Hold Time | 50 | | ns |
| $t_{BUF}$[1] | Time the Bus must be Free Before a New Transmission Can Start | 1.3 | | µs |
| $t_{WC}$[3] | Write Cycle Time (Byte or Page) | | 5 | ms |

Notes:
1. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
2. Test Conditions according to “AC Test Conditions” table.
3. The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high and the device does not respond to its slave address.

## RESET CIRCUIT A.C. CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PURST}$ | Reset Timeout | Note 2 | 130 | 200 | 270 | ms |
| $t_{RPD}$ | $V_{TH}$ to RESET output Delay | Note 3 | | | 5 | µs |
| $t_{GLITCH}$ | $V_{CC}$ Glitch Reject Pulse Width | Note 4, 5 | | | 30 | ns |
| MR Glitch | Manual Reset Glitch Immunity | Note 5 | | | 100 | ns |
| $t_{MRW}$ | MR Pulse Width | Note 5 | 5 | | | µs |

## POWER-UP TIMING[5,6]

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PUR}$ | Power-Up to Read Operation | | | | 270 | ms |
| $t_{PUW}$ | Power-Up to Write Operation | | | | 270 | ms |

Notes:
1. Test Conditions according to “AC Test Conditions” table.
2. Power-up, Input Reference Voltage $V_{CC} = V_{TH}$, Reset Output Reference Voltage and Load according to “AC Test Conditions” Table
3. Power-Down, Input Reference Voltage $V_{CC} = V_{TH}$, Reset Output Reference Voltage and Load according to “AC Test Conditions” Table
4. $V_{CC}$ Glitch Reference Voltage = $V_{THmin}$; Based on characterization data
5. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
6. $t_{PUR}$ and $t_{PUW}$ are the delays required from the time $V_{CC}$ is stable until the specified memory operation can be initiated.

### AC TEST CONDITIONS

| | |
|---|---|
| Input pulse voltages | $0.2V_{CC}$ to $0.8V_{CC}$ |
| Input rise and fall times | 10 ns |
| Input reference voltages | $0.3V_{CC}$, $0.7V_{CC}$ |
| Output reference voltages | $0.5V_{CC}$ |
| Output Load | Current Source: $I_{OL}$ = 3mA; $C_L$ = 100pF |

## RELIABILITY CHARACTERISTICS

| Symbol | Parameter | Reference Test Method | Min | Max | Units |
|---|---|---|---|---|---|
| $N_{END}$(1) | Endurance | MIL-STD-883, Test Method 1033 | 1,000,000 | | Cycles/Byte |
| $T_{DR}$(1) | Data Retention | MIL-STD-883, Test Method 1008 | 100 | | Years |
| $V_{ZAP}$(1) | ESD Susceptibility | MIL-STD-883, Test Method 3015 | 2000 | | Volts |
| $I_{LTH}$(1)(2) | Latch-Up | JEDEC Standard 17 | 100 | | mA |

Notes:
1. This parameter is tested initially and after a design or process change that affects the parameter. Not 100% tested.
2. Latch-up protection is provided for stresses up to 100mA on input and output pins from -1V to $V_{CC}$ + 1V.

## DEVICE OPERATION

### Reset Controller Description

The CAT1320/21 precision Reset controllers ensure correct system operation during brownout and power up/down conditions. They are configured with open-drain $\overline{\text{RESET}}$/RESET outputs.

During power-up, the $\overline{\text{RESET}}$/RESET output remains active until $V_{CC}$ reaches the $V_{TH}$ threshold and will continue driving the outputs for approximately 200ms ($t_{PURST}$) after reaching $V_{TH}$. After the $t_{PURST}$ timeout interval, the device will cease to drive the reset output. At this point the reset output will be pulled up or down by their respective pull up/down resistors.

During power-down, the $\overline{\text{RESET}}$/RESET output will be active when $V_{CC}$ falls below $V_{TH}$. The $\overline{\text{RESET}}$/RESET output will be valid so long as $V_{CC}$ is >1.0V ($V_{RVALID}$). The device is designed to ignore the fast negative going $V_{CC}$ transient pulses (glitches).

Reset output timing is shown in Figure 1.

### Manual Reset Operation

The $\overline{\text{RESET}}$ pin can operate as reset output and manual reset input. The input is edge triggered; that is, the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a high to low transition.

When $\overline{\text{RESET}}$ I/O is driven to the active state, the 200 msec timer will begin to time the reset interval. If external reset is shorter than 200 ms, Reset outputs will remain active at least 200 ms.

Glitches shorter than 100 ns on $\overline{\text{RESET}}$ input will not generate a reset pulse.

### Hardware Data Protection

The CAT1320/21 family has been designed to solve many of the data corruption issues that have long been associated with serial EEPROMs. Data corruption occurs when incorrect data is stored in a memory location which is assumed to hold correct data.

Whenever the device is in a Reset condition, the embedded EEPROM is disabled for all operations, including write operations. If the Reset output is active, in progress communications to the EEPROM are aborted and no new communications are allowed. In this condition an internal write cycle to the memory can not be started, but an in progress internal non-volatile memory write cycle can not be aborted. An internal write cycle initiated before the Reset condition can be successfully finished if there is enough time (5ms) before VCC reaches the minimum value of 2V.

**Figure 1. RESET/$\overline{\text{RESET}}$ Output Timing**

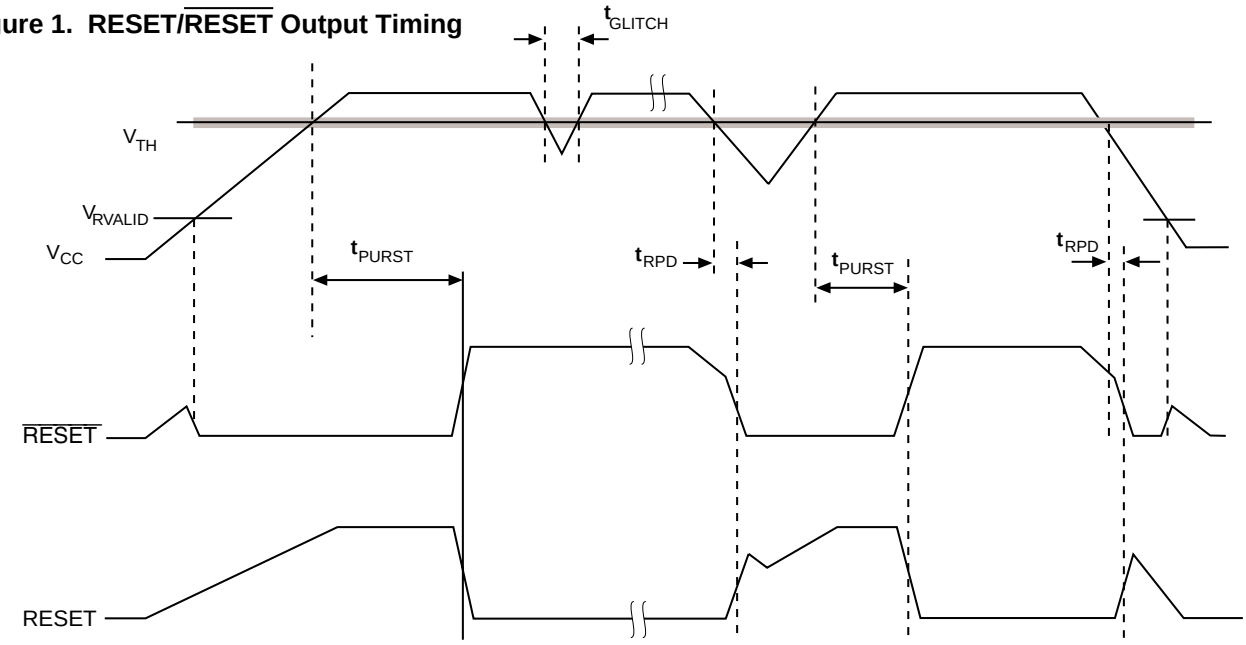


**Figure 2. $\overline{\text{RESET}}$ as Manual Reset Input Operation and Timing**

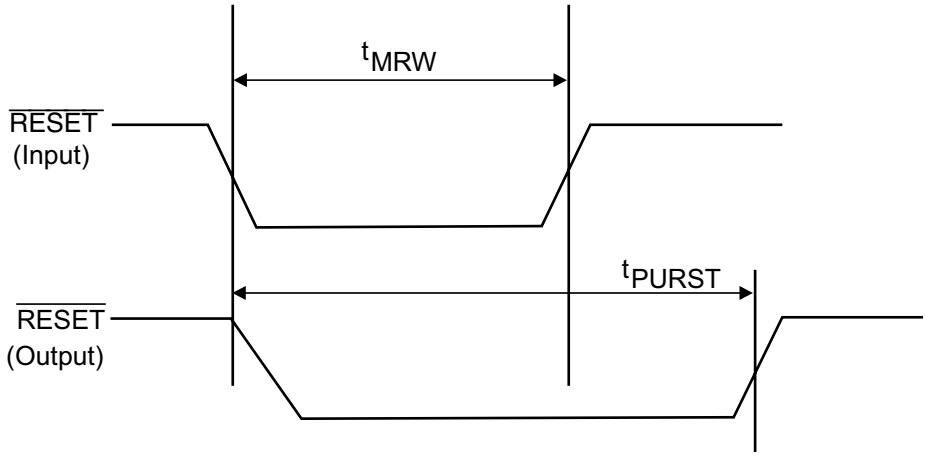
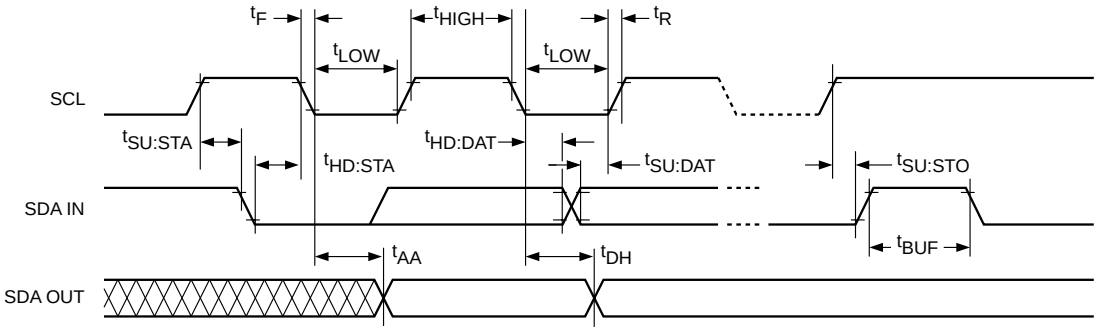



**Figure 3. Bus Timing**



## EMBEDDED EEPROM OPERATION

The CAT1320 and CAT1321 feature a 32kbit embedded serial EEPROM that supports the $I^2C$ Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

### $I^2C$ Bus Protocol

The features of the $I^2C$ bus protocol are defined as follows:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

### START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT1320/21 monitors the SDA and SCL lines and will not respond until this condition is met.

### STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

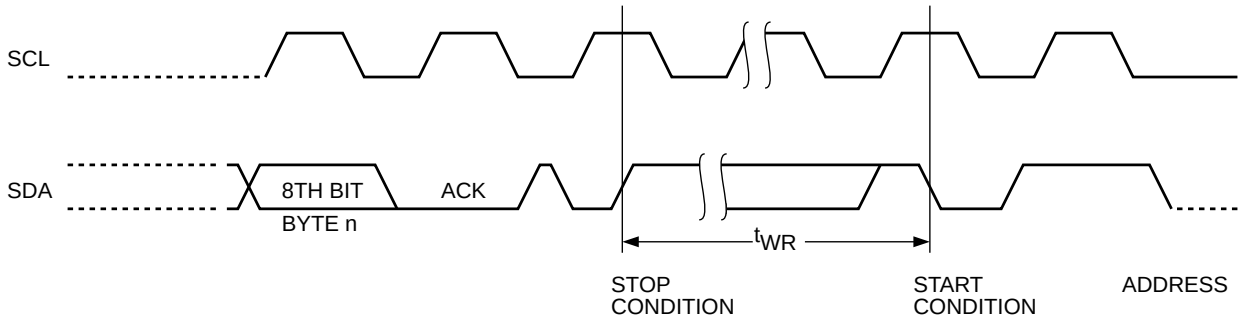
## DEVICE ADDRESSING

The Master begins a transmission by sending a START condition. The Master sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are programmable in metal and the default is 1010.

The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT1320/21 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT1320/21 then performs a Read or Write operation depending on the R/$\overline{W}$ bit.

**Figure 4. Write Cycle Timing**



## ACKNOWLEDGE

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT1320/21 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT1320/21 begins a READ mode it transmits 8 bits of data, releases the SDA line and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT1320/21 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

## WRITE OPERATIONS

### Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends two 8-bit address bytes that are to be written into the address pointers of the device. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT1320/21 acknowledges once more and the Master generates the STOP condition. At this time, the device begins an internal programming cycle to non-volatile memory. While the cycle is in progress, the device will not respond to any request from the Master device.

**Figure 5. Start/Stop Timing**

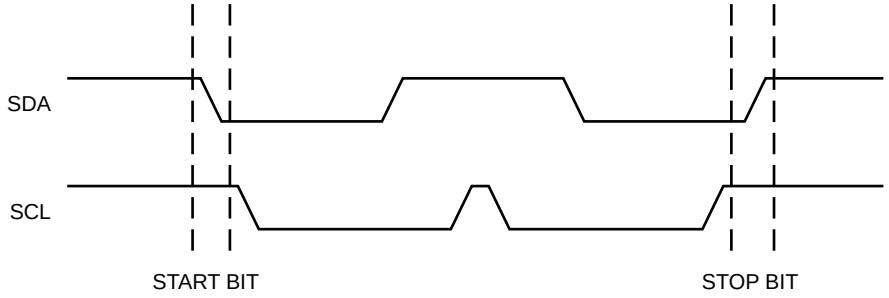



**Figure 6. Acknowledge Timing**

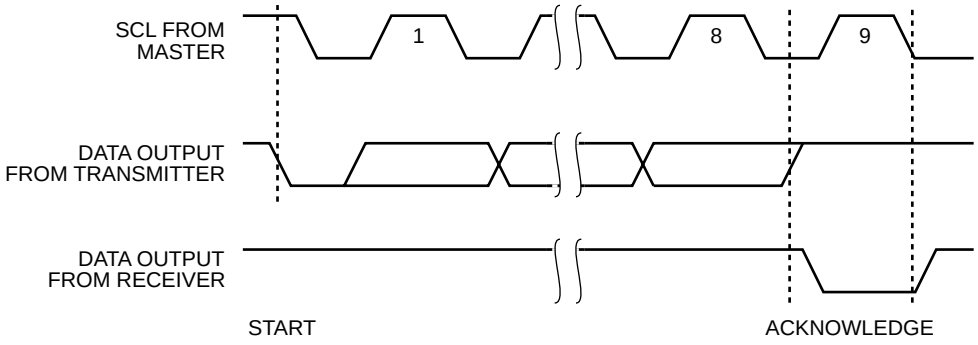



**Figure 7. Slave Address Bits**

Default Configuration

| 1 | 0 | 1 | 0 | A2 | A1 | A0 | R/$\overline{W}$ |
|---|---|---|---|---|---|---|---|

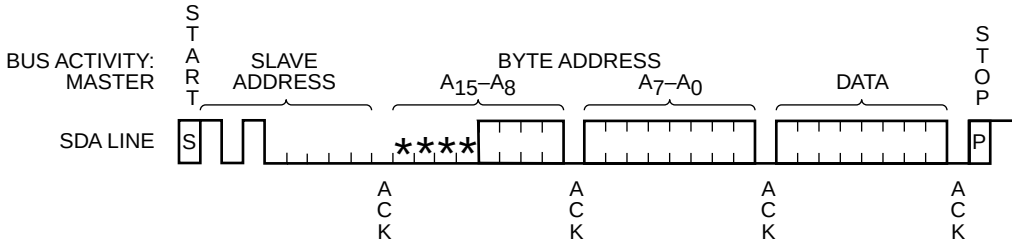
### Page Write

The CAT1320/21 writes up to 64 bytes of data in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to additional 63 bytes. After each byte has been transmitted, the CAT1320/21 will respond with an acknowledge and internally increment the lower order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 64 bytes before sending the STOP condition, the address counter 'wraps around,' and previously transmitted data will be overwritten.

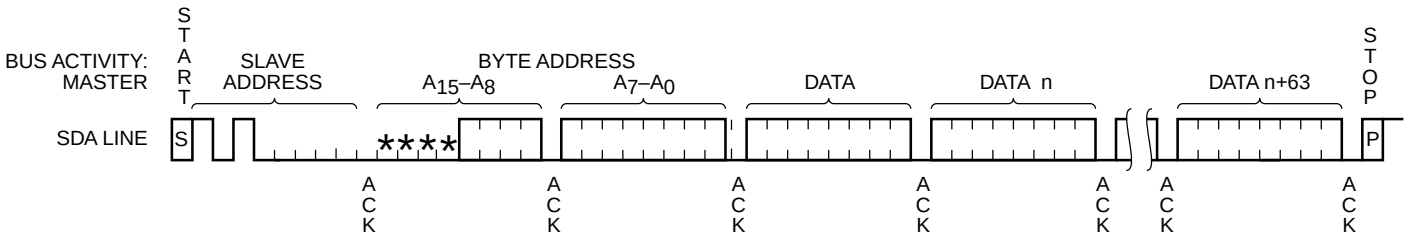
When all 64 bytes are received, and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the CAT1320/21 in a single write cycle.

**Figure 8. Byte Write Timing**




*=Don't Care Bit

**Figure 9. Page Write Timing**




*=Don't Care Bit

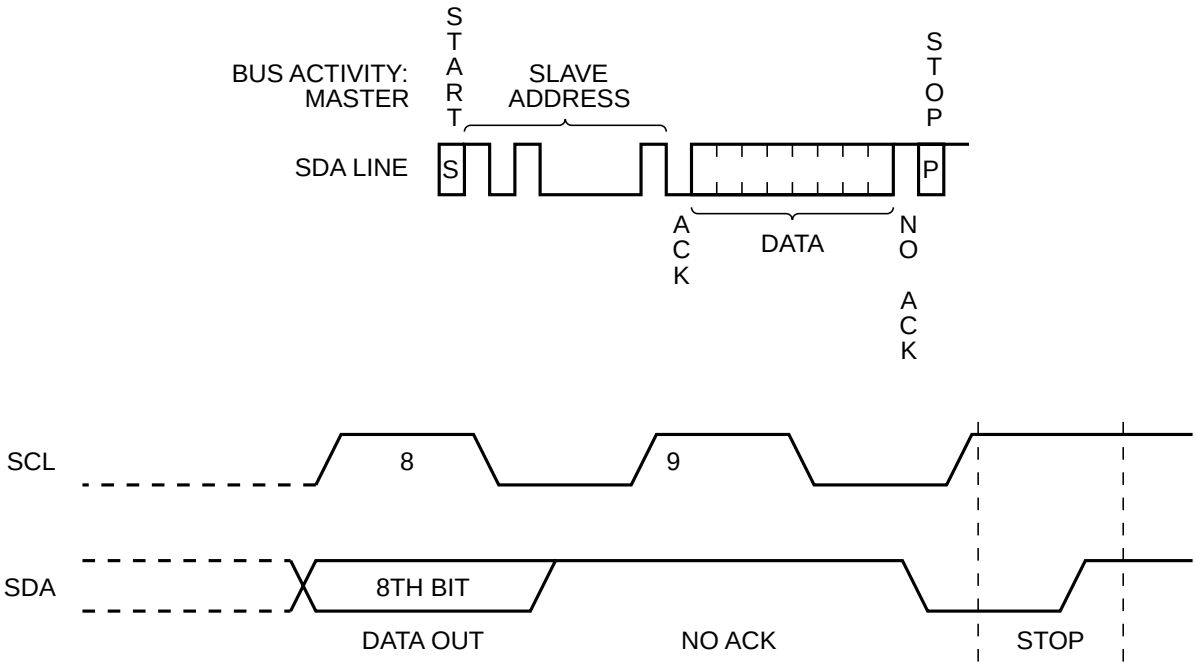
### Acknowledge Polling

Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write opration, the CAT1320/21 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the device is still busy with the write operation, no ACK will be returned. If a write operation has completed, an ACK will be returned and the host can then proceed with the next read or write operation.

### Read Operations

The READ operation for the CAT1320/21 is initiated in the same manner as the write operation with one exception, that R/$\overline{W}$ bit is set to one. Three different READ operations are possible: Immediate/Current Address READ, Selective/Random READ and Sequential READ.

**Figure 10. Immediate Address Read Timing**



### Immediate/Current Address Read

The CAT1320 and CAT1321 address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. For all devices, N=E=4,095. The counter will wrap around to Zero and continue to clock out valid data. After the CAT1320 and CAT1321 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8-bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

### Selective/Random Read

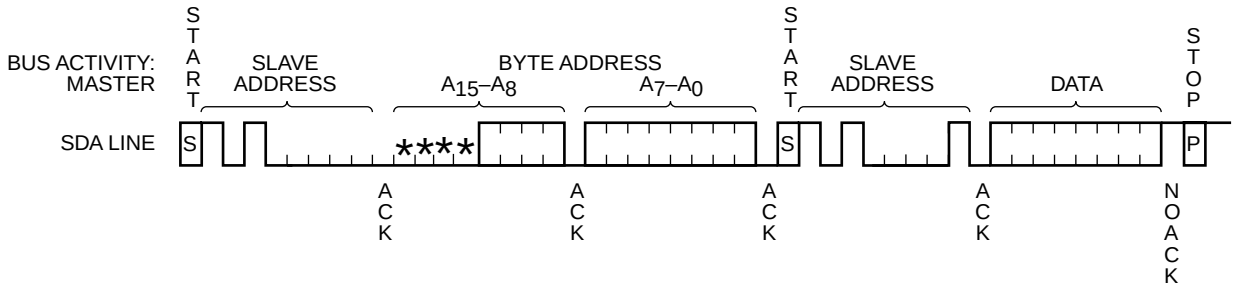
Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After the CAT1320 and CAT1321 acknowledges, the Master device sends the START condition and the slave address again, this time with the R/$\overline{W}$ bit set to one. The CAT1320 and CAT1321 then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

### Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT1320 and CAT1321 sends the inital 8-bit byte requested, the Master will responds with an acknowledge which tells the device it requires more data. The CAT1320 and CAT1321 will continue to output an 8-bit byte for each acknowledge, thus sending the STOP condition.

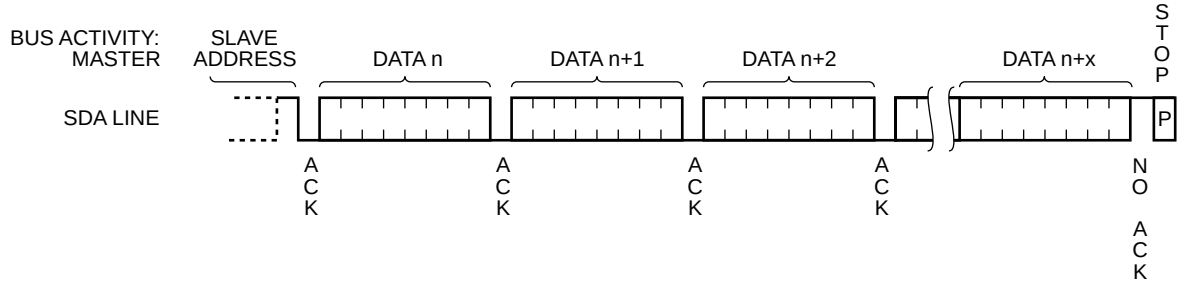
The data being transmitted from the CAT1320 and CAT1321 is sent sequentially with the data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT1320 and CAT1321 address bits so that the entire memory array can be read during one operation.

**Figure 11. Selective Read Timing**

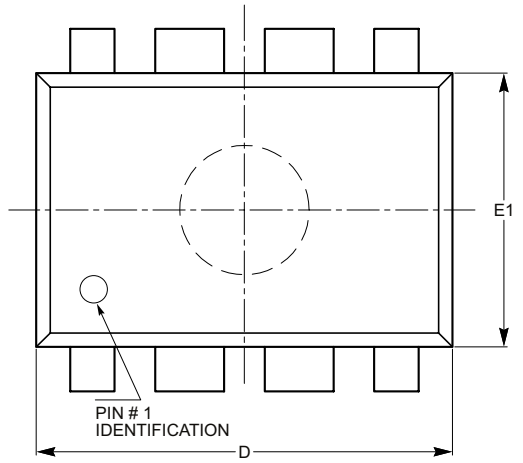



*=Don't Care Bit

**Figure 12. Sequential Read Timing**

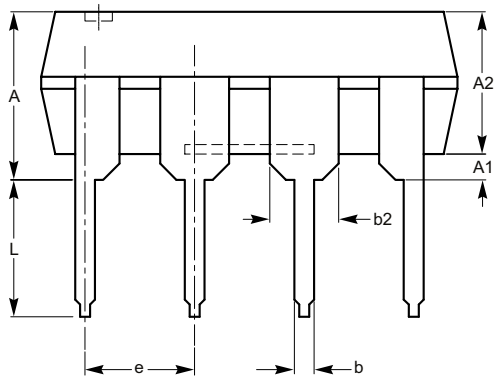


## PACKAGE OUTLINE DRAWINGS
## PDIP 8-Lead 300mils (L)

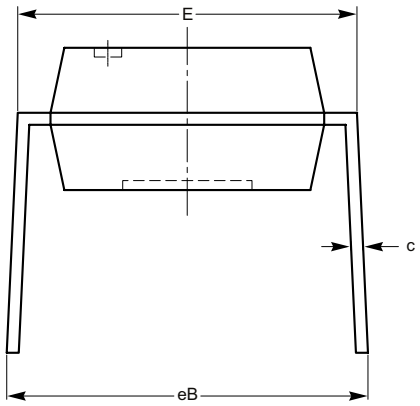



TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 5.33 |
| A1 | 0.38 | | |
| A2 | 2.92 | 3.30 | 4.95 |
| b | 0.36 | 0.46 | 0.56 |
| b2 | 1.14 | 1.52 | 1.78 |
| c | 0.20 | 0.25 | 0.36 |
| D | 9.02 | 9.27 | 10.16 |
| E | 7.62 | 7.87 | 8.25 |
| e | | 2.54 BSC | |
| E1 | 6.10 | 6.35 | 7.11 |
| eB | 7.87 | | 10.92 |
| L | 2.92 | 3.30 | 3.80 |




SIDE VIEW

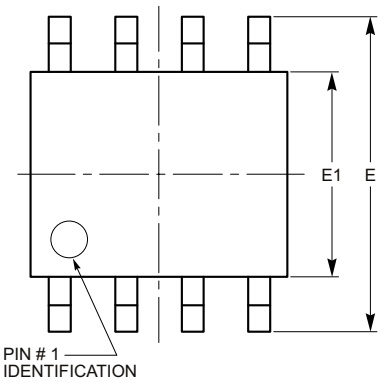



END VIEW

**For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.**

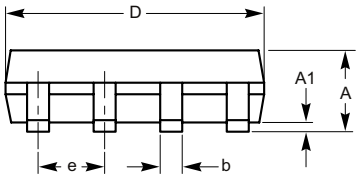
Notes:
1. Al dimensions are in millimeters. Angles in degrees.
2. Complies with JEDEC standard MS-001.

## SOIC 8-Lead 150mils (W)

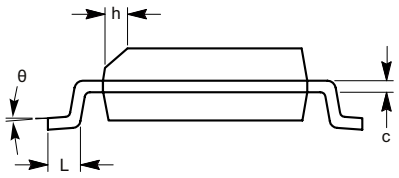



TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.35 | | 1.75 |
| A1 | 0.10 | | 0.25 |
| b | 0.33 | | 0.51 |
| c | 0.19 | | 0.25 |
| D | 4.80 | | 5.00 |
| E | 5.80 | | 6.20 |
| E1 | 3.80 | | 4.00 |
| e | 1.27 BSC | | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ | 0º | | 8º |




SIDE VIEW

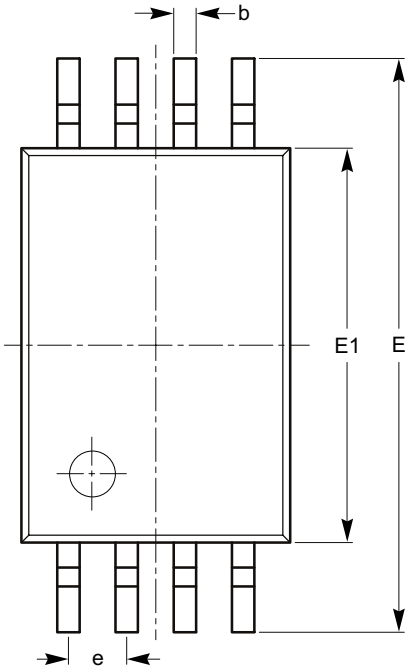



END VIEW

**For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.**

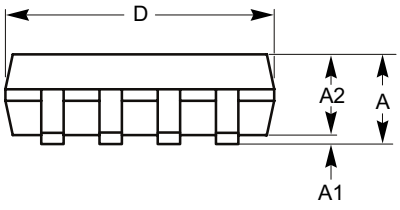
Notes:
1. Al dimensions are in millimeters. Angles in degrees.
2. Complies with JEDEC standard MS-012.

## TSSOP 8-Lead 4.4mm (Y)

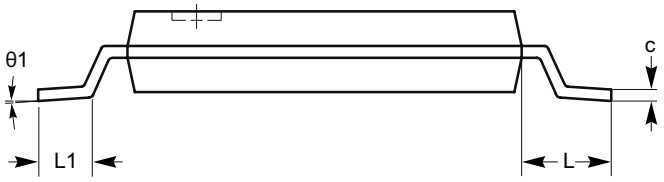



TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | 0.90 | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 2.90 | 3.00 | 3.10 |
| E | 6.30 | 6.40 | 6.50 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | 0.65 BSC | | |
| L | 1.00 REF | | |
| L1 | 0.50 | 0.60 | 0.75 |
| θ1 | 0° | | 8° |




SIDE VIEW

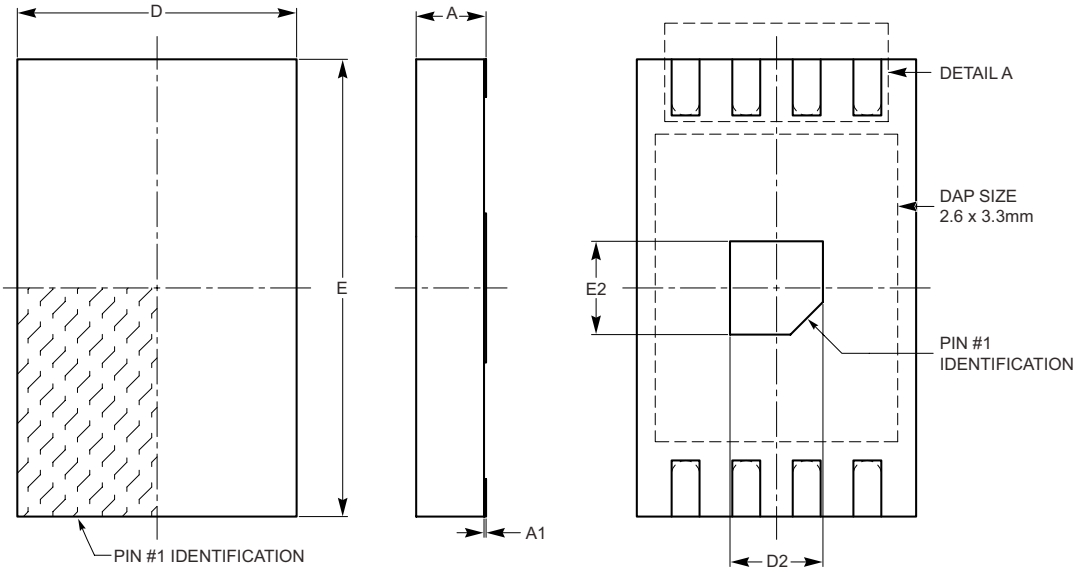



END VIEW

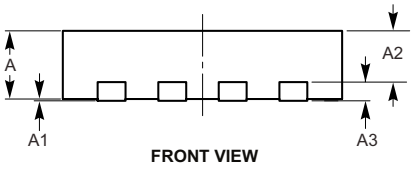
**For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.**

Notes:
1. Al dimensions are in millimeters. Angles in degrees.
2. Complies with JEDEC standard MS-153.

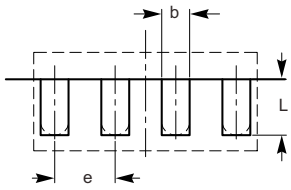
## TDFN-S-MSOP 8-Pad 3 x 4.9mm (ZD2)




| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | 0.45 | 0.55 | 0.65 |
| A3 | | 0.20 REF | |
| b | 0.25 | 0.30 | 0.35 |
| D | 2.90 | 3.00 | 3.10 |
| D2 | 0.90 | 1.00 | 1.10 |
| E | 4.80 | 4.90 | 5.00 |
| E2 | 0.90 | 1.00 | 1.10 |
| e | | 0.65 TYP | |
| L | 0.50 | 0.60 | 0.70 |




FRONT VIEW

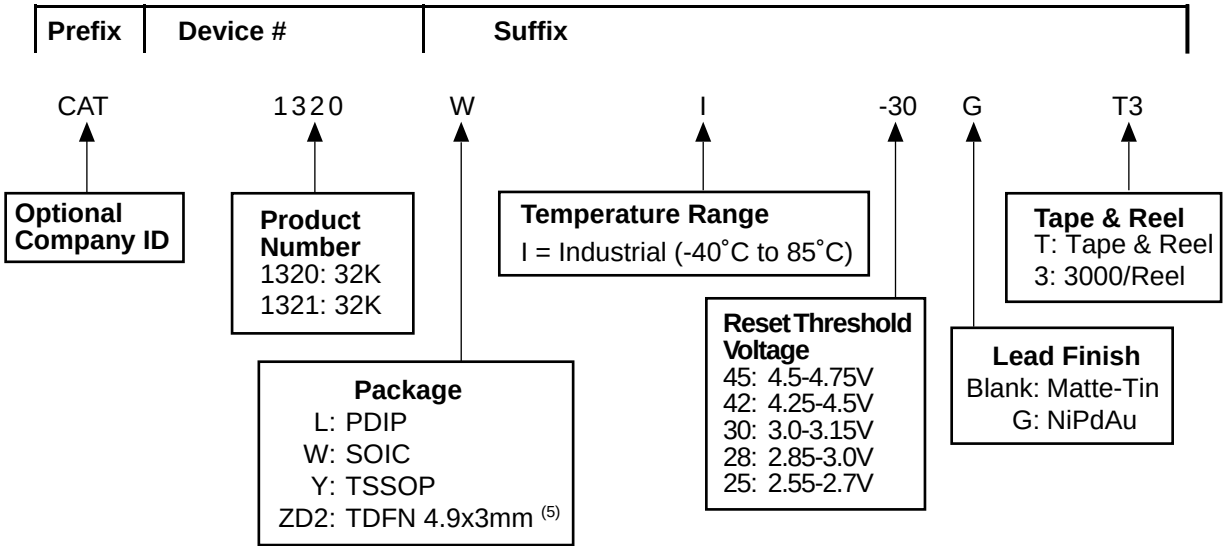



DETAIL A

**For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.**

Notes:
1. Al dimensions are in millimeters. Angles in degrees.
2. Complies with JEDEC standard MS-229.

## EXAMPLE OF ORDERING INFORMATION




## ORDERING PART NUMBERS

| | |
|---|---|
| CAT1320LI-45-G | CAT1321LI-45-G |
| CAT1320LI-42-G | CAT1321LI-42-G |
| CAT1320LI-30-G | CAT1321LI-30-G |
| CAT1320LI-28-G | CAT1321LI-28-G |
| CAT1320LI-25-G | CAT1321LI-25-G |
| CAT1320WI-45-GT3 | CAT1321WI-45-GT3 |
| CAT1320WI-42-GT3 | CAT1321WI-42-GT3 |
| CAT1320WI-30-GT3 | CAT1321WI-30-GT3 |
| CAT1320WI-28-GT3 | CAT1321WI-28-GT3 |
| CAT1320WI-25-GT3 | CAT1321WI-25-GT3 |
| CAT1320YI-45-GT3 | CAT1321YI-45-GT3 |
| CAT1320YI-42-GT3 | CAT1321YI-42-GT3 |
| CAT1320YI-30-GT3 | CAT1321YI-30-GT3 |
| CAT1320YI-28-GT3 | CAT1321YI-28-GT3 |
| CAT1320YI-25-GT3 | CAT1321YI-25-GT3 |
| CAT1320ZD2I-45-T3 | CAT1321ZD2I-45-T3 |
| CAT1320ZD2I-42-T3 | CAT1321ZD2I-42-T3 |
| CAT1320ZD2I-30-T3 | CAT1321ZD2I-30-T3 |
| CAT1320ZD2I-28-T3 | CAT1321ZD2I-28-T3 |
| CAT1320ZD2I-25-T3 | CAT1321ZD2I-25-T3 |

**Notes:**
(1) All packages are RoHS-compliant (Lead-free, Halogen-free).
(2) The standard lead finish is NiPdAu.
(3) The device used in the above example is a CAT1320WI-30-GT3 (SOIC, Industrial Temperature, 3.0 - 3.15V, NiPdAu, Tape & Reel).
(4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.
(5) TDFN not available in NiPdAu (-G) version.

## REVISION HISTORY

| Date | Rev. | Reason |
|---|---|---|
| 1/25/2005 | 00 | Initial issue |
| 01/21/08 | B | Update Package Outline Drawings<br>Update Example of Ordering Information<br>Add Ordering Part Number<br>Change document number from 25085 , Rev.00 |



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