



> 500 MHz, - 3 dB Bandwidth; Dual SPDT Analog Switch

DESCRIPTION

DG2721 is a low $R_{\rm on}$, high bandwidth analog switch configured in dual SPDT.

It achieves 5.7 Ω switch on resistance, greater than 500 MHz - 3 dB bandwidth with 5 pF load, and a channel to channel crosstalk and Isolation at - 49 dB.

Fabricated with high density sub micro CMOS process, the DG2721 provides low parasitic capacitance, handles bidirectional signal flow with minimized phase distortion. Guaranteed 1.3 V logic high threshold makes it possible to interface directly with low voltage MCUs.

The DG2721 is designed for a wide range of operating voltages from 2.7 V to 4.3 V that can be driven directly from one cell Li-ion battery. On-chip protection circuit protects again fault events when signals at "com" pins goes beyond V+.

Latch up current is greater than 300 mA, as per JESD78, and its ESD tolerance exceeds 8 kV.

Packaged in ultra small miniQFN-10 (1.4 mm x 1.8 mm x 0.55 mm), it is ideal for portable high speed mix signal switching application.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device termination. The miniQFN-10 package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free "-E4" suffix to the ordering part number. The nickel-palladium-gold device terminations meet all JEDEC standards for reflow and MSL rating.

As a further sign of Vishay Siliconix's commitment, the DG2721 is fully RoHS complaint.

FEATURES

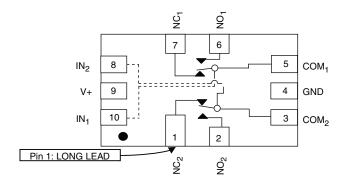
- Wide operation voltage range
- Low on-resistance, 5.7 Ω (typical at 3 V)
- Low capacitance, 5.6 pF (typical)
- 3 dB high bandwidth with 5 pF load:
 > 500 MHz (typical)
- · Low bit to bit skew: 40 pS (typical)
- · Low power consumption
- · Low logic threshold: V
- Power down protection: COM₁ and COM₂ pins can tolerate up to 5 V when V+ = 0 V
- Logic (IN₁ and IN₂) above V+ tolerance
- Latch-up current greater than 300 mA per JESD78
- 8 kV ESD protection (HBM)
- Lead (Pb)-free low profile miniQFN-10 (1.4 mm x 1.8 mm x 0.55 mm)

APPLICATIONS

- · Cellular phones
- · Portable media players
- PDA
- Digital camera
- GPS
- Notebook computer
- TV, monitor, and set top box
- Radio

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

miniQFN-10L



Top View

Device Marking: KX for DG2721 X = Date/Lot Traceability Code



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ORDERING INFORMATION			
Temp. Range	Package	Part Number	
- 40 °C to 85 °C	miniQFN-10	DG2721DN-T1-E4	

TRUTH TABLE			
IN ₁ (Pin 10)	IN ₂ (Pin 8)	Function	
Х	0	COM2 = NC ₂	
Х	1	COM2 = NO ₂	
0	X	COM1 = NC ₁	
1	Х	COM1 = NO ₁	

PIN DESCRIPTIONS			
Pin Name	Description		
IN ₁	Select Input COM ₁		
IN ₂	Select Input COM ₂		
NC _{1/2} , NO _{1/2} , COM _{1/2}	Data Channel		

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter		Limit	Unit	
Reference to GND	V+	- 0.3 to 5.0	V	
neierence to GIND	IN _X , NC _X , NO _X , COM _X ^a	- 0.3 to (V+ + 0.3)	v	
Current (Any Terminal except IN _X , NC _X , NO _X , COM _X)		30	mA	
Continuous Current (IN _X , NC _X , NO _X , COM _X)		± 250		
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 500		
Storage Temperature (D Suffix)		- 65 to 150	°C	
Power Dissipation (Packages) ^b miniQFN-10 ^c		208	mW	
ESD (Human Body Model) All Pins		4	kV	
I/O to GND		8	, KV	
Latch-up (Current Injection)		350	mA	

Notes:

a. Signals on IN_X , NC_X , NO_X , COM_X exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings. b. All leads welded or soldered to PC board.

c. Derate 2.6 mW/°C above 70 °C.





				Limits			
		Test Conditions			°C to 8		
Parameter	Symbol	Otherwise Unless Specified	Temp. ^a	Min.b	Typ.c	Max.b	Unit
Analog Switch			ı		1		
Analog Signal Range ^d	V_{ANALOG}	r _{DS(on)}	Full	0		V+	V
On-Resistance	$R_{DS(on)}$	V+ = 3.0 V, I _{COM} = 8 mA, V _{NC/NO} = 0.4 V	Room Full		5.7	7 9	Ω
On-Resistance Match ^d	ΔR _{ON}	V+ = 3.0 V, I _{COM} = 8 mA, V _{NC/NO} = 0.4 V	Room		0.35		
On-Resistance Resistance Flatness ^d	R _{ON} Flatness	V+ = 3.0 V, I _{COM} = 8 mA, V _{NC/NO} = 0.0 V, 1.0 V			2		
Switch Off Leakage Current	I _(off)	$V+ = 4.3 \text{ V}, V_{NC/NO} = 0.3 \text{ V}, 3.0 \text{ V},$ $V_{COM} = 3.0 \text{ V}, 0.3 \text{ V}$	Full	- 100		100	
Channel On Leakage Current	I _(on)	$V+ = 4.3 \text{ V}, V_{NC/NO} = 0.3 \text{ V}, 4.0 \text{ V}, $ $V_{COM} = 4.0 \text{ V}, 0.3 \text{ V}$	Full	- 200		200	nA
Digital Control							
loon at Malta and I limb	W	V+ = 3.0 V to 3.6 V	Full	1.3			
Input Voltage High	V_{INH}	V+ = 4.3 V	Full	1.7			٧
Input Voltage Low	V _{INL}	V+ = 3.0 V to 4.3 V	Full			0.5	
Input Capacitance	C _{IN}		Full		5.6		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	- 1		1	μΑ
Dynamic Characteristics							
Break-Before-Make Time ^{e, d}	t _{BBM}		Room Full		5		ns
Turn-On Time ^{e, d}	t _{ON}	$V+ = 3.0 \text{ V}, V_{COM} = 1.5 \text{ V}, R_L = 50 \Omega,$ $C_L = 35 \text{ pF}$	Room Full			30	
Turn-Off Time ^{e, d}	t _{OFF}		Room Full			25	
Charge Injection ^d	Q _{INJ}	$C_L = 1 \text{ nF}, R_{GEN} = 0 \Omega, V_{GEN} = 0 V$			0.5		рС
Off-Isolation ^d	OIRR	$V+ = 3.0 \text{ V to } 3.6 \text{ V}, R_L = 50 \Omega, C_L = 5 \text{ pF},$			- 30		dB
Crosstalk ^d	X _{TALK}	f = 240 MHz			- 49		
Bandwidth ^d	BW	V+ = 3.0 V to 3.6 V, R_L = 50 Ω, C_L = 5 pF, - 3 dB			> 500		MHz
	C _{NO(off)}	V+ = 3.3 V, f = 1 MHz			4		pF
Channel-Off Capacitance ^d	C _{NC(off)}		Room		4		
Channel-On Capacitance ^d	C _{COM(on)}	1			11		
Channel-to-Channel Skew ^d	t _{SK(O)}	V+ = 3.0 V to 3.6 V, R_L = 50 Ω, C_L = 5 pF]		50		
Skew Off Opposite Transitions of the Same Output ^d	t _{SK(p)}				20		ps
Total Jitter ^d	tJ	1			200		
Power Supply	-		ļ				
Power Supply Range	V+			2.6		4.3	V
Power Supply Current	I+	$V_{IN} = 0 \text{ V, or V+}$	Full		 		μΑ

Notes:

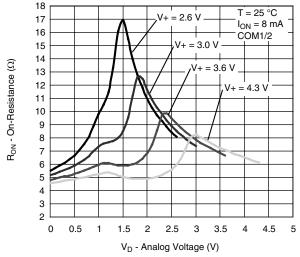
- a. Room = 25 $^{\circ}$ C, Full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, not subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Crosstalk measured between channels.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

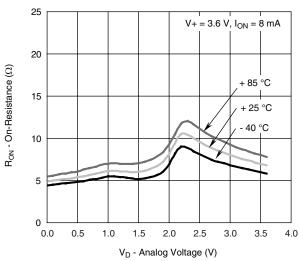
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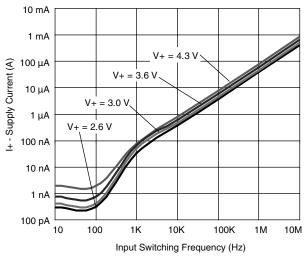
TYPICAL CHARACTERISTICS $T_A = 25$ °C, unless otherwise noted



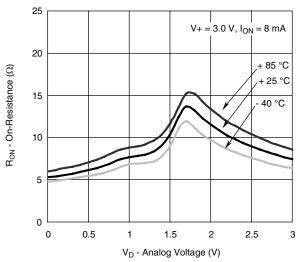
On-Resistance vs. $V_{\rm D}$ and Single Supply Voltage



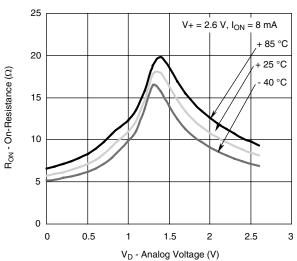
On-Resistance vs. Analog Voltage and Temperature



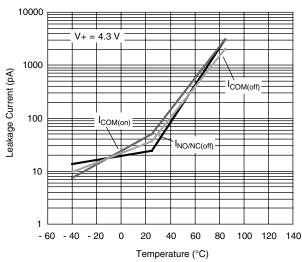
Supply Current vs. Input Switching Frequency



On-Resistance vs. Analog Voltage and Temperature



On-Resistance vs. Analog Voltage and Temperature

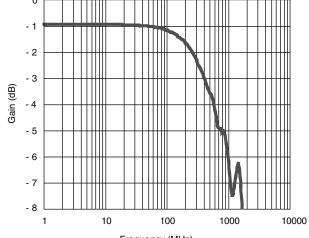


Leakage Current vs. Temperature





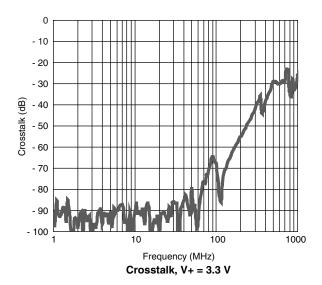
TYPICAL CHARACTERISTICS $T_A = 25$ °C, unless otherwise noted



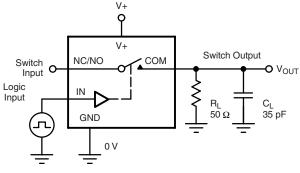
-10 -20 -30 -30 -40 -50 -70 -80 -90 -100 1 10 100 1000 Frequency (MHz)

0

OFF Isolation, V+ = 3.3 V



TEST CIRCUITS



Logic Input $V_{INL} = \begin{array}{c} V_{INH} & t_r < 5 \text{ ns} \\ V_{INL} & t_f < 5 \text{ ns} \\ V_{INL} & 0.9 \times V_{OUT} \\ \end{array}$ Switch Output $0 \text{ V} = \begin{array}{c} 0.9 \times V_{OUT} \\ 0.9 \times V_{OUT} \\ \end{array}$

C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$

Logic "1" = Switch On Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

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TEST CIRCUITS

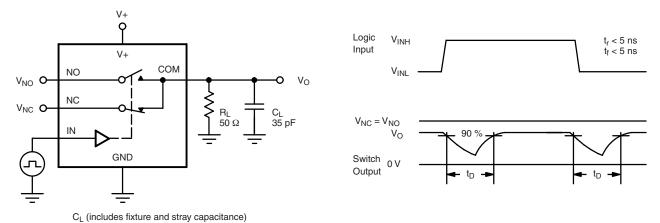


Figure 2. Break-Before-Make Interval

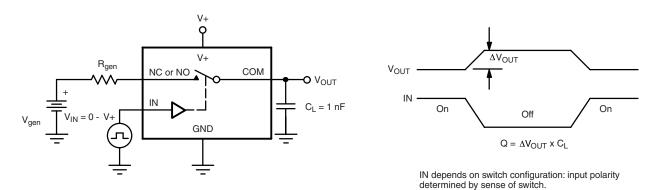


Figure 3. Charge Injection

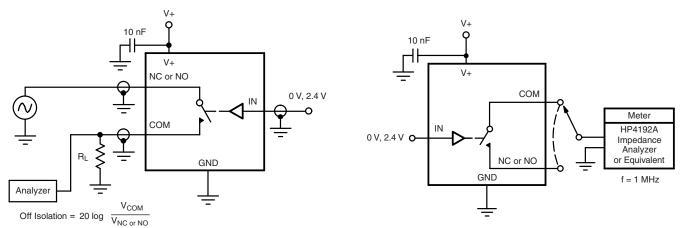


Figure 4. Off-Isolation

Figure 5. Channel Off/On Capacitance

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Revision: 18-Jul-08

Document Number: 91000 www.vishay.com