Quad, High Speed, ±100V 850mA, Ultrasound Damper

Features

- HVCMOS® technology for high performance
- High density integration ultrasound transmitter
- 0 to ±100V open-drain voltage
- ±850mA source and sink current
- Up to 20MHz operation frequency
- Matched delay times
- 1.8 to 5V CMOS logic interface

Applications

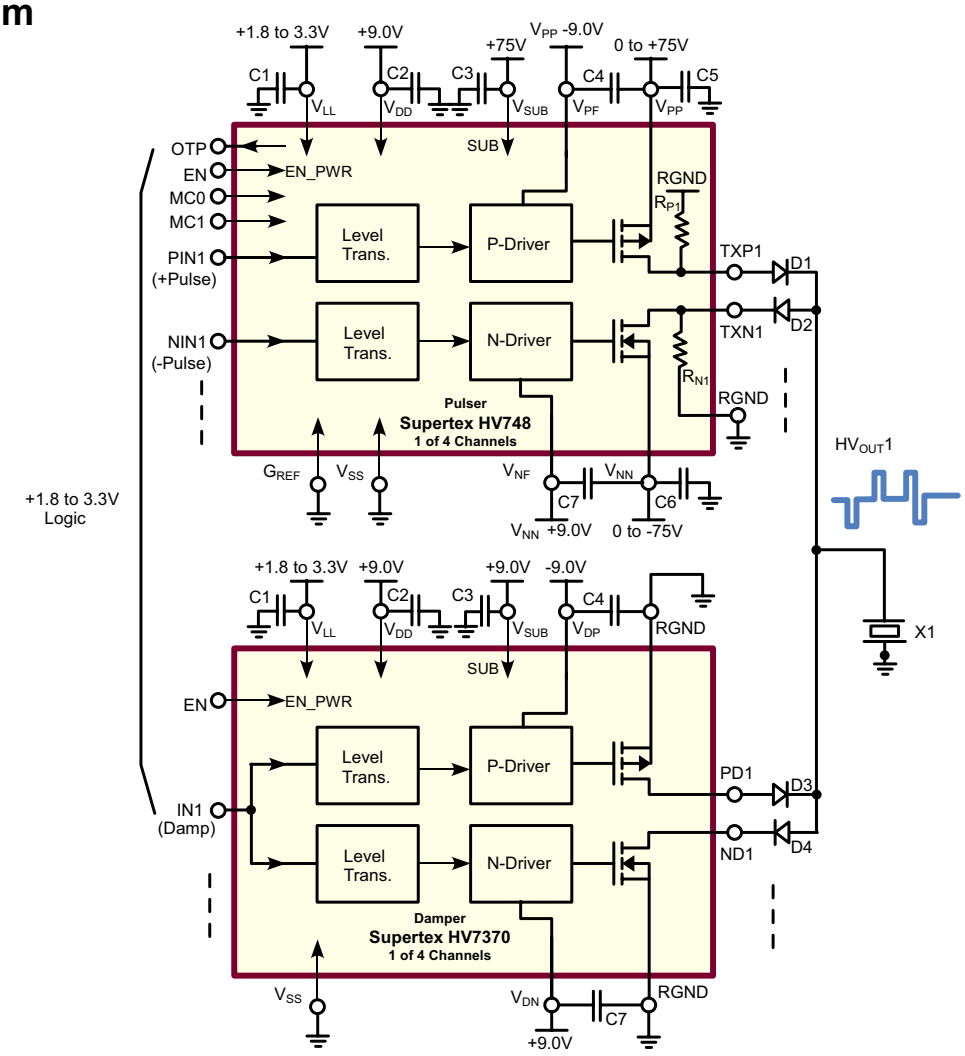
- Medical ultrasound imaging
- Piezoelectric transducer drivers
- NDT ultrasound transmission
- Pulse waveform generator

General Description

The Supertex HV7370 is a four-channel, monolithic high voltage, high-speed damper. It is designed for working with the HV738, HV748 or HV758 for medical ultrasound waveform generators requiring fast return-to-zero applications. The HV7370 consists of a controller logic interface circuit, level translators, MOSFET gate drives and high current power P-channel and N-channel MOSFETs as the output stage for each channel.

The output stages of each channel are designed to provide peak output currents of over ±0.85A for damping to ground, with up to ±100V swing. The control from inputs to outputs uses direct coupling topology, which not only saves components and PCB layout space, but also makes the damping frequency function down to DC.

Block Diagram



Ordering Information

Device	Package Option
	32-Lead QFN ***5.00x5.00mm body*** ***1.00mm height (max)*** ***0.50mm pitch***
HV7370	HV7370K6-G

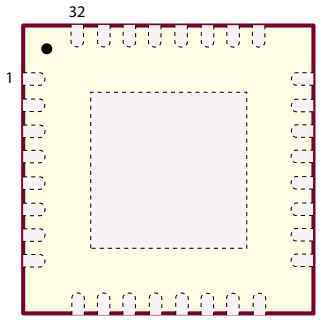
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
V_{SS}, power supply reference	0V
V_{LL}, positive logic supply	-0.5V to +7.0V
V_{DD}, positive logic, level translator supply	-0.5V to +13V
(RGND - V_{DP}), P-Gate driver supply	+0.5V to -13V
(V_{DN} - RGND), N-Gate driver supply	-0.5V to +13V
RGND, RTZ-Ground voltage	-2.0V to +2.0V
All logic input PIN_X, NIN_X and EN voltages	-0.5V to +7.0V
VSUB substrate voltage	+120V
(ND_X - RGND) damping N-MOSFET BVSUB voltage	+120V
(PD_X - RGND) damping P-MOSFET BVSUB voltage	-120V
Maximum junction temperature	+150°C
Storage temperature	-65°C to 150°C
Thermal resistance, θ_{JA}	21.6°C/W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



32-Lead QFN (K6)
(top view)

Package Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
___ = "Green" Packaging

32-Lead QFN (K6)

Power-Up Sequence of Pulser & Damper

Step	Description
1	V_{SUB}
2	V_{LL} with logic signal low
3	V_{DD}, V_{DN}, and V_{DP}
4	(V_{PP}- V_{PF}) and (V_{NF}- V_{NN})
5	V_{PP} and V_{NN}
6	Logic control signals

Power-Down Sequence of Pulser & Damper

Step	Description
1	All logic control signals go to low
2	V_{PP} and V_{NN}
3	(V_{PP}- V_{PF}) and (V_{NF}- V_{NN})
4	V_{DD}, V_{DN}, and V_{DP}
5	V_{LL}
6	V_{SUB}

Operating Supply Voltages and Current (4 Channel Active)

(Operating conditions, unless otherwise specified, V_{SS} = 0V,V_{LL} = +3.3V,V_{DD} = V_{DN} = +9V, V_{DP} = -9V, V_{PP} - V_{PF} = +9V, V_{NN} - V_{NF} = -9V, V_{SUB} = +75V V_{PP}/V_{NN} = ±75V, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{LL}	Logic voltage reference	1.8	3.3	5.0	V	---
V_{DD}	Internal voltage supply[1]	5.0	8.0 to 11	12	V	---
V_{DP}	P-Gate driver supply	-12	-V_{DD}	-5.0	V	Negative voltage supply
V_{DN}	N-Gate drive supply	5.0	V_{DD}	12	V	Positive voltage supply
V_{SUB}	IC substrate voltage	5.0	V_{DD}	100	V	---
RGND	RTZ-Ground voltage	-2.0	0	+2.0	V	---
I_{LL}	V_{LL} Current EN = Low	-	35	120	µA	---
I_{DDQ}	V_{DD} Current EN = Low	-	10	-	µA	---
I_{DDEN}	V_{DD} Current EN = High	-	1.5	3.0	mA	f = 0MHz
I_{DDEN}	V_{DD} Current	-	6.0	-	mA	f = 5.0MHz, continuous, no loads
I_{DPQ}	V_{DP} Current EN = Low	-	50	-	µA	f = 0MHz
I_{DPEN}	V_{DP} Current	-	30	-	mA	f = 5.0MHz, continuous, no loads
I_{DNQ}	V_{DN} Current EN = Low	-	50	-	µA	f = 0MHz
I_{DNEN}	V_{DN} Current	-	12	-	mA	f = 5.0MHz, continuous, no loads

Note:

1. P&N-FETs best matching when V_{DD} = V_{DN} = +10V, V_{PN} = -10V

Under Voltage

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{UVDD}	V_{DD} threshold	2.0	3.7	7.0	V	---
V_{UVLL}	V_{LL} threshold	1.0	1.25	1.5	V	---
V_{UVVDN}	UV threshold for V_{DN}	3.5	4.25	4.75	V	---
V_{UVVDP}	UV threshold for V_{DP}	1.75	4.5	6.0	V	Typ V_{UVVDP} ≤ -(V_{DN}/2), [V_{DN} = +9.0V]

Electrical Characteristics

(Operating conditions, unless otherwise specified, V_{SS} = 0V,V_{LL} = +3.3V,V_{DD} = V_{DN} = +9V, V_{DP} = -9V, V_{PP} - V_{PF} = +9V, V_{NN} - V_{NF} = -9V, V_{SUB} = +75V, V_{PP}/V_{NN} = ±75V, T_A = 25°C)

Output P-Channel MOSFET, PDx

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	0.6	0.85	-	A	---
R_{ON}	Channel resistance	-	13	-	Ω	I_{SD} = 100mA
C_{OSS}	Output capacitance	-	50	-	pF	V_{SUB} = 25V, f = 1.0MHz

Output N-Channel MOSFET, NDx

I_{OUT}	Output saturation current	0.6	0.85	-	A	---
R_{ON}	Channel resistance	-	12.5	-	Ω	I_{DS} = 100mA
C_{OSS}	Output capacitance	-	20	-	pF	V_{SUB} = 25V, f = 1.0MHz

Logic Inputs

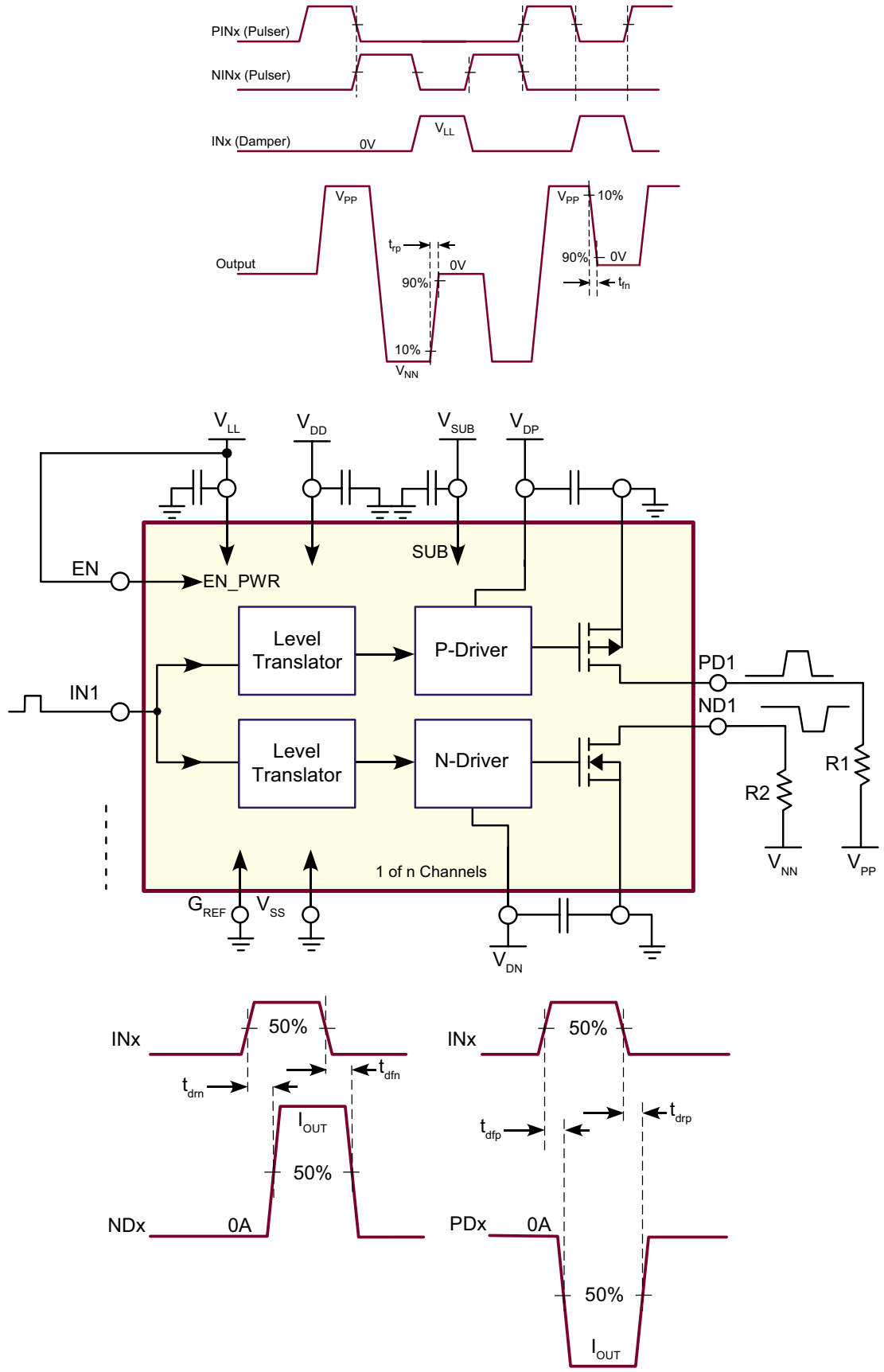
Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input logic high voltage	(V_{LL} -0.4)	-	V_{LL}	V	---
V_{IL}	Input logic low voltage	0	-	0.4	V	---
I_{IH}	Input logic high current	-	-	10	µA	---
I_{IL}	Input logic low current	-10	-	-	µA	---
C_{IN}	Input logic capacitance	-	5	-	pF	---

AC Electrical Characteristics

(Operating conditions, unless otherwise specified, V_{SS} = 0V,V_{LL} = +3.3V,V_{DD} = V_{DN} = +9V, V_{DP} = -9V, V_{PP} - V_{PF} = +9V, V_{NN} - V_{NF} = -9V, V_{SUB} = +75V V_{PP}/V_{NN} = ±75V, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_{rp}	P-FET output rise time	-	26	-	ns	330pF//2.5kΩ load
t_{fn}	N-FET output fall time	-	26	-	ns	
f_{OUT}	Output frequency range	-	-	20	MHz	---
t_{EN}	Enable time	-	180	500	µs	100Ω resistor load, +10V to ND_X and -10V to PD_X
t_{EN}	Disable time	-	2.8	10		
t_{drp}	P-FET on delay time	-	19	-	ns	8.2Ω resistor load (see timing diagram)
t_{dfp}	P-FET off delay time	-	17	-		
t_{drn}	N-FET on delay time	-	19	-		
t_{dfn}	N-FET off delay time	-	17	-		
Δt_{DELAY}	$\lvert t_{dr} - t_{df} \rvert$ delay time matching	-	±3.0	-	ns	P to N, channel to channel
tJ	Delay time jitter, rise or fall	-	15	-	ps	V_{PP}/V_{NN} = ±25V, input rising 50% to output PD_X/ND_X rising/falling 50%, with 100Ω load

Switch Test Timing Diagram



Pin Description

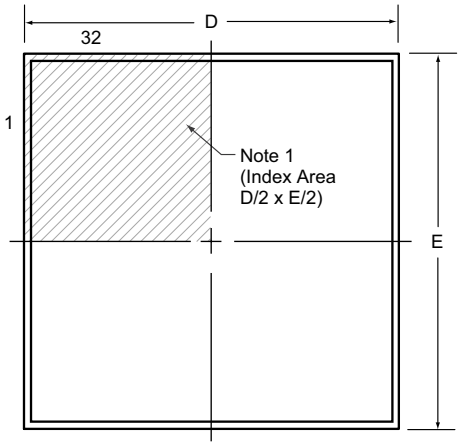
Pin #	Name	Description
1	VLL	Logic Hi voltage reference input (+3.3V).
2	VSS	Power supply return (0V).
3	IN1	Input logic control of damping P&N-FET of channel 1, Hi = on, Low = off.
4	IN2	Input logic control of damping P&N-FET of channel 2, Hi = on, Low = off.
5	IN3	Input logic control of damping P&N-FET of channel 3, Hi = on, Low = off.
6	IN4	Input logic control of damping P&N-FET of channel 4, Hi = on, Low = off.
7	VSS	Power supply return (0V).
8	VDD	Positive internal voltage supply (+9.0V).
9	NC	No connection.
10	VSUB	Substrate of the damper HV7370, must V_{SUB} = V_{DD}, or V_{SUB} of the pulser.
11	VDP	P-FET drive floating power supply, (RGND - V_{DP}) = +9.0V.
12	RGND	Return ground.
13	RGND	
14	RGND	
15	VDN	N-FET drive floating power supply, (V_{DN} - RGND) = +9.0V.
16	VSUB	Substrate of the damper HV7370, must V_{SUB} = V_{DD}, or V_{SUB} of the pulser.
17	ND4	Output damping N-FET drain (open drain output) for channel 4.
18	PD4	Output damping P-FET drain (open drain output) for channel 4.
19	ND3	Output damping N-FET drain (open drain output) for channel 3.
20	PD3	Output damping P-FET drain (open drain output) for channel 3.
21	ND2	Output damping N-FET drain (open drain output) for channel 2.
22	PD2	Output damping P-FET drain (open drain output) for channel 2.
23	ND1	Output damping N-FET drain (open drain output) for channel 1.
24	PD1	Output damping P-FET drain (open drain output) for channel 1.
25	VSUB	Substrate of the damper HV7370, must V_{SUB} = V_{DD} , or V_{SUB} of the pulser.
26	VDN	N-FET drive floating power supply, (V_{DN} - RGND) = +9.0V.
27	RGND	Return ground.
28	RGND	
29	RGND	
30	VDP	P-FET drive floating power supply, (RGND - V_{DP}) = +9.0V.
31	VSUB	Substrate of the damper HV7370, must V_{SUB} = V_{DD}, or V_{SUB} of the pulser.
32	EN	Chip power enable Hi = on, Low = off.
Thermal Pad (VSUB)		Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to VSUB. VSUB normally is connected to V_{DD} = +9.0V or +75V (pulser VSUB).

Note:

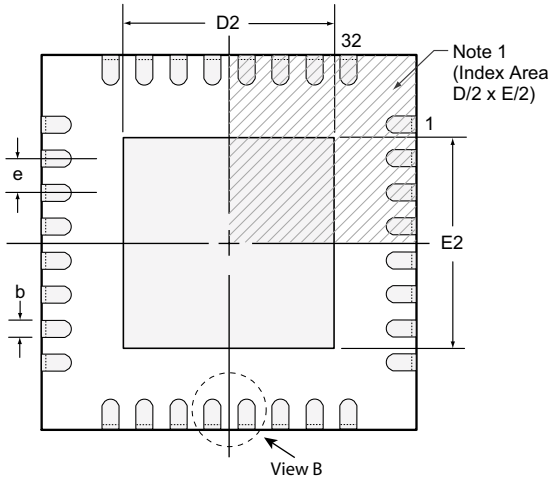
Thermal pad must be connected to VSUB.

32-Lead QFN Package Outline (K6)

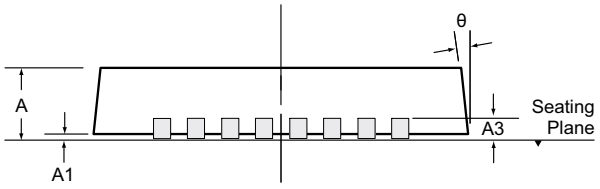
5.00x5.00mm body, 1.00mm height (max), 0.50mm pitch



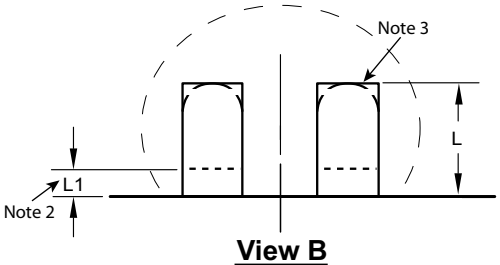
Top View



Bottom View



Side View



View B

Notes:

1. *Details of Pin 1 identifier are optional, but must be located within the indicated area. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	4.85*	1.05	4.85*	1.05	0.50 BSC	0.30†	0.00	0°
	NOM	0.90	0.02		0.25	5.00	-	5.00	-		0.40†	-	-
	MAX	1.00	0.05		0.30	5.15*	3.55†	5.15*	3.55†		0.50†	0.15	14°

JEDEC Registration MO-220, Variation VHHD-6, Issue K, June 2006.
** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*
† This dimension is a non-JEDEC dimension.
Drawings not to scale.
Supertex Doc. #: *DSPD-32QFNK65X5P050, Version A071408.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 222-8888 / FAX: (408) 222-4895
www.supertex.com