M62463AFP

Dolby Pro Logic Surround Decoder

REJ03F0275-0200
Rev.2.00
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Description

The M62463AFP is a single chip Dolby Pro Logic surround decoder. This LSI has all of required functions for Dolby Pro Logic surround.

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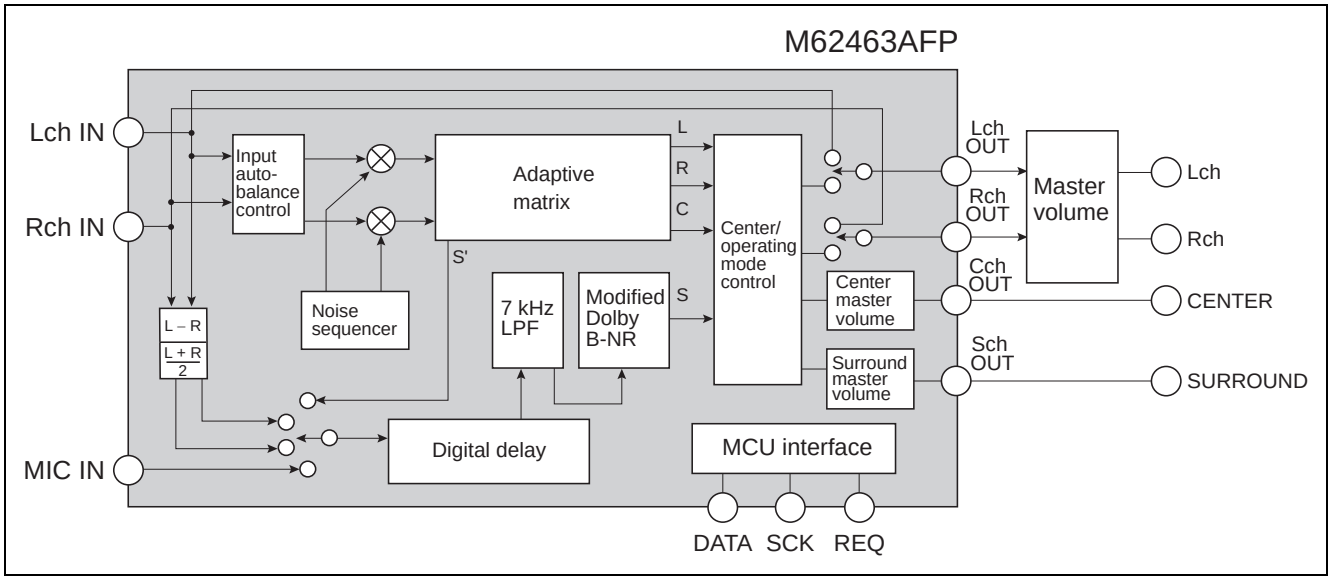
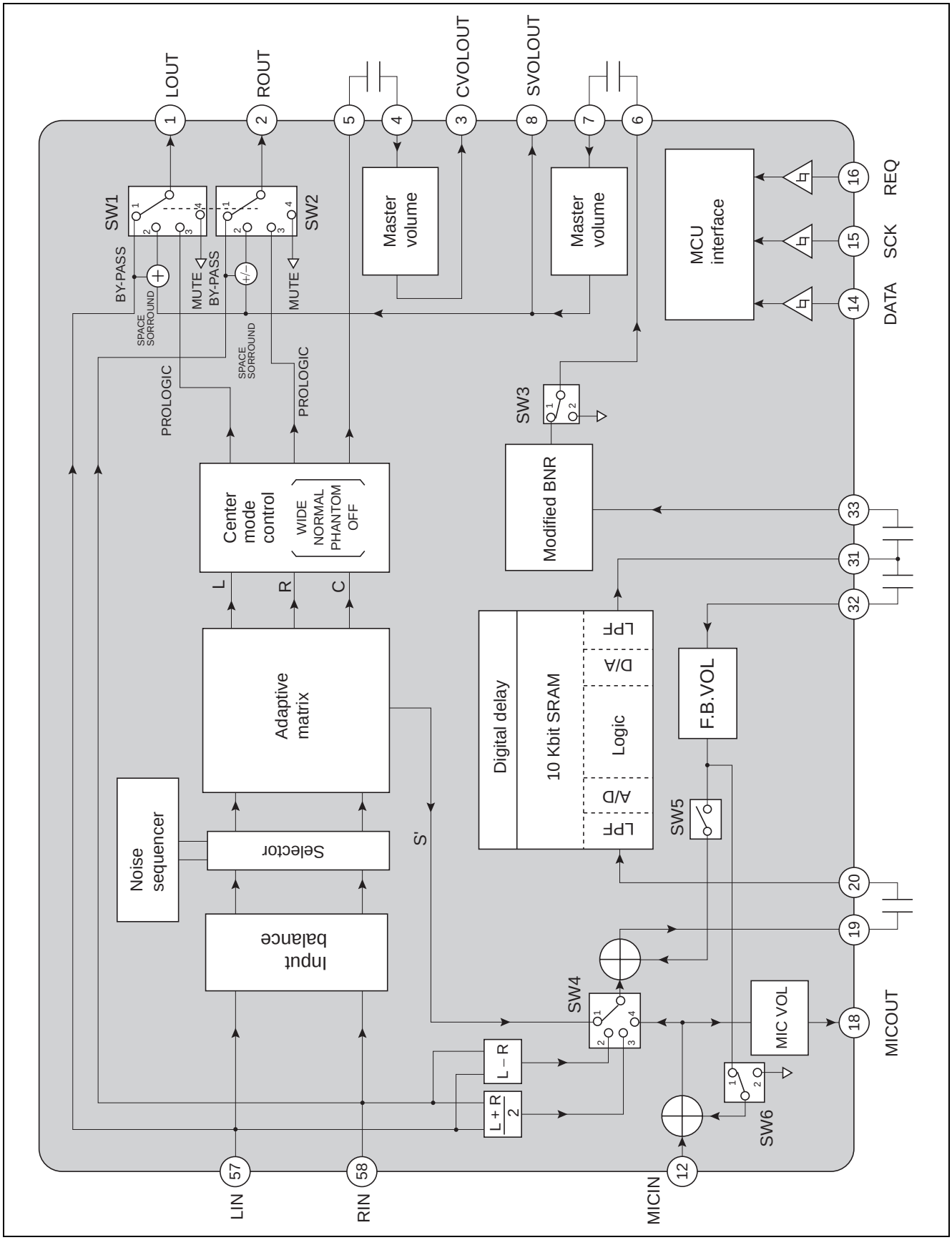
Features

- Includes all functions necessary for Dolby Pro Logic surround
  - Adaptive matrix
  - Input auto-balance
  - Noise sequencer
  - Center mode control ON/OFF, WIDE/NORMAL/PHANTOM
  - Modified Dolby B type noise reduction
  - 4 channel (Lch/Rch/Cch/Sch) / 3 channel (Lch/Rch/Cch)
  - Digital delay Delay time: 15.4 to 51.2 ms
- Cch/Sch master volume: 0 to –87 dB / 1 dB step, –∞
- 3-lines MCU control
- Space surround such as Disco, Hall and Live
- Digital echo for Karaoke function Delay time: 123,184 ms
- Current control oscillation circuit for system clock

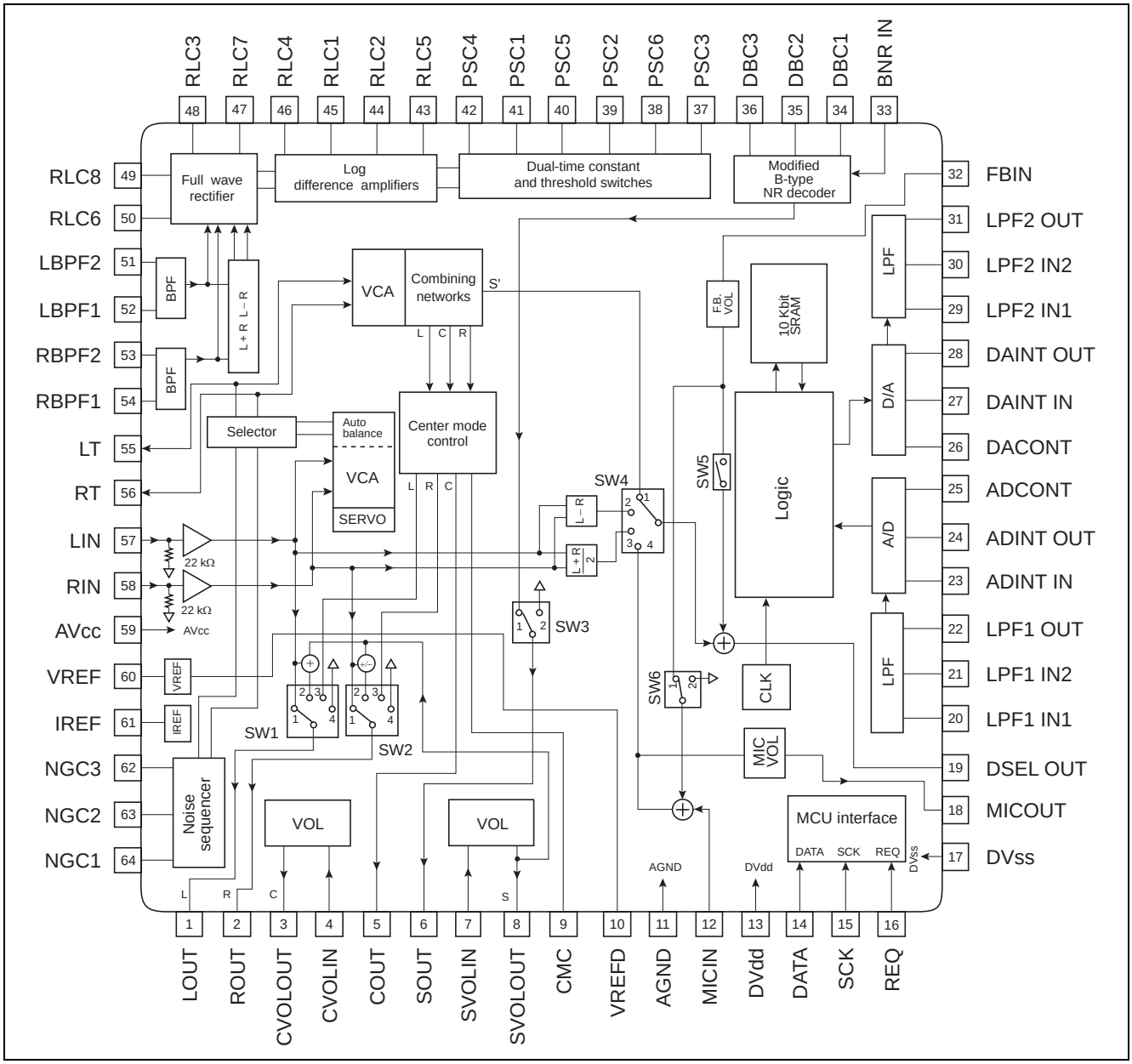
System Configuration



Block Diagram



Pin Arrangement



Functional Description

Function		Description
1	Fundamental function for Dolby Pro Logic surround decoder	Adaptive matrix Input auto-balance Noise sequencer Center mode control ON/OFF WIDE/NORMAL/PHANTOM Modified Dolby B type noise reduction 4 ch (L, R, C, S), 3 ch (L, R, C) mode switch
2	RAM for digital delay	10-Kbit RAM
3	Surround delay time	15.4, 20.5, 25.6, 29.2 ms (for Dolby Pro Logic surround) 51.2 ms (for space surround)
4	Circuit for space surround	Digital delay circuit can be used for space surround such as a Disco, Hall or Live, and Karaoke echo
5	Echo delay time	123,184 ms
6	Feedback volume	Delay signal feedback volume –3 to –21 dB / 3 dB step, and –∞
7	Microphone volume	Internal microphone volume 0 to –18 dB / 3 dB step, and –∞
8	Cch/Sch master volume	0 to –87 dB / 1 dB step, and –∞
9	Bypass switch	Bypass the decode circuit
10	Output mute	Mute the Lch and Rch output
11	MCU interface	Controlled by 3-lines serial data from MCU Including the chip address (2-bit)
12	Current control oscillation circuit	Including the oscillation circuit without external parts

Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit
Supply voltage	Vcc	10.5	V
	Vdd	6.5	V
Power dissipation	Pd	1	W
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–40 to +125	°C

Recommended Operating Condition

Item	Symbol	Min	Typ	Max	Unit	Condition
Supply voltage	Vcc	8	9	10	V	
	Vdd	4.5	5	5.5	V	
Input voltage (L)	V_{IL}	0	—	0.8	V	14, 15, 16 pin
Input voltage (H)	V_{IH}	Vdd – 1	—	Vdd	V	14, 15, 16 pin

Electrical Characteristics

(Ta = 25°C, Vcc = 9 V, Vdd = 5 V, Cch volume = 0 dB, at C-OUT 0 dBd = 300 mVrms, f = 1 kHz, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Total						
Circuit current	I_{CC}	—	25	40	mA	No signal
Circuit current	I_{DD}	—	13	25	mA	No signal
Auto-Balance						
Capture range	CPR	—	5	—	dB	
Error correction	CER	—	4	—	dB	
Adaptive Matrix						
Output level accuracy relative to Cch	ΔVoL	–0.5	0	0.5	dB	L, R, Sch output
Matrix rejection	MR	25	40	—	dB	L, R, C, Sch output
Head room	HRAM	15	17	—	dB	L, R, C, Sch output
Total harmonic distortion	THDAM	—	0.05	0.2	%	L, R, Cch output, 30 kHzLPF
S/N ratio	SNAM	70	80	—	dB	Rg = 0 Ω, weighted CCIR/ARM, 4 ch mode
Noise Sequencer						
Output noise level	Vno	–15	–12.5	–10	dB	L, R, C, Sch output
Noise level accuracy relative to Cch	ΔVno	–0.5	0	0.5	dB	L, R, Sch output
Modified B Noise Reduction (Sch volume = 0 dB, 0 dB reference is 300 mVrms/100 Hz at S-Out)						
Gain between input and output	VGNR	—	5.1	—	dB	Vin = 0 dBd, f = 100 Hz
Decode character 1	DEC1	–1.6	–0.1	1.4	dB	Vin = 0 dBd, f = 1.0 kHz
Decode character 2	DEC2	–3.0	–1.5	0		Vin = –15 dBd, f = 1.4 kHz
Decode character 3	DEC3	–4.9	–3.4	–1.9		Vin = –20 dBd, f = 1.4 kHz
Decode character 4	DEC4	–6.8	–5.3	–3.8		Vin = –40 dBd, f = 5.0 kHz
Total harmonic distortion	THDNR	—	0.07	0.3	%	Vin = 0 dBd, f = 1 kHz, 30 kHzLPF
Head room	HRNR	15	17	—	dB	THD = 1%
S/N ratio	SNNR	68	78	—	dB	Rg = 0 Ω, weighted CCIR/ARM
Cch/Sch Master Volume						
Maximum attenuator	ATTmax	—	–95	–87	dB	ATT = –∞, Vi = 2 Vrms
Minimum attenuator	ATTmin	–3.0	0	3.0	dB	ATT = 0 dB
Volume step	VOLS1	0.5	1.0	1.5	dB	ATT = 0 to –40 dB
	VOLS2	0.2	1.0	1.8	dB	ATT = –40 to –87 dB
Volume cross-talk	CTVOL	68	83	—	dB	R input/CVOL, SVOL output
Output noise voltage	VnoVOL	—	2.6	5.2	μVrms	ATT = –∞
Line (Bypass mode)						
Total harmonic distortion	THDLN	—	0.002	0.05	%	L, Rch output, 30 kHzLPF
S/N ratio	SNLN	95	100	—	dB	L, Rch output
Line cross-talk	CTLN	70	80	—	dB	L input/R output, R input/L output
Input impedance	Zi	11	22	44	kΩ	

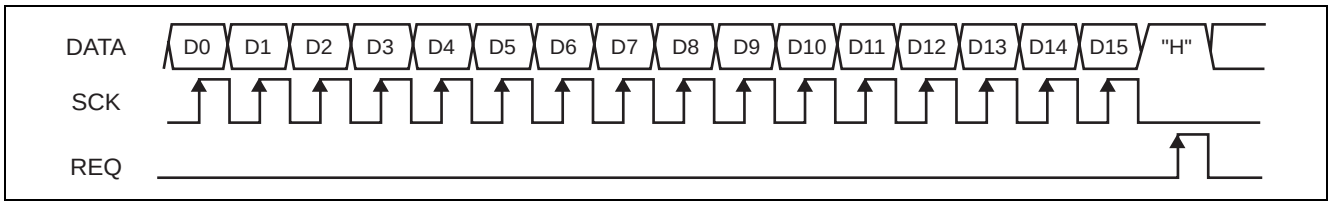
(Ta = 25°C, Vcc = 9 V, Vdd = 5 V, Vin = 200 mVrms, f = 1 kHz, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Digital Delay							
Input/output voltage gain	GvD	–8.1	–5.1	–2.1	dB	LIN-LPF2OUT, surround L – R	
Delay time	Td	17.4	20.5	23.6	ms	Td = 20.5 ms	
Total harmonic distortion	THDD	—	0.5	0.9	%	30 kHz LPF	Td = 20.5 ms
		—	1.2	2.2			Td = 51.2 ms
		—	3.0	5.6			Td = 184 ms
Output noise voltage	NoD	—	–92	–80	dBV	Vin = 0 Vrms JIS-A	Td = 20.5 ms
		—	–84	–70			Td = 51.2 ms
		—	–80	–65			Td = 184 ms
Maximum output voltage	Vomax	0.7	1.0	—	Vrms	THD = 10%	
LPF cut-off frequency	LPFfc	6.0	7.0	8.0	kHz	Td = 15.4 to 51.2 ms Gv = –3 dB (Dolby Pro Logic mode)	
		—	3.0	—	kHz	Td = 123,184 ms (Echo mode) Gv = –3 dB	
Feedback Volume							
Maximum attenuation	FBATTmax	—	–70	–60	dB	ATT = –∞	
Minimum attenuation	FBATTmin	–6.0	–3.0	0	dB	ATT = –3 dB	
Volume step	FBVOLS	—	3.0	—	dB		
Microphone Volume							
Maximum attenuation	MICATTmax	—	–70	–60	dB	ATT = –∞	
Minimum attenuation	MICATTmin	–3.0	0	3.0	dB	ATT = 0 dB	
Volume step	MICVOLS	—	3.0	—	dB		
Output noise voltage	VnoMIC	—	2.0	4.0	μVrms	ATT = –∞	

Serial Data Control Format

(1) Data input format

DATA is read at the rising edge of SCK, and loaded last 16 bits at the rising edge of REQ.



D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
L	L	Mode set		Pro Logic mode	Center mode		Sch volume							L	H
	H	Delay time			Auto-balance	set to "L"	Cch volume							Chip address	
H	L	Noise sequencer			Surround/echo mode										
	H	Test mode (user inhibit)													

(2) Control condition

No.	Control Mode	Contents
1	Mode set	Normal stereo/Dolby Pro Logic/space surround or echo/mute
2	Pro Logic mode	4 ch Pro Logic/3 ch stereo
3	Center mode	Wide/Normal/Phantom/OFF
4	Delay time	15.4, 20.5, 25.6, 29.2, 51.2 ms (for surround) 123,184 ms (for echo)
5	Auto-balance	Input auto-balance ON/OFF
6	Noise sequencer	ON/OFF Lch/Rch/Cch/Sch
7	Surround/echo mode	Delay input L – R/(L + R) / 2 /MICin Feedback volume, microphone volume, delay output mixing
8	Cch/Sch volume	0 to –87 dB / 1 dB step, and –∞
9	Chip address	Input data effect or not

(3) Set conditions

Mode Setting (D0 = "L", D1 = "L")

D2	D3	Condition
L	L	Normal stereo (bypass)
L	H	Dolby Pro Logic surround
H	L	Space surround/echo
H	H	Output mute

Pro Logic Mode Setting (D0 = "L", D1 = "L")

D4	Condition
L	4 ch Pro Logic
H	3 ch stereo

Center Mode Setting (D0 = "L", D1 = "L")

D5	D6	Condition
L	L	Wide
L	H	Normal
H	L	Phantom
H	H	OFF

Delay Time Setting (D0 = "L", D1 = "H")

D2	D3	D4	Delay Time	Sampling Frequency	LPF Cutoff Frequency
L	L	L	15.4 ms	500 kHz	7 kHz
L	L	H	20.5 ms	500 kHz	
L	H	L	25.6 ms	400 kHz	
L	H	H	29.2 ms	333 kHz	
H	L	L	51.2 ms	200 kHz	
H	L	H	123 ms	83.3 kHz	3 kHz
H	H	L	184 ms	55.6 kHz	

Auto-Balance Setting (D0 = "L", D1 = "H")

D5	Condition
L	Auto-balance OFF
H	Auto-balance ON

Noise Sequencer (D0 = "H", D1 = "L")

D2	D3	D4	Condition	
L	—	—	Noise sequencer OFF	
H	L	L	Noise sequencer ON	Lch
	L	H		Rch
	H	L		Cch
	H	H		Sch

Surround/Echo Mode (D0 = "H", D1 = "L")

Surround/Echo Mode Switch

D5	Condition
L	Surround
H	Echo

Delay Input

D6	Delay Input
L	L – R
H	(L + R) / 2

Delay Mixing Polarity

D7	Mixing Polarity
L	L+ delay signal/R+ delay signal
H	L+ delay signal/R– delay signal

Feedback Volume

D8	D9	D10	Volume
L	L	L	–3 dB
L	L	H	–6 dB
L	H	L	–9 dB
L	H	H	–12 dB
H	L	L	–15 dB
H	L	H	–18 dB
H	H	L	–21 dB
H	H	H	–∞

Microphone Volume

D11	D12	D13	Volume
L	L	L	0 dB
L	L	H	–3 dB
L	H	L	–6 dB
L	H	H	–9 dB
H	L	L	–12 dB
H	L	H	–15 dB
H	H	L	–18 dB
H	H	H	–∞

Relation Between Mode Setting and Switch Condition

Mode Setting	Pro Logic Mode (D0 = L, D1 = L)	Surround/Echo Mode (D0 = H, D1 = L)		Switch Condition					
	D4	D5	D6	SW1	SW2	SW3	SW4	SW5	SW6
Normal stereo (bypass)	X	X	X	1	1	2	4	OFF	2
Dolby Pro Logic surround	L	X	X	3	3	1	1	OFF	2
	H					2			
Space surround/echo	X	L (Surround)	L	2	2	1	2	ON	2
			H	Delay mixing ON			3		
	X	H (Echo)	X	1	1	2	4	OFF	1
				Delay mixing OFF					
Mute	X	X	X	4	4	2	4	OFF	2

Note: X: L or H

Sch Volume Setting (D0 = "L", D1 = "L"), Cch Volume Setting (D0 = "L", D1 = "H")

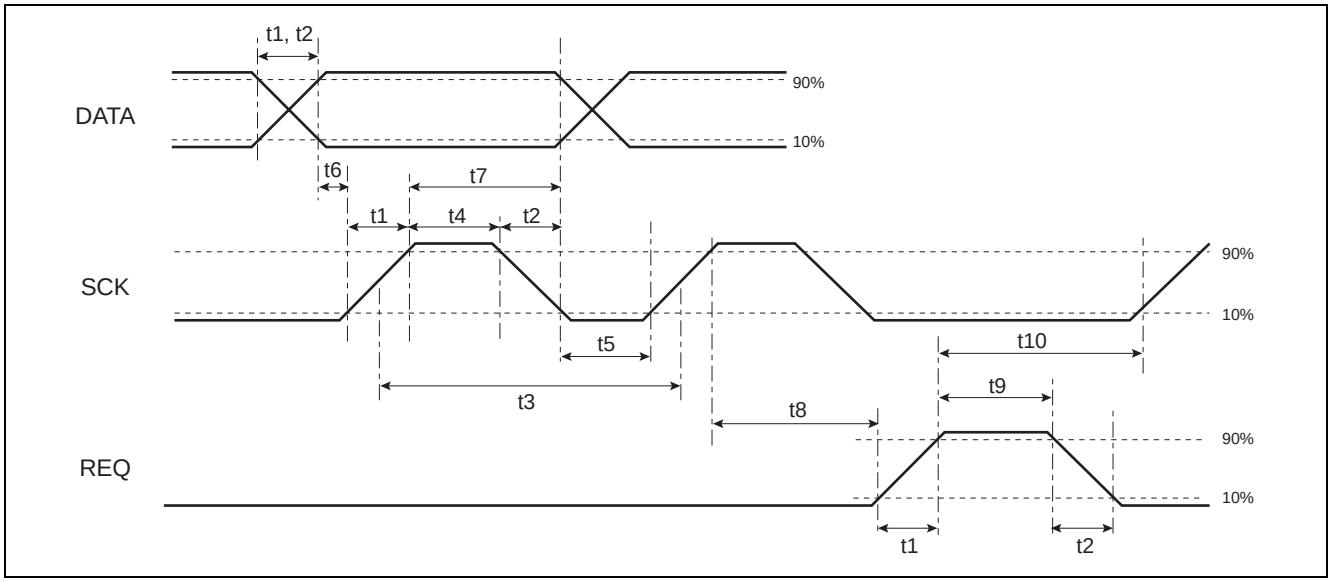
Volume Level	D7	D8	D9	D10	D11
0 dB	L	L	L	L	L
–2 dB	L	L	L	L	H
–4 dB	L	L	L	H	L
–6 dB	L	L	L	H	H
–8 dB	L	L	H	L	L
–10 dB	L	L	H	L	H
–12 dB	L	L	H	H	L
–14 dB	L	L	H	H	H
–16 dB	L	H	L	L	L
–18 dB	L	H	L	L	H
–20 dB	L	H	L	H	L
–22 dB	L	H	L	H	H
–24 dB	L	H	H	L	L
–26 dB	L	H	H	L	H
–28 dB	L	H	H	H	L
–30 dB	L	H	H	H	H
–32 dB	H	L	L	L	L
–34 dB	H	L	L	L	H
–36 dB	H	L	L	H	L
–40 dB	H	L	L	H	H
–44 dB	H	L	H	L	L
–48 dB	H	L	H	L	H
–52 dB	H	L	H	H	L
–56 dB	H	L	H	H	H
–60 dB	H	H	L	L	L
–64 dB	H	H	L	L	H
–68 dB	H	H	L	H	L
–72 dB	H	H	L	H	H
–76 dB	H	H	H	L	L
–80 dB	H	H	H	L	H
–84 dB	H	H	H	H	L
–∞	H	H	H	H	H

Volume Level	D12	D13
0 dB	L	L
–1 dB	L	H
–2 dB	H	L
–3 dB	H	H

Chip Address

D14	D15	Data Read
L	H	Enable
Others		Unable

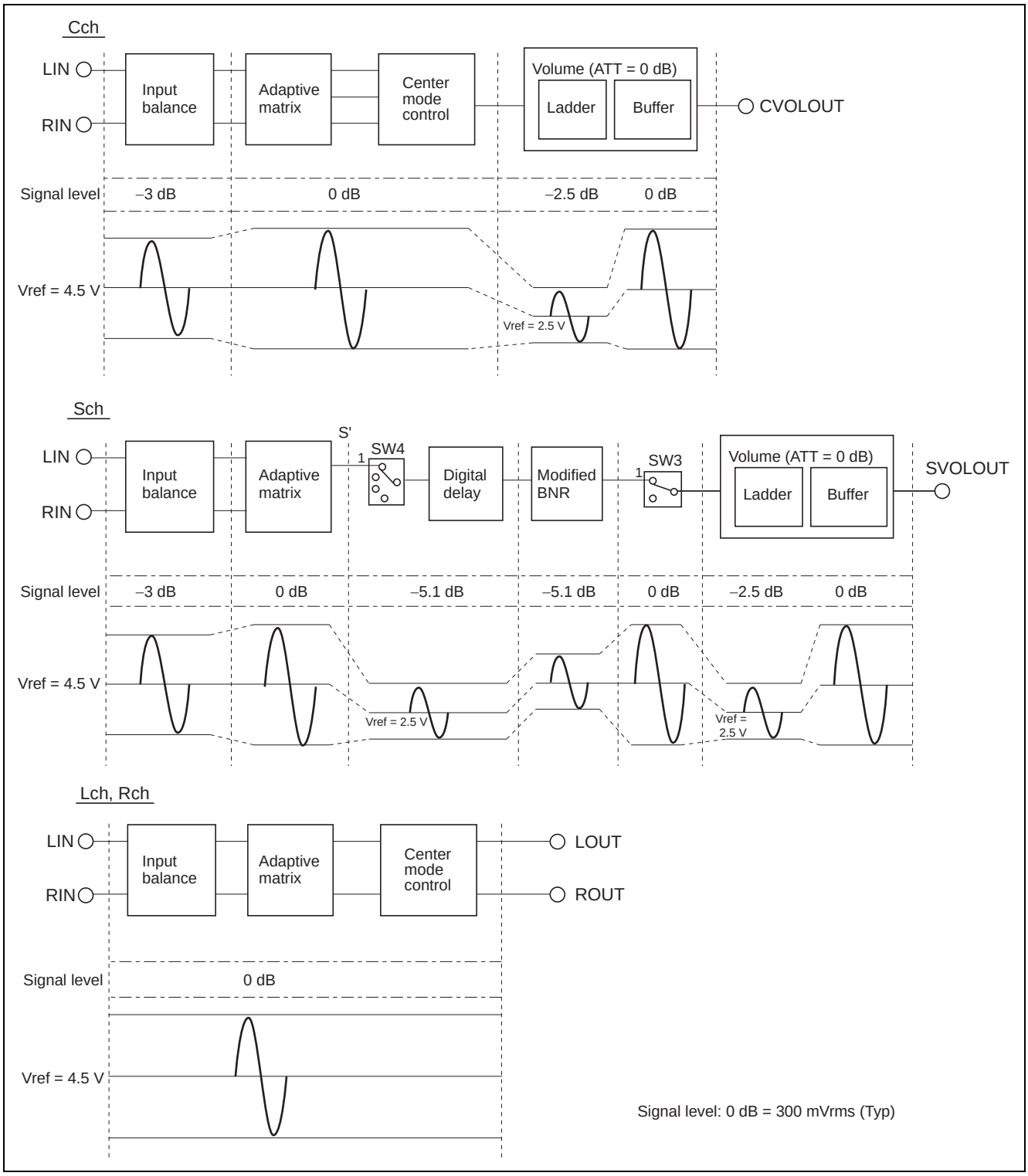
(4) Data timing



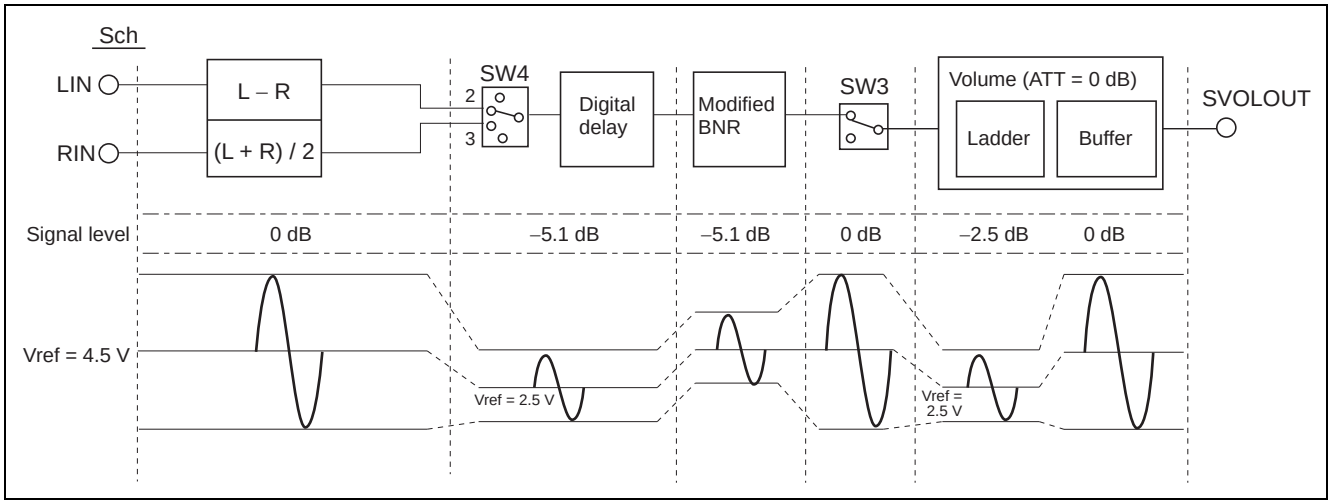
Symbol	Name	Min	Typ	Max	Unit
t1	Signal rise time	—	—	0.5	µs
t2	Signal fall time	—	—	0.5	µs
t3	SCK clock width	2	—	—	µs
t4	SCK "H" pulse width	0.8	—	—	µs
t5	SCK "L" pulse width	0.8	—	—	µs
t6	DATA setup time	0.8	—	—	µs
t7	DATA hold time	0.8	—	—	µs
t8	REQ rise hold time	1.6	—	—	µs
t9	REQ "H" pulse width	0.8	—	—	µs
t10	SCK setup time	1.6	—	—	µs

Level Diagram

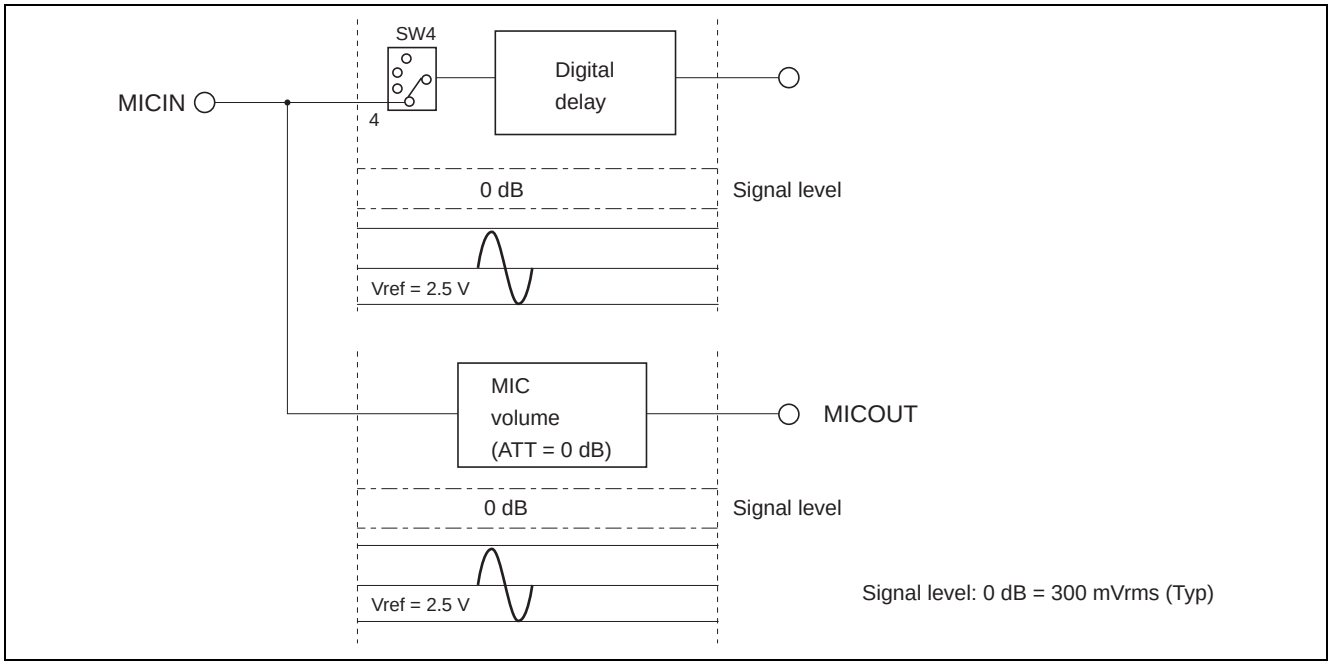
(1) Dolby Pro Logic surround mode



(2) Space surround mode



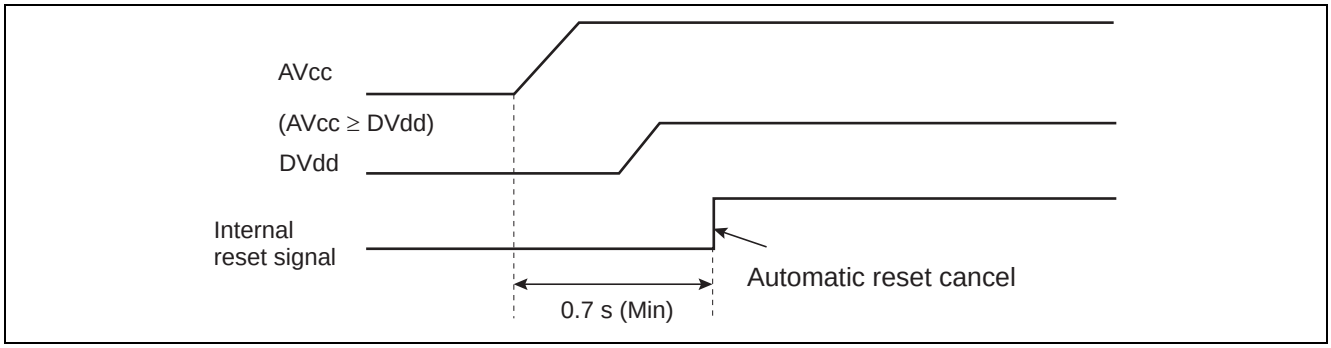
(3) Echo mode



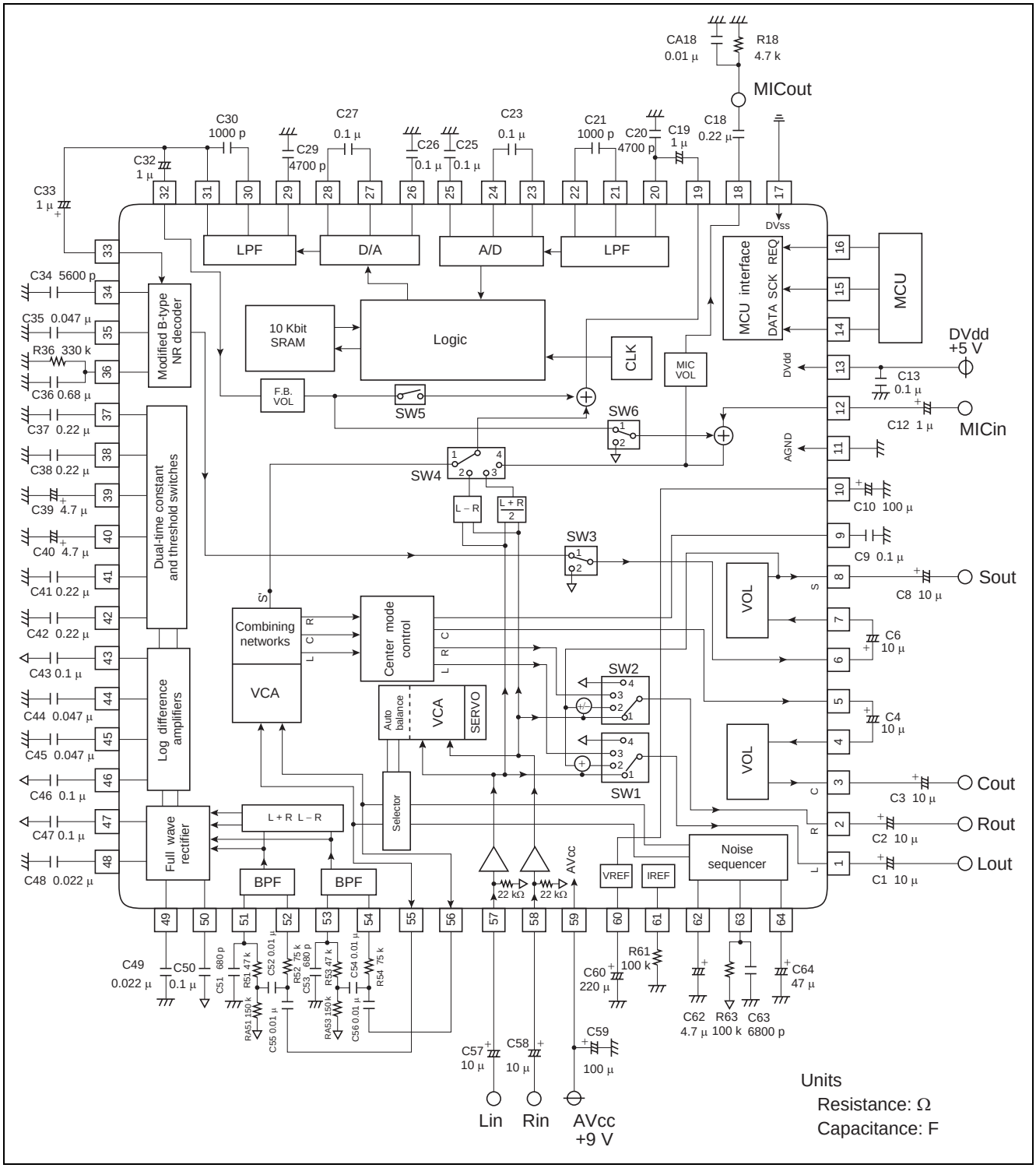
Notice

Relation AVcc and DVdd at power supply

Digital Vdd must be supplied less than 0.7 seconds from analog Vcc supply.



Application Example



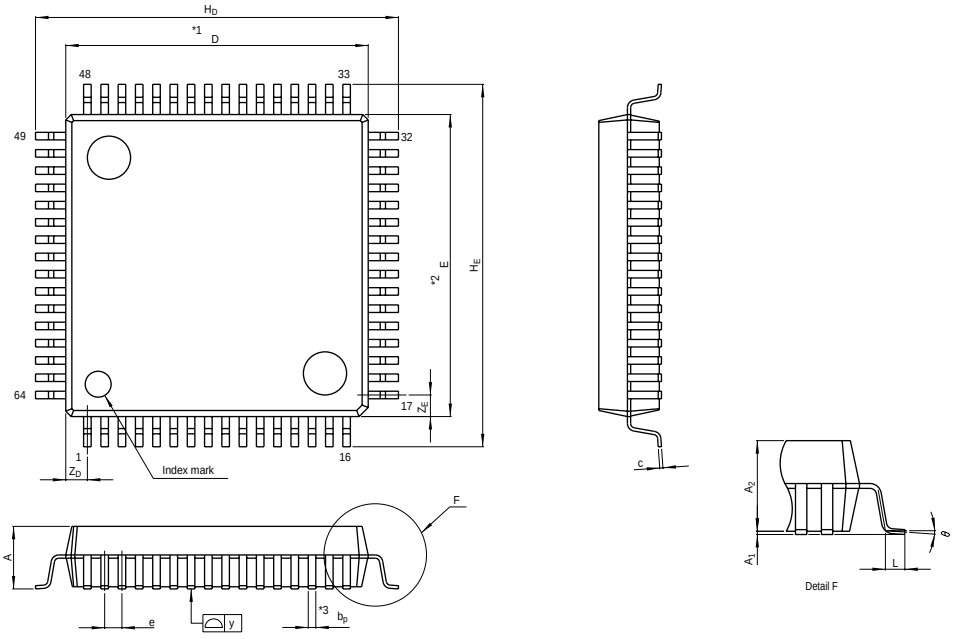
External Parts List

Parts No.	Values	Unit	Tol.
C1	10	µF	
C2	10	µF	
C3	10	µF	
C4	10	µF	
C6	10	µF	
C8	10	µF	
C9	0.1	µF	10%
C10	100	µF	
C12	10	µF	
C13	0.1	µF	
C18	0.22	µF	
CA18	0.01	µF	
C19	1.0	µF	non-polar
C20	4700	pF	5%
C21	1000	pF	5%
C23	0.1	µF	5%
C25	0.1	µF	5%
C26	0.1	µF	5%
C27	0.1	µF	5%
C29	4700	µF	5%
C30	1000	pF	5%
C32	1.0	µF	
C33	1.0	µF	
C34	5600	pF	5%
C35	0.047	µF	5%
C36	0.68	µF	10%
C37	0.22	pF	10%
C38	0.22	pF	10%
C39	4.7	µF	20%
C40	4.7	µF	20%
C41	0.22	µF	10%
C42	0.22	µF	10%
C43	0.1	µF	20%
C44	0.047	µF	5%
C45	0.047	µF	5%
C46	0.1	µF	20%

Parts No.	Values	Unit	Tol.
C47	0.1	µF	20%
C48	0.022	µF	5%
C49	0.022	µF	5%
C50	0.1	µF	20%
C51	680	pF	5%
C52	0.01	µF	5%
C53	680	pF	5%
C54	0.01	µF	5%
C55	0.01	µF	5%
C56	0.01	µF	5%
C57	10	µF	
C58	10	µF	
C59	100	µF	
C60	220	µF	
C62	4.7	µF	10%
C63	6800	pF	5%
C64	47	µF	
R18	4.7	kΩ	10%
R36	330	kΩ	10%
R51	47	kΩ	5%
RA51	150	kΩ	5%
R52	75	kΩ	5%
R53	47	kΩ	5%
RA53	150	kΩ	5%
R54	75	kΩ	5%
R61	100	kΩ	1%
R63	100	kΩ	5%

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP64-14x14-0.80	PRQP0064GA-A	64P6N-A	1.1g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.8	14.0	14.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	16.5	16.8	17.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.3	0.35	0.45
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.65	0.8	0.95
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.4	0.6	0.8

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Colophon .7.2