32-Mbit (1M x 32) Static RAM

Features

- **High density 32-Mbit SRAM**
- **High speed**
  - **t_{AA} = 10 ns**
- **Low active power**
  - **I_{CC} = 450 mA**
- **Operating voltages of 3.3 ± 0.3V**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL compatible inputs and outputs**
- **Available in standard 119-ball FBGA**

Functional Description

The CYM1072AV33 is a 3.3V high-performance 32-Megabit static RAM organized as 1M words by 32 bits.

Writing to the device is accomplished by enabling the chip ($\overline{CE}_1$ LOW and CE_2 HIGH) while forcing the Write Enable ($\overline{WE}$) input LOW. If Byte Enable A ($\overline{B}_A$) is LOW, then data from the I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{19}). If Byte Enable B ($\overline{B}_B$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{19}). Likewise, $\overline{B}_C$ and $\overline{B}_D$ correspond with the I/O pins I/O_{16} to I/O_{23} and I/O_{24} to I/O_{31}, respectively.

Reading from the device is accomplished by enabling the chip by taking $\overline{CE}_1$ LOW and CE_2 HIGH while forcing the Output Enable ($\overline{OE}$) LOW and the Write Enable ($\overline{WE}$) HIGH. If the first Byte Enable ($\overline{B}_A$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte Enable B ($\overline{B}_B$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. Similarly, $\overline{B}_c$ and $\overline{B}_D$ correspond to the third and fourth bytes. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_0 through I/O_{31}) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH/CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), the byte selects are disabled ($\overline{B}_{A-D}$ HIGH), or during a Write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C1072AV33 is available in a 119-ball grid array (FBGA) package.
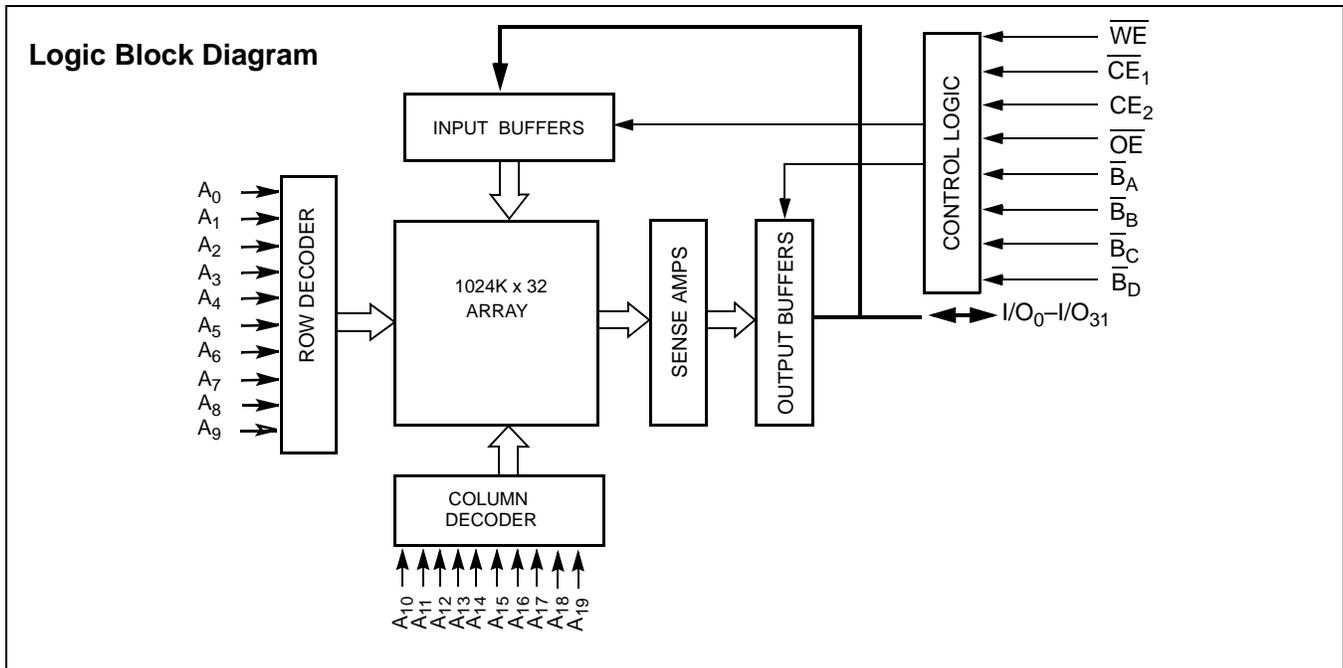
Selection Guide

	CY7C1072AV33-10	CY7C1072AV33-12	Unit
Maximum Access Time	10	12	ns
Maximum Operating Current	450	400	mA
Maximum Standby Current	100	100	mA

Pin Configurations

119 BGA

(Top View)

	1	2	3	4	5	6	7
A	I/O_{16}	A	A	A	A	A	I/O_0
B	I/O_{17}	A	A	$\overline{CE_1}$	A	A	I/O_1
C	I/O_{18}	$\overline{B_c}$	CE_2	A	NC	$\overline{B_a}$	I/O_2
D	I/O_{19}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_3
E	I/O_{20}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_4
F	I/O_{21}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_5
G	I/O_{22}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_6
H	I/O_{23}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_7
J	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	DNU
K	I/O_{24}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_8
L	I/O_{25}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_9
M	I/O_{26}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{10}
N	I/O_{27}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_{11}
P	I/O_{28}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{12}
R	I/O_{29}	A	$\overline{B_d}$	NC	$\overline{B_b}$	A	I/O_{13}
T	I/O_{30}	A	A	$\overline{WE}$	A	A	I/O_{14}
U	I/O_{31}	A	A	$\overline{OE}$	A	A	I/O_{15}

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....−65°C to +150°C

Ambient Temperature with
Power Applied..−55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] ...... −0.5V to 4.6V

DC Voltage Applied to Outputs
in High Z State [1] ....−0.3V to V_{CC} + 0.3V

DC Input Voltage [1] .... −0.3V to V_{CC} + 0.3V

Current into Outputs (LOW).. 20 mA

Static Discharge Voltage.. >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	−40°C to +85°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−2	+2	−2	+2	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−2	+2	−2	+2	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{RC}	Com'l / Ind'l		450		400	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, CE_2 ≤ V_{IL}; V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			140		140	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} − 0.3V, or V_{IN} ≤ 0.3V, f = 0	Com'l / Ind'l		100		100	mA

Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	12	pF
C_{OUT}	Output Capacitance		15	pF

Thermal Resistance[2]

Parameter	Description	Test Conditions	All-Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[2]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[2]		TBD	°C/W

AC Test Loads and Waveforms[3]

(a)

(b)

(c) ALL INPUT PULSES
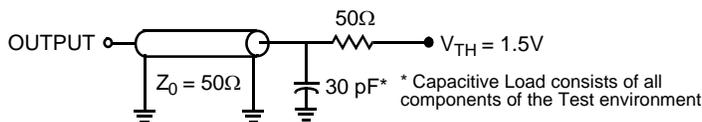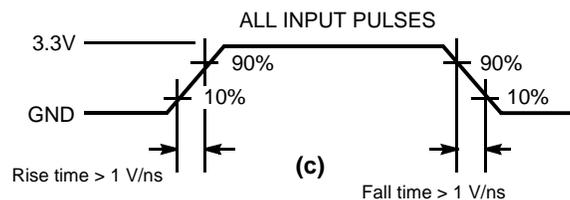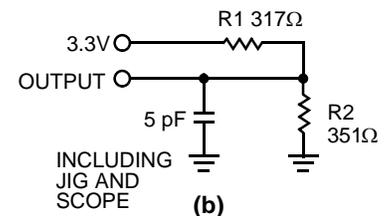
Notes:
1. V_{IL} (min.) = −2.0V and V_{IH}(max) = V_{CC} + 0.5V for pulse durations of less than 20 ns.
2. Tested initially and after any design or process changes that may affect these parameters.
3. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). As soon as 1ms (T_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0V) voltage.

Switching Characteristics[4,5] Over the Operating Range

Parameter	Description	-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
Read Cycle						
t_{power}	V_{CC}(typical) to the first access[6]	1		1		ms
t_{RC}	Read Cycle Time	10		12		ns
t_{AA}	Address to Data Valid		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ active to Data Valid		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	1		1		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		5		6	ns
t_{LZCE}	$\overline{CE}$ active to Low Z[7]	3		3		ns
t_{HZCE}	$\overline{CE}$ inactive to High Z[7]		5		6	ns
t_{PU}	$\overline{CE}$ active to Power-Up[8]	0		0		ns
t_{PD}	$\overline{CE}$ inactive to Power-Down[8]		10		12	ns
t_{DBE}	Byte Enable to Data Valid		10		12	ns
t_{LZBE}	Byte Enable to Low-Z	1		1		ns
t_{HZBE}	Byte Disable to High-Z		5		6	ns
Write Cycle[9, 10]						
t_{WC}	Write Cycle Time	10		12		ns
t_{SCE}	$\overline{CE}$ active to Write End	7		8		ns
t_{AW}	Address Set-Up to Write End	7		8		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		ns
t_{SD}	Data Set-Up to Write End	5.5		6		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		5		6	ns
t_{BW}	Byte Enable to End of Write	7		8		ns

Data Retention Characteristics Over the Operating Range

| Parameter	Description		Conditions[12]	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	Com'l / Ind'l	$V_{CC} = V_{DR} = 2.0V$,		100	mA
t_{CDR}[2]	Chip Deselect to Data Retention Time		$\overline{CE} \geq V_{CC} - 0.3V$	0		ns
t_R[11]	Operation Recovery Time		$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$			µs

Notes:
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and specified transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
5. $\overline{CE}$ indicates a combination of both chip enables. When ACTIVE LOW, $\overline{CE}$ indicates the $\overline{CE_1}$ is LOW and CE_2 is HIGH.
6. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
7. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE} and t_{LZOE}, t_{LZCE}, $t_{\backslash LZWE}$, t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
8. These parameters are guaranteed by design and are not tested.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
11. Test conditions assume $t_r \leq 3$ ns.
12. No input may exceed $V_{CC} + 0.3V$.

Data Retention Waveform
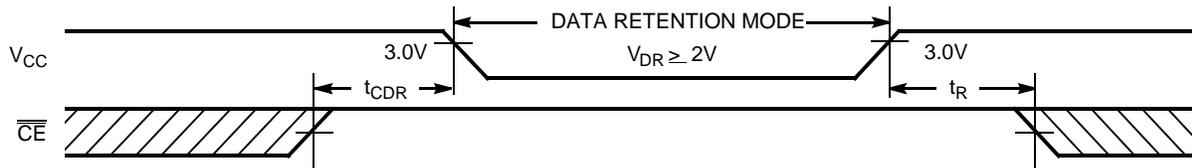
Switching Waveforms

Read Cycle No. 1[13, 14]
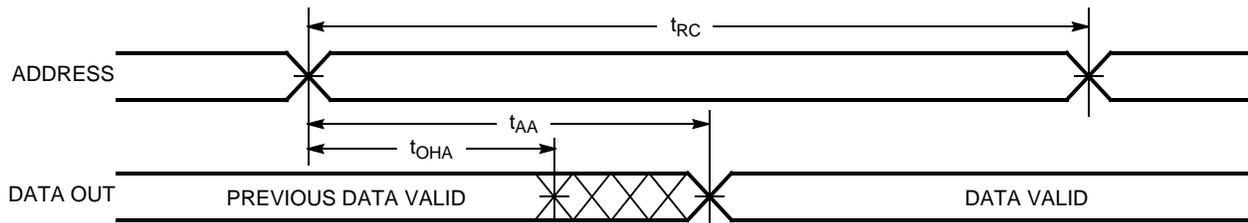
Read Cycle No. 2 ($\overline{OE}$ Controlled)[14, 15]
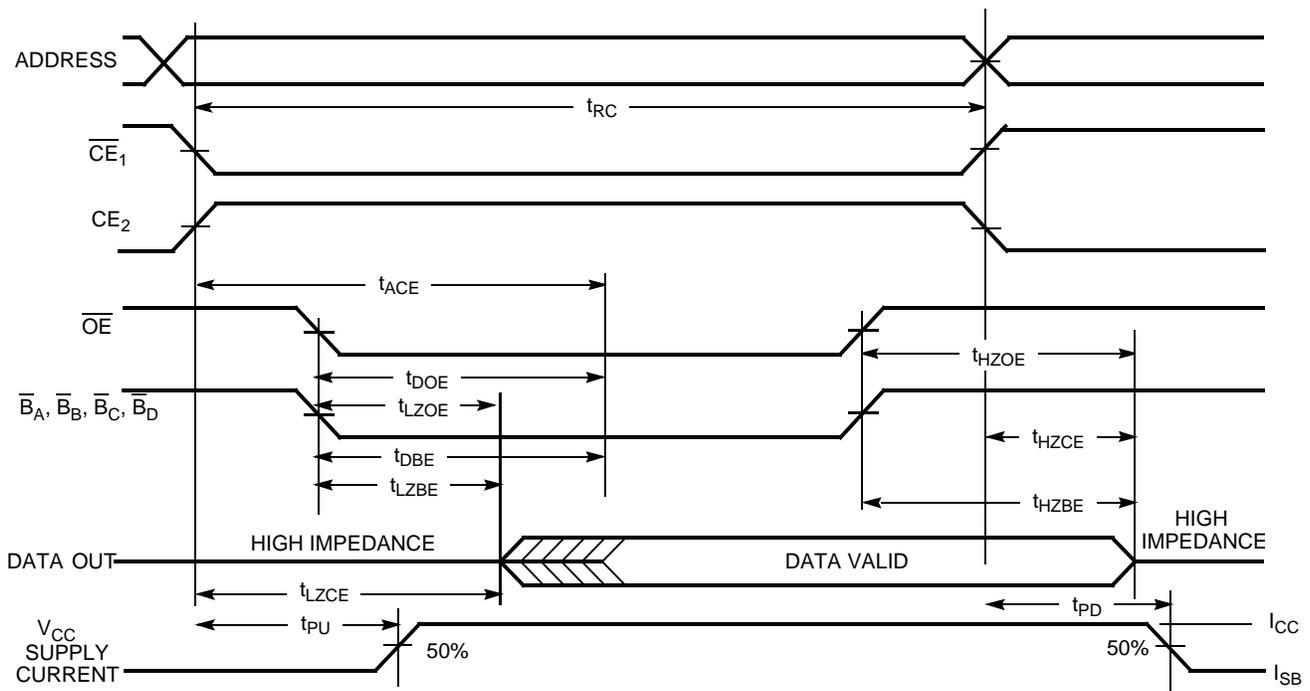
Notes:
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1$, $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D = V_{IL}$, $CE_2 = V_{IH}$
14. $\overline{WE}$ is HIGH for read cycle.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW, CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[5, 16, 17]
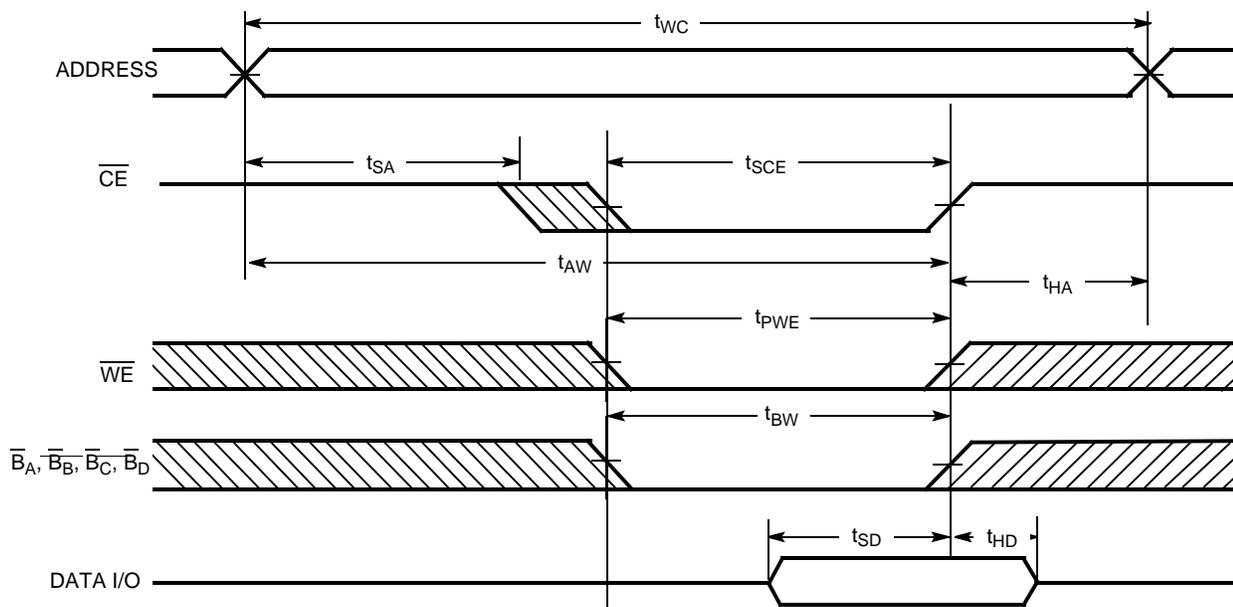
Write Cycle No. 2 ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ Controlled)[5, 16, 17]
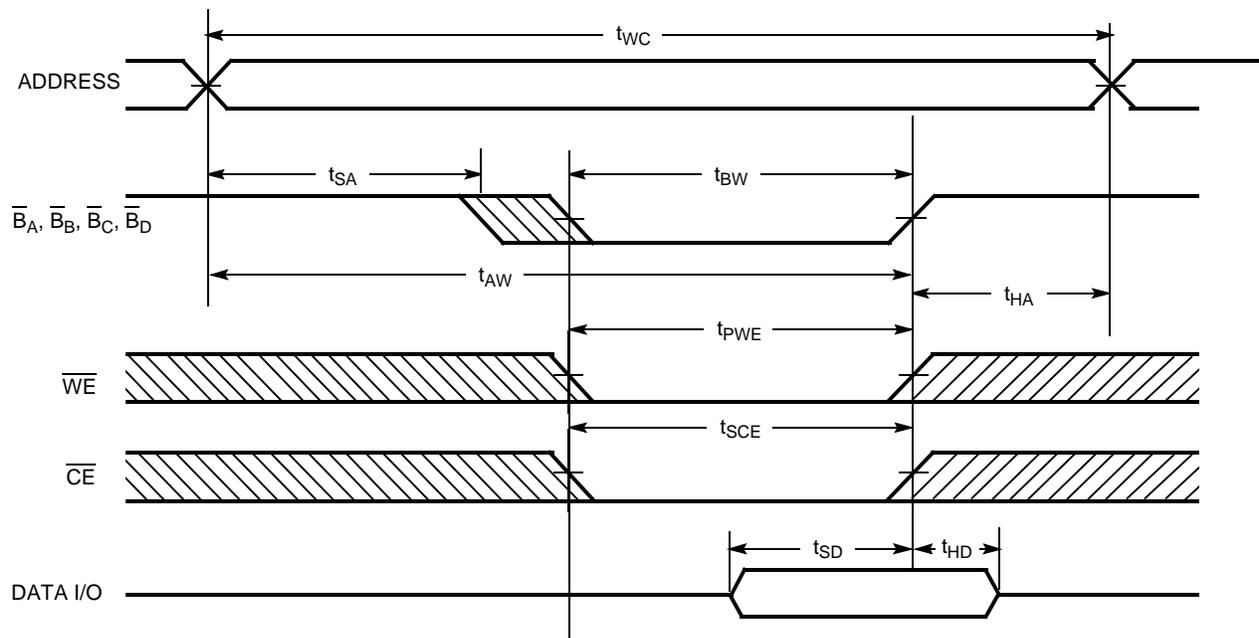
Notes:
16. Data I/O is high impedance if $\overline{OE} = V_{IH}$ or $\overline{B}_A/\overline{B}_B/\overline{B}_C/\overline{B}_D = V_{IH}$
17. If $\overline{CE}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)[5, 16, 17]
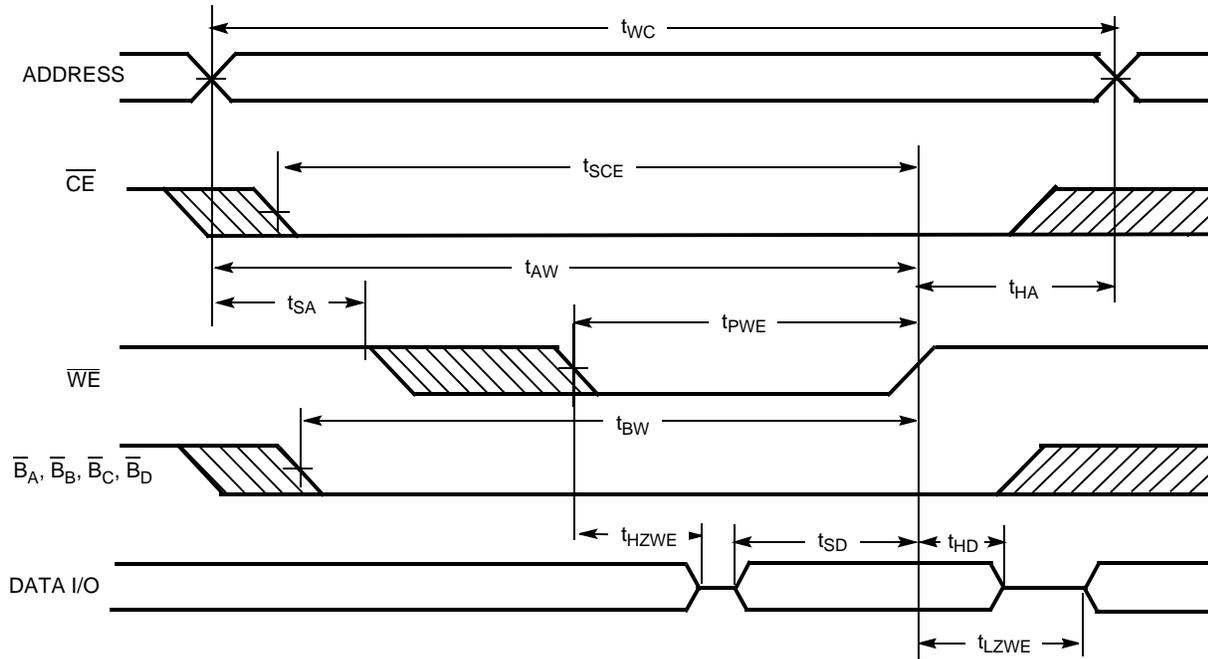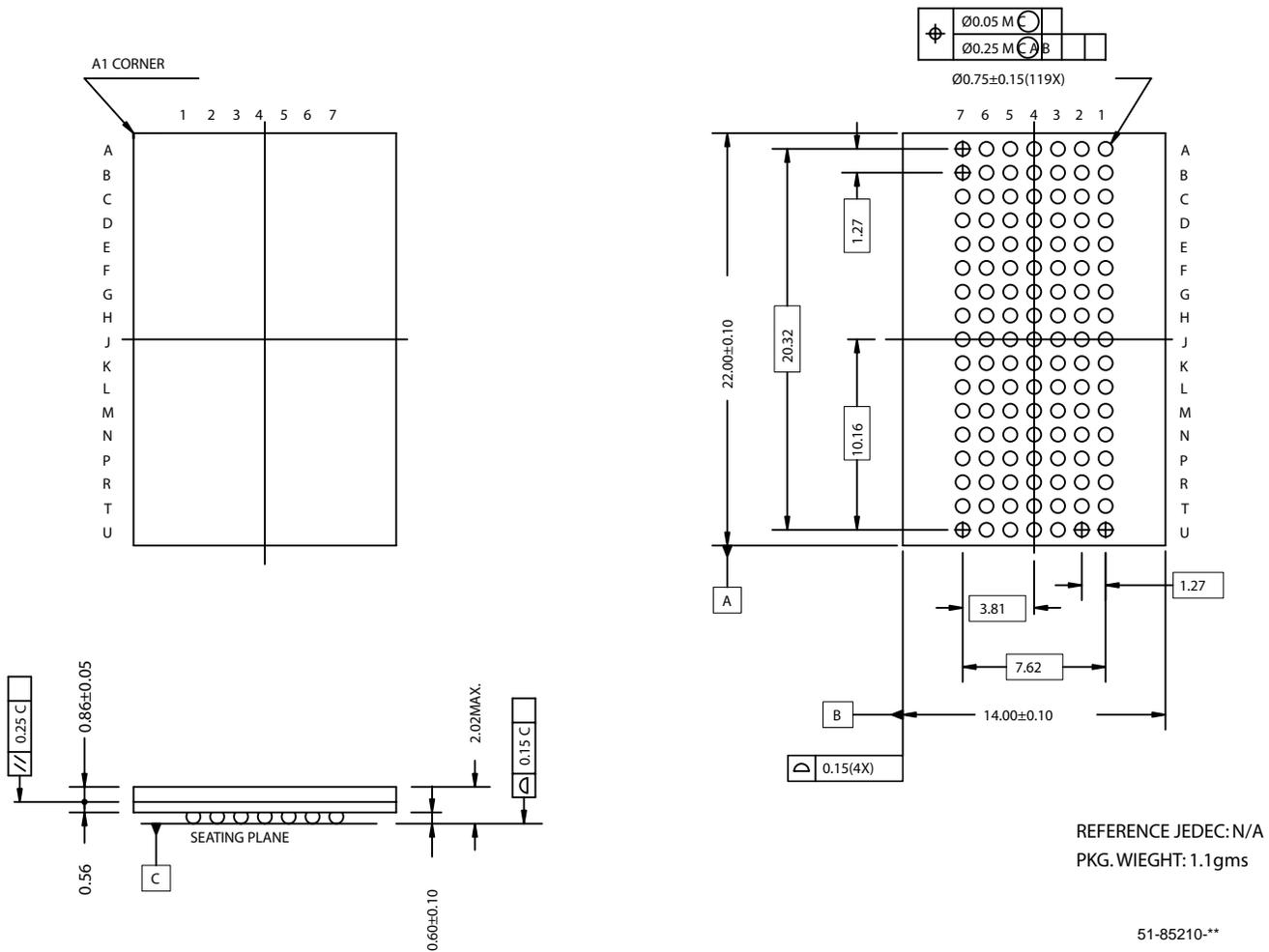

Truth Table

$\overline{\text{CE}_1}$	CE_2	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{B}_A}$	$\overline{\text{B}_B}$	$\overline{\text{B}_c}$	$\overline{\text{B}_D}$	I/O$_0$–I/O$_7$	I/O$_8$–I/O$_{15}$	I/O$_{16}$–I/O$_{23}$	I/O$_{24}$–I/O$_{31}$	Mode	Power
H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I_{SB})
X	L	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I_{SB})
L	H	L	H	L	L	L	L	Data Out	Data Out	Data Out	Data Out	Read All Bits	(I_{CC})
L	H	L	H	L	H	H	H	Data Out	High-Z	High-Z	High-Z	Read Byte A Bits Only	(I_{CC})
L	H	L	H	H	L	H	H	High-Z	Data Out	High-Z	High-Z	Read Byte B Bits Only	(I_{CC})
L	H	L	H	H	H	L	H	High-Z	High-Z	Data Out	High-Z	Read Byte C Bits Only	(I_{CC})
L	H	L	H	H	H	H	L	High-Z	High-Z	High-Z	Data Out	Read Byte D Bits Only	(I_{CC})
L	H	X	L	L	L	L	L	Data In	Data In	Data In	Data In	Write All Bits	(I_{CC})
L	H	X	L	L	H	H	H	Data In	High-Z	High-Z	High-Z	Write Byte A Bits Only	(I_{CC})
L	H	X	L	H	L	H	H	High-Z	Data In	High-Z	High-Z	Write Byte B Bits Only	(I_{CC})
L	H	X	L	H	H	L	H	High-Z	High-Z	Data In	High-Z	Write Byte C Bits Only	(I_{CC})
L	H	X	L	H	H	H	L	High-Z	High-Z	High-Z	Data In	Write Byte D Bits Only	(I_{CC})
L	H	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Selected, Outputs Disabled	(I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1072AV33-10 BBC	BB119	119-Ball (14 x 22 x 2.02 mm) FBGA	Commercial
	CY7C1072AV33-10 BBI			Industrial
12	CY7C1072AV33-12 BBC	BB119	119-Ball (14 x 22 x 2.02 mm) FBGA	Commercial
	CY7C1072AV33-12 BBI			Industrial

Package Diagrams

119 FBGA (14 x 22 x 2.02 MM) BB119B

REFERENCE JEDEC: N/A

PKG. WIEGHT: 1.1gms

51-85210-**

Document History Page

Document Title: CY7C1072AV33 32-Mbit (1M x 32) Static RAM Module Document Number: 38-05635				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	278072	See ECN	RKF	New Data Sheet
*A	397700	See ECN	SYT	Converted from "Advance Information" to "Preliminary" Changed the MPN from CYM1072AV33 to CY7C1072AV33 Changed Title from "CY7C1072AV33 32-Mbit (1M x 32) Static RAM Module" to "CY7C1072AV33 32-Mbit (1M x 32) Static RAM" Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Removed redundant information from the "Features" and "Functional Description" sections Changed Package offering from 119 PBGA (BG119) to 119 FBGA (BB119) Changed the DC Voltage Applied to Outputs in High-Z State and DC Input Voltage from "-0.5V to V_{CC} + 0.5V" to "-0.3V to V_{CC} + 0.3V" in the Maximum Ratings on Page # 3 Changed V_{CC} from "3.3V +5%" to "3.3V + 0.3V" in the Operating Range table on Page # 3 Edited Test Conditions for I_{SB1} and I_{SB2} in the Electrical Characteristics table on Page # 3 Changed t_{DBE} from 5 ns to 10 ns and 6 ns to 12 ns for -10 and -12 speed bins respectively on Page # 4 Moved footnote #15 to footnote # 5 Included spec for I_{CCDR} = 100 mA in the Data Retention Characteristics table on Page# 5 Edited footnote # 12 from "V_{CC} + 0.5V" to "V_{CC} + 0.3V" Edited footnote # 13 to include "CE_2 = V_{IH} " Edited footnote # 15 to include "$\overline{CE_2}$ transition HIGH" Edited footnote # 16 to include "$\overline{B}_A/\overline{B}_B/\overline{B}_C/\overline{B}_D$ = V_{IH} " Edited footnote # 17 to include "CE_2 goes LOW" Corrected typo on footnote #16 Referenced Footnotes # 5, 16 and 17 on to the Write Cycle No.3 on Page # 7 Corrected Truth table on Page #9 Updated the Ordering Information to include the BB119 Package