FAIRCHILD SEMICONDUCTOR®

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FDMF6730
Driver plus FET Multi-chip Module

Features

- Over 95% efficiency
- Internal 5V regulator for gate drive
- 6V-16V input range
- 1MHz max operating frequency
- SMOD operation capability for light load efficiency
- 5A current capability (10A with PASS FET)
- Current limit set by R_{DSON} sensing to minimize power losses
- Integrated bootstrap diode

Applications

- Ultra Mobile PC
- Notebook Computers

General Description

The FDMF6730 is a high efficiency Driver plus MOSFET power stage solution optimized for Ultra Mobile PC (UMPC) system power voltage supplies. It is fully compliant with the Intel Ultra-Mobile Driver MOS (uDrMOS) Specification. The MOSFETs and driver have been optimized to perform with high efficiency at light and medium loads, ideal for compact PC devices.

The internal driver IC integrates two highly efficient LDOs for internal gate-drive and external circuitry. The bootstrap diode is also integrated within the IC. When operating with a single low side MOSFET the uDrMOS module is capable of delivering up to 5A of continuous current. The PASS transistor may be easily routed in parallel with the low side MOSFET to provide up to 10A. The module also incorporates an over current protection flag from an R_{DSON} current sense architecture.

The device comes in a 6X6 Power QFN package for improved thermal performance.

Typical Application

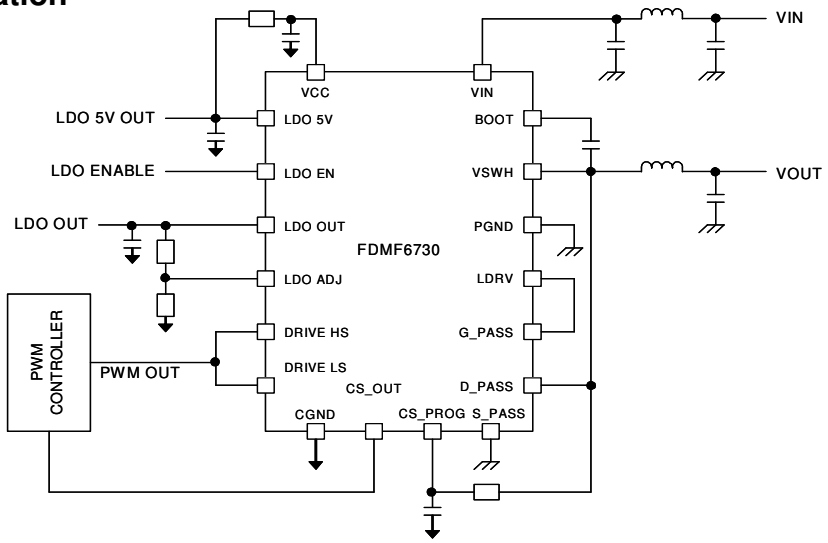


Figure 1. Power Train Application Circuit

Ordering Information

Part	Current Rating Max [A]	Input Voltage Typical [V]	Frequency Max [KHz]	Device Marking
FDMF6730	10	6-16	1000	FDMF6730

Functional Block Diagram

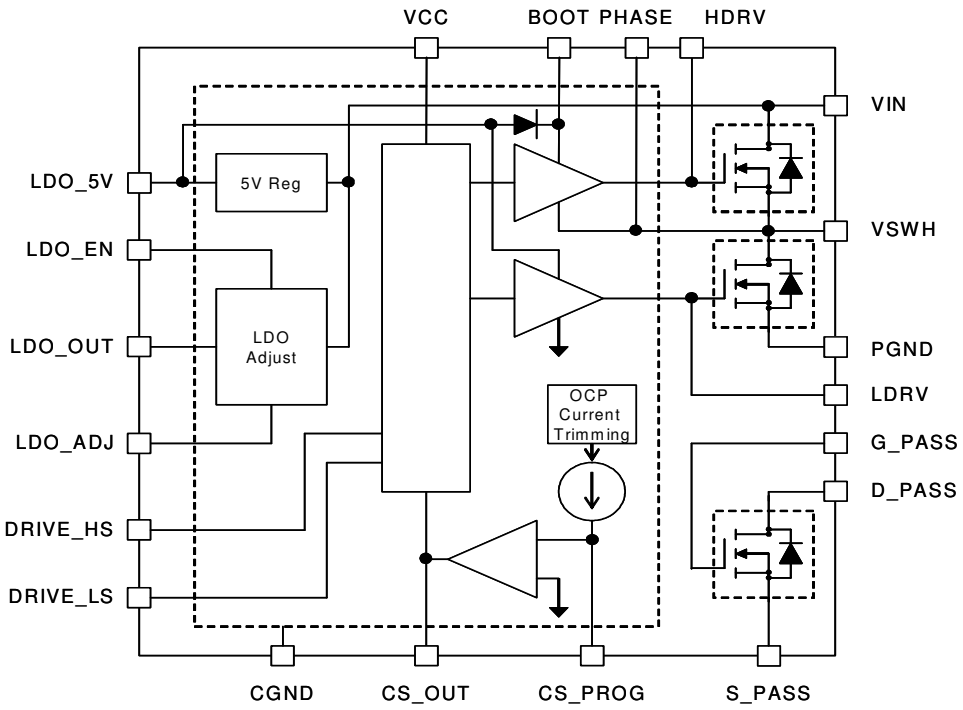


Figure 2. Functional Block Diagram

Pin Configuration

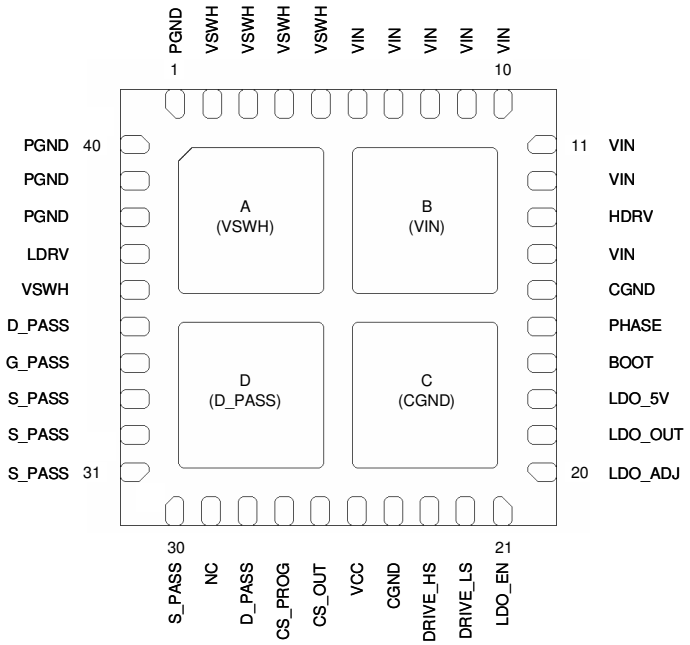


Figure 3. 6mm X 6mm, 40L MLP Bottom View

Pin Description

Pin	Name	Function
1, 38 - 40	PGND	Low Side FET Source Pin. Connect to GND
2 - 5, 36, A	VSWH	Switch Node Pin. Low Side FET Drain pin. Electrically shorted to PHASE pin
6 - 12,14,B	VIN	Input Voltage Pin. Input voltage for buck converter
13	HDRV	HDRV pin. High Side driver output. Connected to High Side FET gate pin.
15, 24, C	CGND	IC Ground. Ground return for driver IC.
16	PHASE	Switch Node Pin for easy bootstrap capacitor routing. Electrically shorted to VSWH pin.
17	BOOT	Bootstrap Supply Input Pin. Provides voltage supply to high-side MOSFET driver. Connect bootstrap capacitor.
18	LDO_5V	5V Internal LDO Output.
19	LDO_OUT	Adjustable LDO Output.
20	LDO_ADJ	LDO Adjust Input. Connect to external voltage divider to adjust LDO output.
21	LDO_EN	Adjustable LDO Enable Pin. 1 = Enable, 0 = Disable
22	DRIVE_LS	Low Side PWM Input. Connect to PWM controller.
23	DRIVE_HS	High Side PWM Input. Connect to PWM controller.
25	VCC	Driver VCC. Connect to 5V.
26	CS_OUT	Current Sense Output. 1 = Over-current Fault, 0 = No Fault.
27	CS_PROG	Current Sense Program.
28, 35, D	D_PASS	Pass FET Drain Pin. Connect to VSWH pad for higher output current.
29	NC	No Connect. This pin must be floated. Must not be connected to any pin.
30-33	S_PASS	Pass FET Source Pin. Connect to PGND pad for higher output current.
34	G_PASS	Pass FET Gate Pin. Connect to LDRV pin for higher output current.
37	LDRV	LDRV pin. Low Side driver output. Connect to G_PASS pin for higher output current.

Absolute Maximum Rating

Stresses exceeding the absolute maximum rating may damage the device. The device may not function or be operable above the recommended operating conditions and stressing these parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect the device reliability. The absolute maximum rating are stress ratings only.

Parameter		Min.	Max.	Units
V_{CC}, Drive_LS, Drive_HS, LDO_EN, CS_Prog, CS_Out to GND		-0.3	6	V
V_{IN} to PGND		-0.3	20	V
BOOT to VSWH		-0.3	6	V
VSWH to PGND		-1.0	27	V
BOOT to PGND		-0.3	27	V
$I_{O(AV)}$	V_{IN} = 8.4V, V_O = 3.3V, f_{SW} = 1MHz, T_{PCB} = 130°C		10	A
$I_{O(PK)}$	V_{IN} = 8.4V, t_{PULSE} = 10µs		35	A
$R_{\theta JPCB}$	Junction to PCB Thermal Resistance note 1. T_{PCB} =130°C		5.5	°C/W
P_T			3.3	W
Operating and Storage Junction Temperature Range		-55	150	°C

Note 1: Package power dissipation based on 4 layer, 2 square inch, 2 oz. copper pad. $R_{\theta JPCB}$ is the steady state junction to PCB thermal resistance with PCB temperature referenced at VSWH pin.

Recommended Operating Range

The recommended operating conditions table defines the conditions for actual device operation. These conditions are specified to ensure optimal performance to the datasheet specification. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Parameter		Min.	Typ.	Max.	Units
V_{CC}	Control Circuit Supply Voltage	4.5	5	5.5	V
V_{IN}	Output Stage Supply Voltage	6	8.4	16	V
V_{OUT}	Output Voltage	1.5	3.3	5	V

Electrical Characteristics

V_{IN} = 8.4V, V_{CC} = 5V, T_A = 25°C unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Voltage Range	V_{IN}		6		16	V
Operating Quiescent Current					2	mA
Drive_HS, Drive_LS, LDO_EN Logic Inputs						
High Level Input	V_{IH}		2.4			V
Low Level Input	V_{IL}				0.4	V
Input Current			-2		2	µA
5V LDO						
Output Voltage			4.7	5	5.3	V
Line Regulation		6V < V_{IN} < 16V		5		mV
Load Regulation		5mA < I_{LOAD} < 100mA		75		mV
Short Circuit Current Limit			100	180		mA
Adjustable LDO						
Adjust Voltage	V_{ADJ}		0.58	0.6	0.62	V
Line Regulation		6V < V_{IN} < 16V		3		mV
Load Regulation		5mA < I_{LOAD} < 100mA		11		mV
Short Circuit Current Limit			100	180		mA
Adjust Input Bias Current					0.2	µA
Over Current Protection						
CS_Prog Current			30	40	50	µA
Thermal Shutdown						
Threshold				150		°C
Hysteresis				19		°C
Propagation Delay						
250ns Timeout	$t_{TIMEOUT}$	VSWH = 2V, HDRV from HI to LO and LDRV from LO to HI		250		ns
	t_{DTHH}	LDRV going LO to VSWH going HI		30		ns
	t_{PDHL}	Drive_LS going HI to HDRV going LO		10		ns
	t_{DTLH}	VSWH going LO to LDRV going HI		20		ns
	t_{PDLL}	Drive_LS going LO to LDRV going LO		10		ns

Description of Operation

2-Bit PWM Input

The PWM input is composed of a high side drive and a low side drive input which control the high side and low side FETs respectively. They can also be setup to provide asynchronous rectification (low FET off) and phase shutoff (both FETs off).

Truth Table

DRIVE_LS	DRIVE_HS	Low Side MOSFET	High Side MOSFET
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	OFF	OFF

PASS FET

One of the most unique features of the uDrMOS is the integrated Pass FET. The pass FET can be easily routed in parallel with the low side FET in order to provide up to 10A of current. When not used as part of the DC-DC controller, it can be used in other applications such as load switching, etc.

5V LDO

The uDrMOS conveniently incorporates a 5V LDO regulator to drive the internal logic of the IC and gates of the internal MOSFETs.

Adjustable LDO

Another feature of the part is the adjustable 100mA LDO. The LDO output voltage is easily configured with a resistor divider.

Current Limit

The part also has current limit flag which is set by an internal OCP topology.

Applications Section

Input Capacitor

A High frequency 4.7ceramic X5R must be connected directly from V_{IN} to GND

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor and an external diode. A minimum of 0.1µF high frequency capacitor must be connected between the BOOT and PHASE pin. The PHASE pin is already internally connected to the switch-node.

5V LDO

A minimum of 4.7µF ceramic X5R type must be connected from LDO_5V pin to GND to ensure stable operation and to provide high frequency bypassing for low side driver. This LDO can provide power to the internal logic circuitry and gate drivers via a 10Ohm resistor. A high frequency 1µF ceramic capacitor must be placed from V_{CC} to GND.

Adjustable LDO

A minimum of 10µF ceramic X5R type must be connected close from this pin to GND to insure stable operation for a range of 2.5V to 5V outputs. For output voltages of 0.6V to 2.5V the minimum capacitance must be 22µF ceramic type. A minimum of 1mA load current must be connected from this pin to GND. LDO_ADJ voltage 0.6V typical.
LDO_EN: Adjustable LDO enable pin (1= Enable, 0= Disable)

Over Current Protection

A resistor connected from the VSWH pin and this pin programs the over current threshold point. CS_OUT is the output of an internal current sense comparator which switches high when the current in low side MOSFET exceeds a pre program level set by the CS_PROG pin. This pin is low during normal operation.

Typical Characteristics

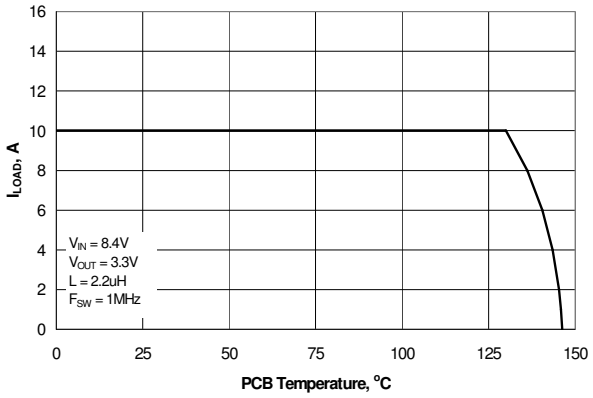


Figure 4. Safe Operating Area

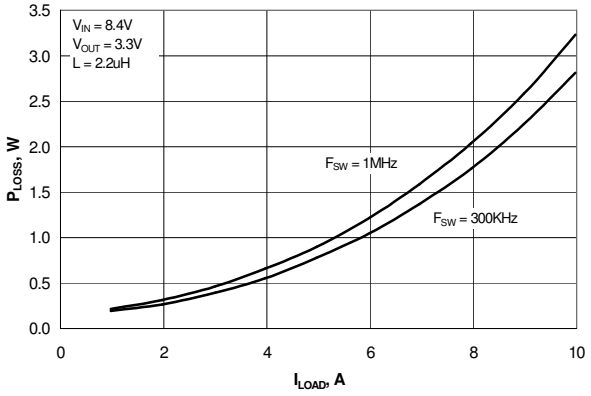


Figure 5. Power Loss vs. Output Current

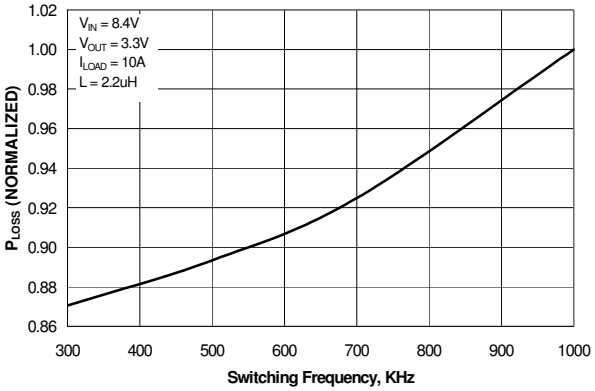


Figure 6. Power Loss vs. Switching Frequency

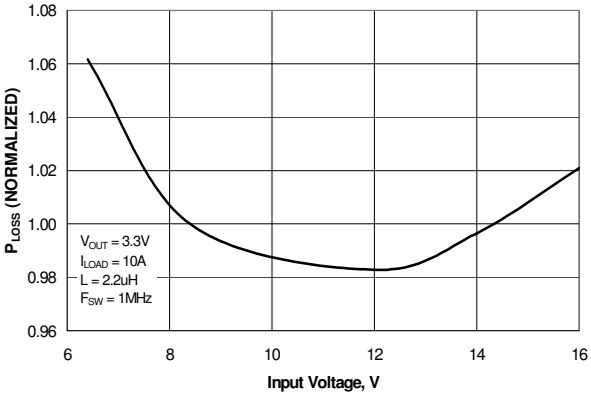


Figure 7. Power Loss vs. Input Voltage

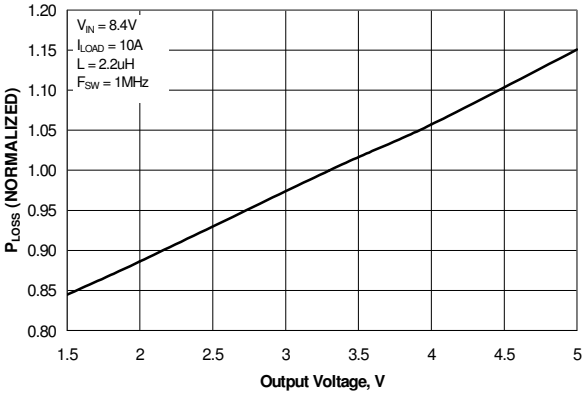


Figure 8. Power Loss vs. Output Voltage

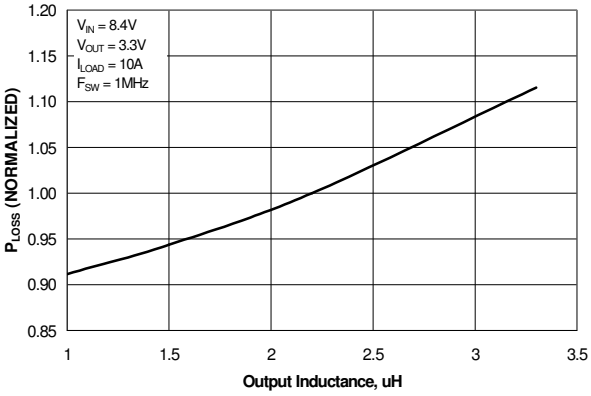


Figure 9. Power Loss vs. Output Inductance

Typical Characteristics

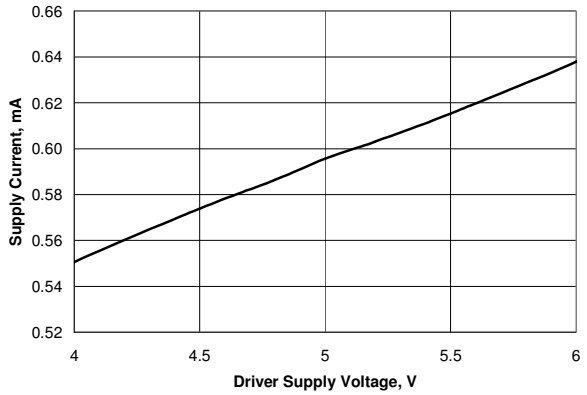


Figure 10. Supply Current vs. Driver Supply

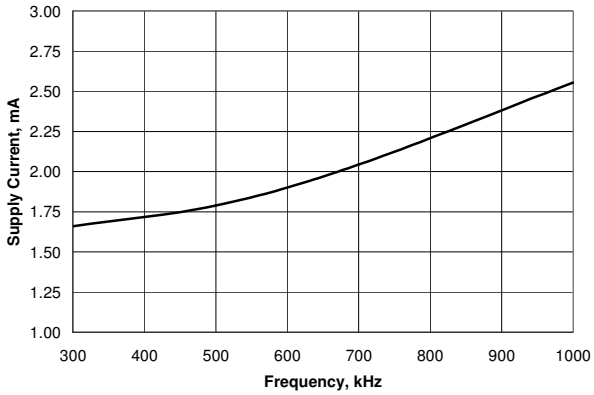


Figure 11. Supply Current vs. Frequency

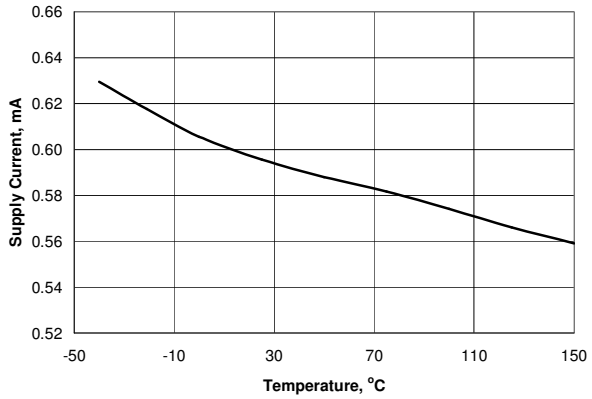


Figure 12. Supply Current vs. Temperature

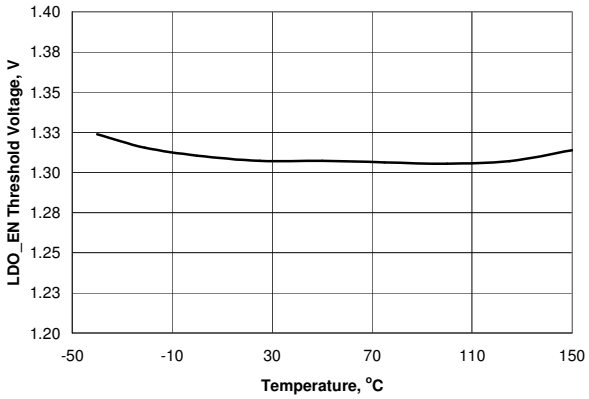


Figure 13. LDO_EN Threshold Voltage vs. Temperature

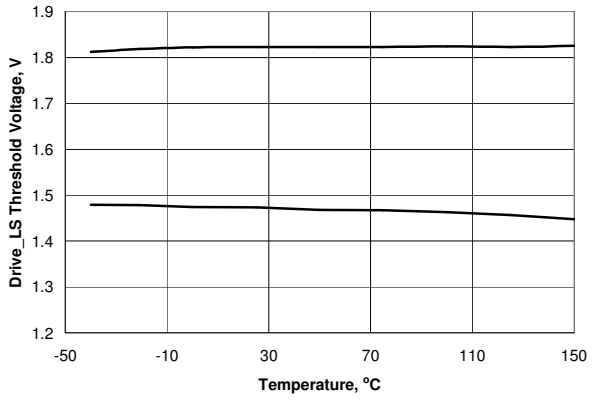


Figure 14. Driver_LS Threshold Voltage vs. Temperature

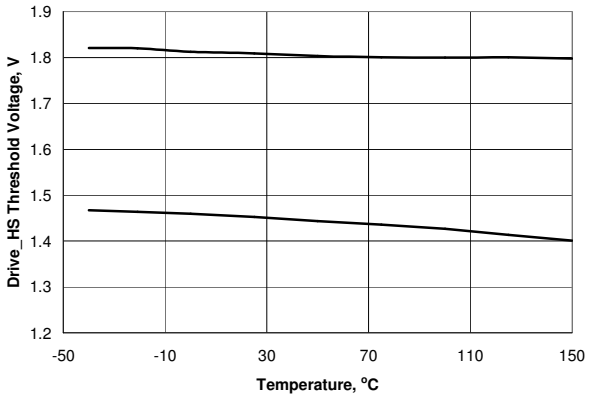


Figure 15. Driver_HS Threshold Voltage vs. Temperature

Typical Characteristics

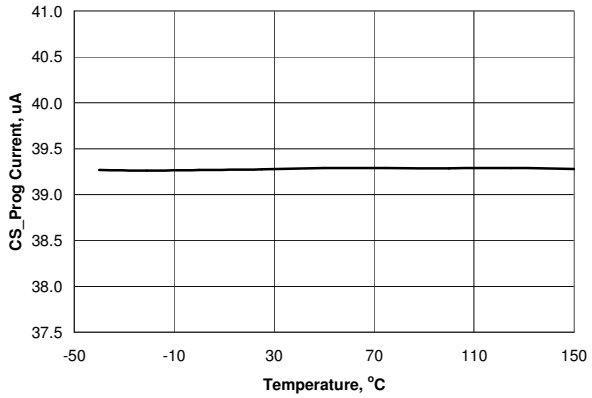
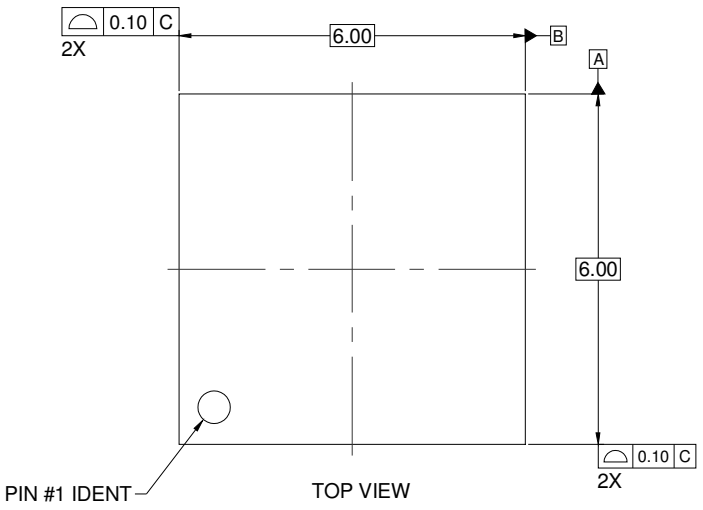
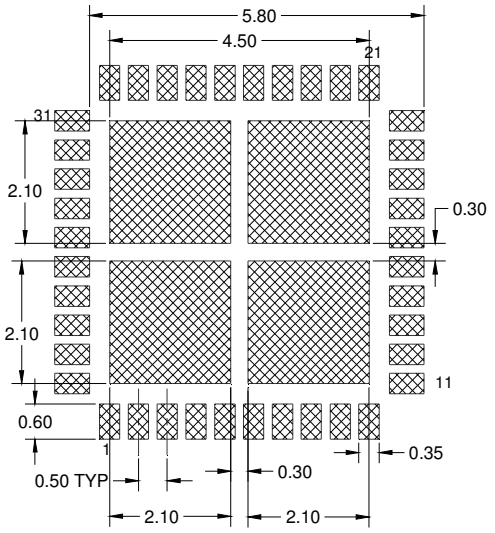


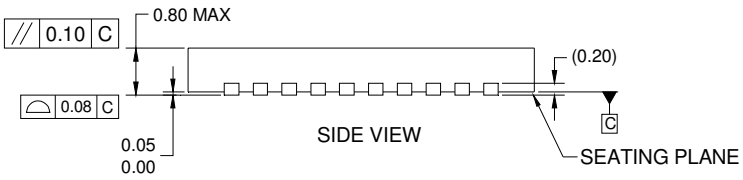
Figure 16. CS_Prog Current vs. Temperature

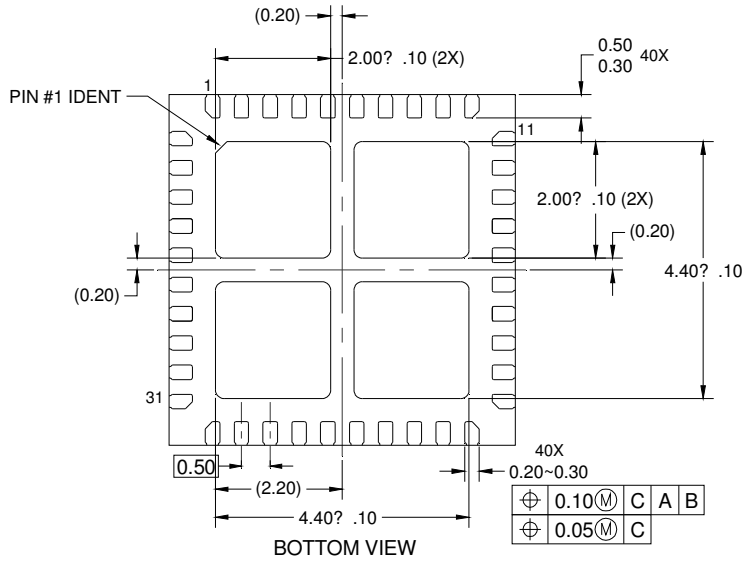
Dimensional Outline and Pad layout





RECOMMENDED LAND PATTERN





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