

## DESCRIPTION

The M5M5V208AKV is low voltage 2-Mbit static RAMs organized as 262,144-words by 8-bit, fabricated by high-performance 0.25 $\mu$ m CMOS technology.

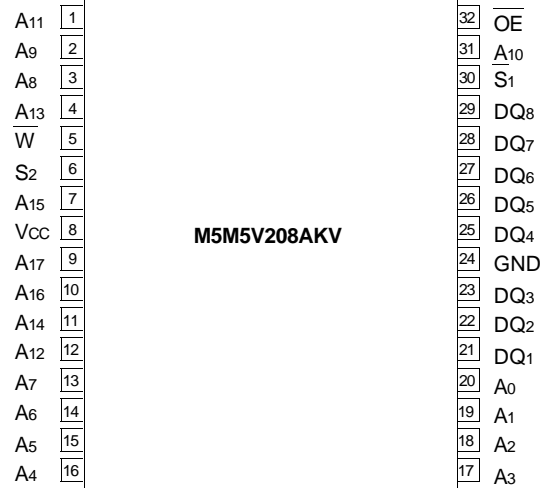
The M5M5V208AKV is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

The M5M5V208AKV is packaged in 32-pin 8mm x 13.4mm sTSSOP packages which is a high reliability and high density surface mount device.

## FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	stand-by (max)
M5M5V208AKV-55HI	55ns	35mA (10MHz)	30 $\mu$ A (V <sub>CC</sub> =3.6V)
M5M5V208AKV-70HI	70ns	7mA (1MHz)	0.3 $\mu$ A (V <sub>CC</sub> =3.0V TYPICAL)

## PIN CONFIGURATION (TOP VIEW)



Outline 32P3K-B(KV)

- Single 2.7 ~3.6V power supply
- No clock, No refresh
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by S1,S2
- Data hold on +2V power supply
- Three-state outputs : OR - tie capability
- OE prevents data contention in the I/O bus
- Common data I/O
- Package

M5M5V208AKV ..... 32pin 8 X 13.4 mm<sup>2</sup> sTSSOP



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage	With respect to GND	- 0.5*~4.6	V
V <sub>I</sub>	Input voltage		- 0.5*~V <sub>CC</sub> + 0.3	V
V <sub>O</sub>	Output voltage		0~V <sub>CC</sub>	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25°C	700	mW
T <sub>opr</sub>	Operating temperature		- 40~85	°C
T <sub>stg</sub>	Storage temperature		- 65~150	°C

\* -3.0V in case of AC ( Pulse width ≤ 30ns )

**DC ELECTRICAL CHARACTERISTICS** (T<sub>a</sub>= -40~85°C, V<sub>CC</sub>=2.7~3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>IH</sub>	High-level input voltage		2.0		V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Low-level input voltage		-0.3*		0.6	V
V <sub>OH1</sub>	High-level output voltage 1	I <sub>OH</sub> = - 0.5mA	2.4			V
V <sub>OH2</sub>	High-level output voltage 2	I <sub>OH</sub> = - 0.05mA	V <sub>CC</sub> - 0.5			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 2mA			0.4	V
I <sub>I</sub>	Input current	V <sub>I</sub> =0~V <sub>CC</sub>			±1	μA
I <sub>O</sub>	Output current in off-state	S <sub>1</sub> =V <sub>IH</sub> or S <sub>2</sub> =V <sub>IL</sub> or OE=V <sub>IH</sub> V <sub>I/O</sub> =0~V <sub>CC</sub>			±1	μA
I <sub>CC1</sub>	Active supply current (CMOS-level input)	S <sub>1</sub> ≤ 0.2V, S <sub>2</sub> ≥ V <sub>CC</sub> -0.2V other inputs ≤ 0.2V or ≥ V <sub>CC</sub> -0.2V, Output-open	10MHz	28	30	mA
			1MHz	5	7	
I <sub>CC2</sub>	Active supply current (TTL-level input)	S <sub>1</sub> =V <sub>IL</sub> , S <sub>2</sub> =V <sub>IH</sub> , other inputs=V <sub>IH</sub> or V <sub>IL</sub> , Output-open	10MHz	33	35	mA
			1MHz	5	7	
I <sub>CC3</sub>	Stand-by current	1) S <sub>2</sub> ≤ 0.2V, other inputs=0 ~ V <sub>CC</sub> 2) S <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V, S <sub>2</sub> ≥ V <sub>CC</sub> - 0.2V other inputs=0 ~ V <sub>CC</sub>	~25°C	0.3	2	μA
			~40°C		5	
			~70°C		10	
			~85°C		30	
I <sub>CC4</sub>	Stand-by current	1) S <sub>1</sub> =V <sub>IH</sub> , other inputs=V <sub>IL</sub> or V <sub>IH</sub> 2) S <sub>2</sub> =V <sub>IL</sub> , other inputs=V <sub>IL</sub> or V <sub>IH</sub>			0.33	mA

\* -3.0V in case of AC ( Pulse width ≤ 30ns )

**CAPACITANCE** (T<sub>a</sub>= -40~85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>I</sub>	Input capacitance	V <sub>I</sub> =GND, V <sub>I</sub> =25mVrms, f=1MHz			8	pF
C <sub>O</sub>	Output capacitance	V <sub>O</sub> =GND, V <sub>O</sub> =25mVrms, f=1MHz			10	pF

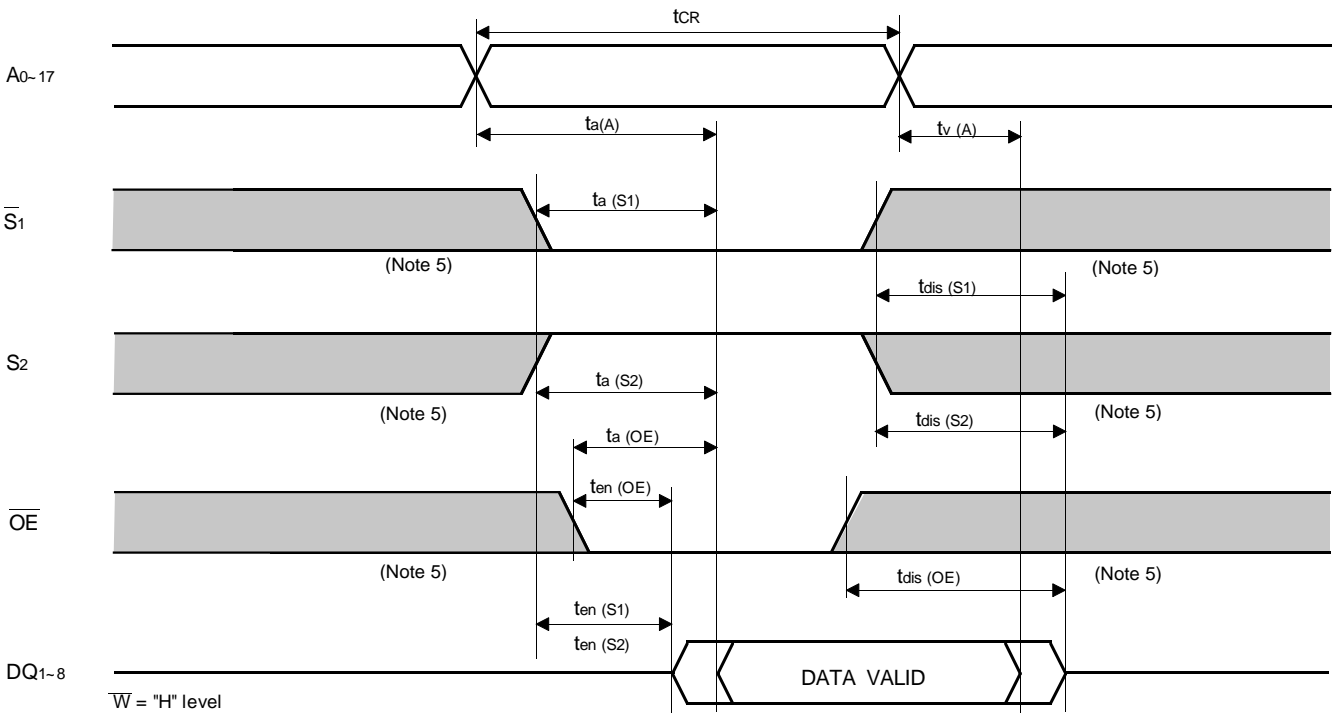
Note 3: Direction for current flowing into an IC is positive (no mark).

4: Typical value is V<sub>CC</sub> = 3V, T<sub>a</sub> = 25°C

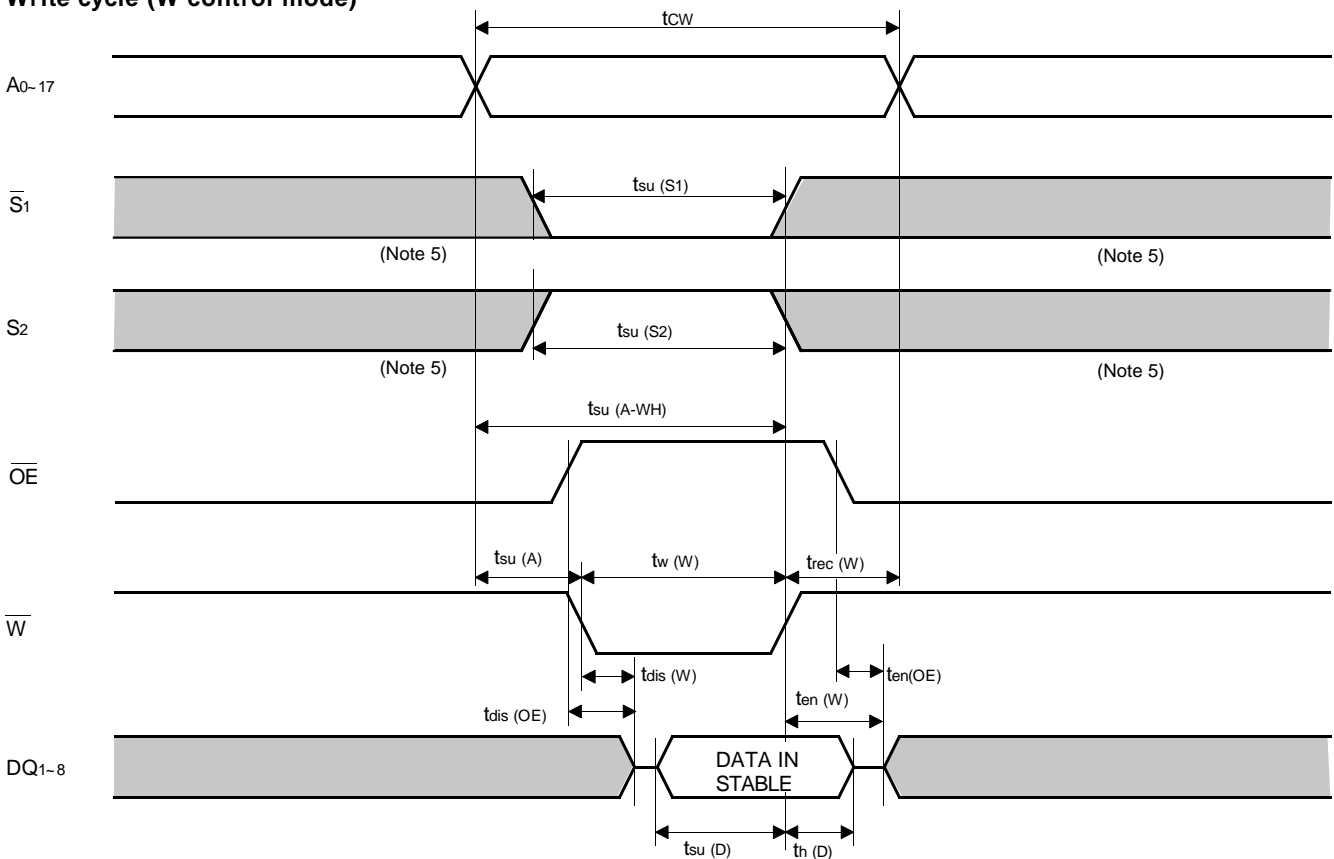


(4) TIMING DIAGRAMS

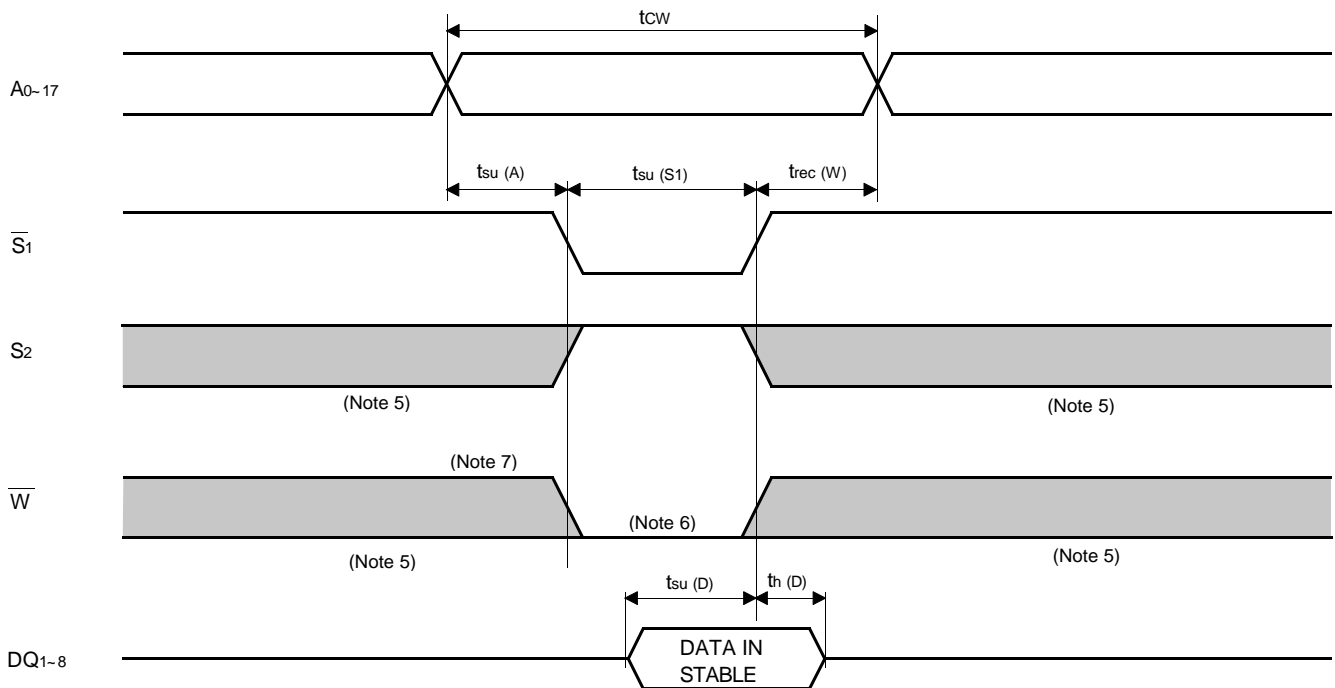
Read cycle



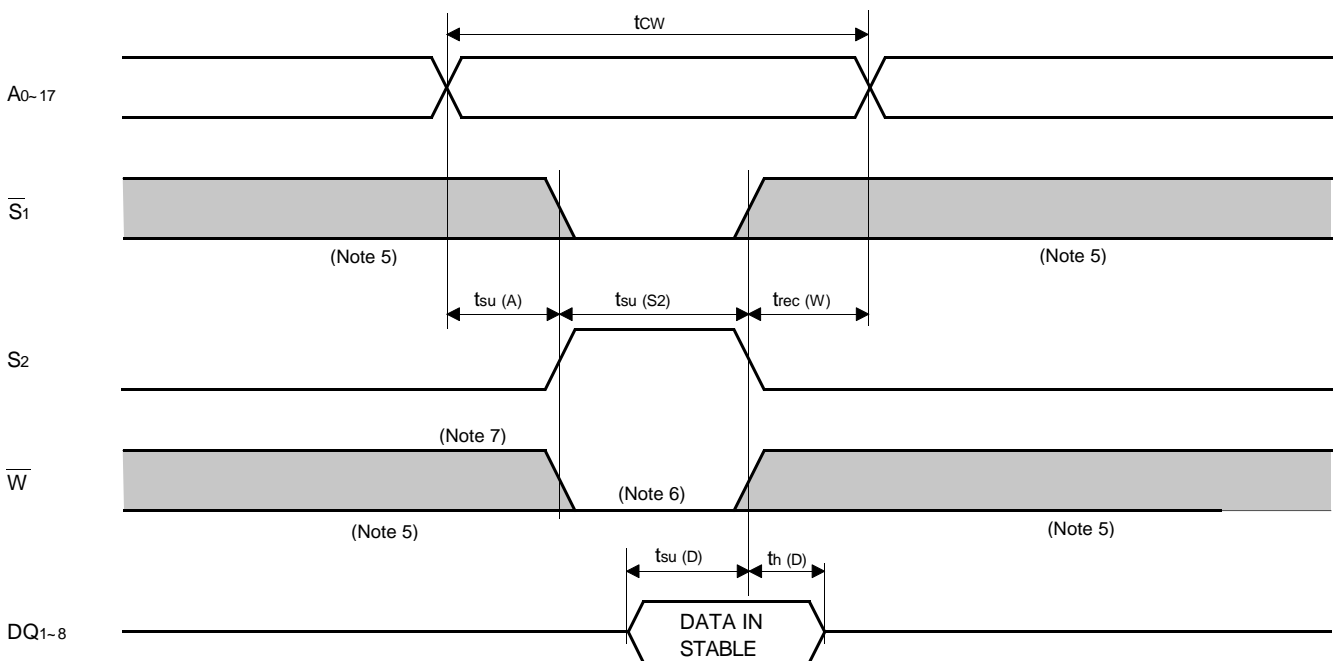
Write cycle ( $\overline{W}$  control mode)



Write cycle ( $\overline{S1}$  control mode)



Write cycle (S2 control mode)



- Note 5: Hatching indicates the state is "don't care".  
 6: Writing is executed while S2 high overlaps  $\overline{S1}$  and  $\overline{W}$  low.  
 7: When the falling edge of  $\overline{W}$  is simultaneously or prior to the falling edge of  $\overline{S1}$  or rising edge of S2, the outputs are maintained in the high impedance state.  
 8: Don't apply inverted phase signal externally when DQ pin is output mode.

**POWER DOWN CHARACTERISTICS**

**(1) ELECTRICAL CHARACTERISTICS** (T<sub>a</sub>= -40~85°C, unless otherwise noted)

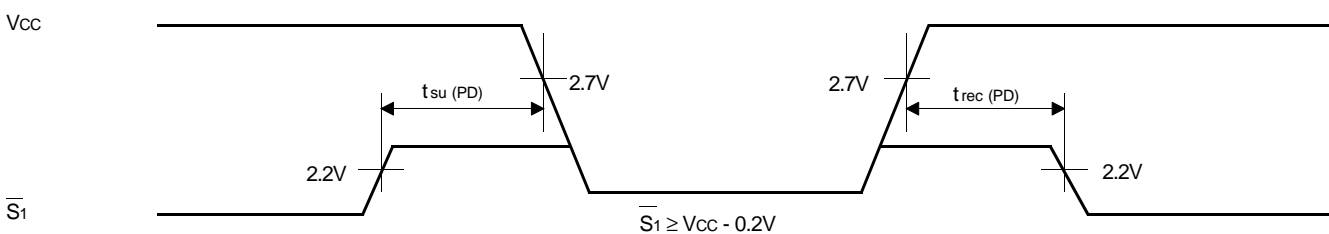
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>CC</sub> (PD)	Power down supply voltage		2.0			V
V <sub>I</sub> (S1)	Chip select input $\overline{S1}$		2.0			V
V <sub>I</sub> (S2)	Chip select input S2				0.2	V
I <sub>CC</sub> (PD)	Power down supply current	V <sub>CC</sub> = 3.0V 1) S <sub>2</sub> ≤ 0.2V, other inputs = 0~V <sub>CC</sub> 2) $\overline{S1} \geq V_{CC}-0.2V$ , S <sub>2</sub> ≥ V <sub>CC</sub> -0.2V, other inputs = 0~V <sub>CC</sub>	~25°C	0.3	1	μA
			~40°C		3	
			~70°C		8	
			~85°C		24	

**(2) TIMING REQUIREMENTS** (T<sub>a</sub>=-40~85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t <sub>su</sub> (PD)	Power down set up time		0			ns
t <sub>rec</sub> (PD)	Power down recovery time		5			ms

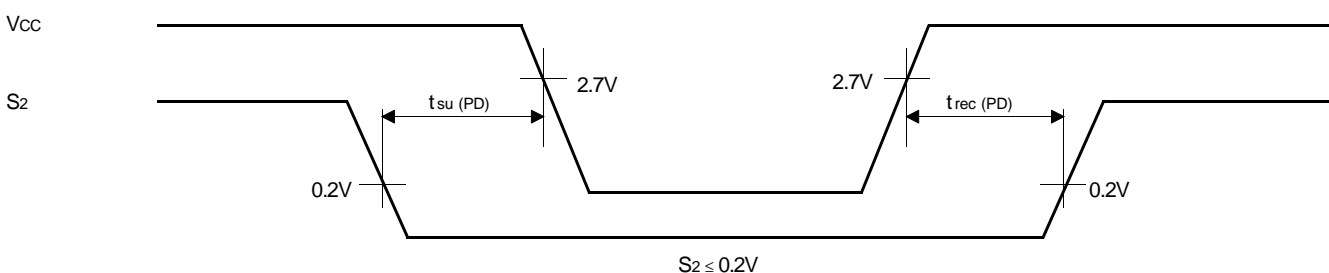
**(3) POWER DOWN CHARACTERISTICS**

**$\overline{S1}$  control mode**



Note 9: On the power down mode by controlling  $\overline{S1}$ , the input level of S2 must be S<sub>2</sub> ≥ V<sub>CC</sub> - 0.2V or S<sub>2</sub> ≤ 0.2V. The other pins (Address, I/O,  $\overline{WE}$ ,  $\overline{OE}$ ) can be in high impedance state.

**S2 control mode**



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