



# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

Designed primarily for pulsed wideband applications with frequencies up to 450 MHz. Devices are unmatched and are suitable for use in industrial, medical and scientific applications.

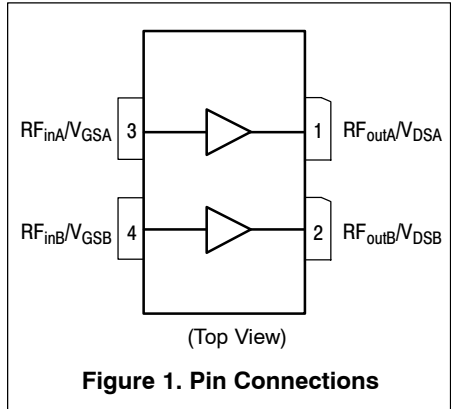
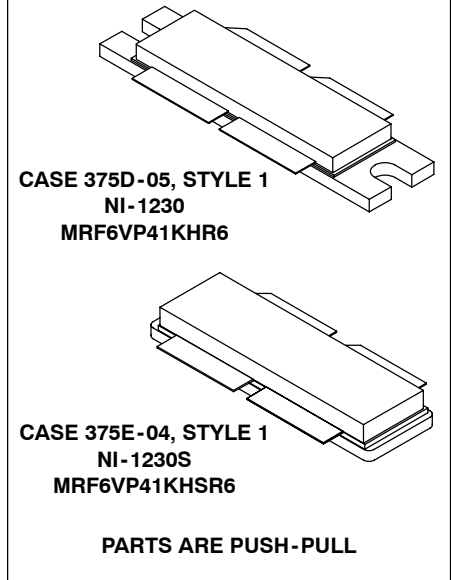
- Typical Pulsed Performance at 450 MHz:  $V_{DD} = 50$  Volts,  $I_{DQ} = 150$  mA,  $P_{out} = 1000$  Watts Peak, Pulse Width = 100  $\mu$ sec, Duty Cycle = 20%  
 Power Gain — 20 dB  
 Drain Efficiency — 64%
- Capable of Handling 10:1 VSWR, @ 50 Vdc, 450 MHz, 1000 Watts Peak Power

### Features

- Qualified Up to a Maximum of 50  $V_{DD}$  Operation
- Integrated ESD Protection
- Excellent Thermal Stability
- Designed for Push-Pull Operation
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- RoHS Compliant
- In Tape and Reel. R6 Suffix = 150 Units per 56 mm, 13 inch Reel.

**MRF6VP41KHR6**  
**MRF6VP41KHSR6**

**10-450 MHz, 1000 W, 50 V**  
**LATERAL N-CHANNEL**  
**BROADBAND**  
**RF POWER MOSFETs**



**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +110	Vdc
Gate-Source Voltage	$V_{GS}$	-6, +10	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	$^{\circ}$ C
Case Operating Temperature	$T_C$	150	$^{\circ}$ C
Operating Junction Temperature	$T_J$	200	$^{\circ}$ C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 1000 W Pulsed, 100 μsec Pulse Width, 20% Duty Cycle	R <sub>θJC</sub>	0.03	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

**Table 4. Electrical Characteristics** (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics** <sup>(3)</sup>

Gate-Source Leakage Current (V <sub>GS</sub> = 5 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	—	—	10	μAdc
Drain-Source Breakdown Voltage (I <sub>D</sub> = 300 mA, V <sub>GS</sub> = 0 Vdc)	V <sub>(BR)DSS</sub>	110	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 50 Vdc, V <sub>GS</sub> = 0 Vdc)	I <sub>DSS</sub>	—	—	100	μAdc
Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 100 Vdc, V <sub>GS</sub> = 0 Vdc)	I <sub>DSS</sub>	—	—	5	mA

**On Characteristics**

Gate Threshold Voltage <sup>(3)</sup> (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 1600 μAdc)	V <sub>GS(th)</sub>	1	1.68	3	Vdc
Gate Quiescent Voltage <sup>(4)</sup> (V <sub>DD</sub> = 50 Vdc, I <sub>D</sub> = 150 mAdc, Measured in Functional Test)	V <sub>GS(Q)</sub>	1.5	2.2	3.5	Vdc
Drain-Source On-Voltage <sup>(3)</sup> (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 4 Adc)	V <sub>DS(on)</sub>	—	0.28	—	Vdc

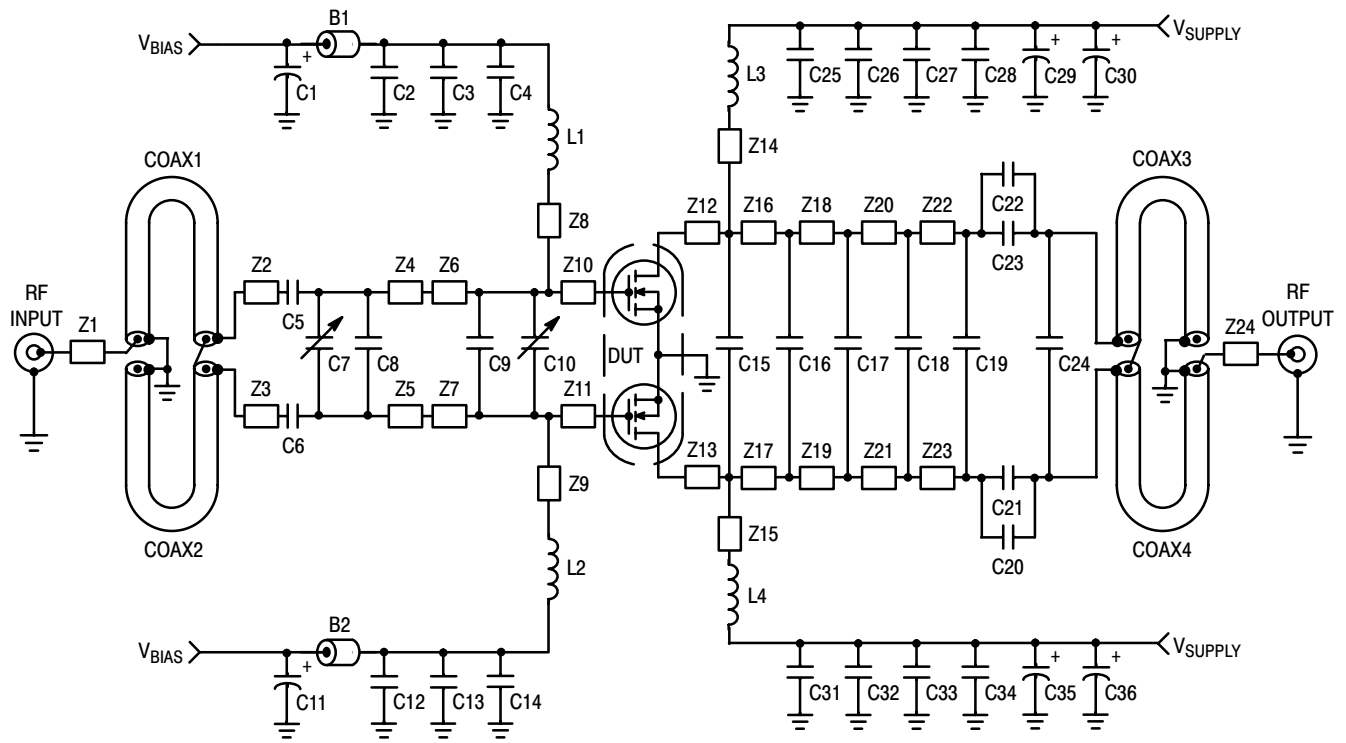
**Dynamic Characteristics** <sup>(3)</sup>

Reverse Transfer Capacitance (V <sub>DS</sub> = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V <sub>GS</sub> = 0 Vdc)	C <sub>rss</sub>	—	3.3	—	pF
Output Capacitance (V <sub>DS</sub> = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V <sub>GS</sub> = 0 Vdc)	C <sub>oss</sub>	—	147	—	pF
Input Capacitance (V <sub>DS</sub> = 50 Vdc, V <sub>GS</sub> = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C <sub>iss</sub>	—	506	—	pF

**Functional Tests** <sup>(4)</sup> (In Freescale Test Fixture, 50 ohm system) V<sub>DD</sub> = 50 Vdc, I<sub>DQ</sub> = 150 mA, P<sub>out</sub> = 1000 W Peak (200 W Avg.), f = 450 MHz, 100 μsec Pulse Width, 20% Duty Cycle

Power Gain	G <sub>ps</sub>	19	20	22	dB
Drain Efficiency	η <sub>D</sub>	60	64	—	%
Input Return Loss	IRL	—	-18	-9	dB

1. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
3. Each side of device measured separately.
4. Measurement made with device in push-pull configuration.



Z1	0.366" x 0.082" Microstrip	Z14*, Z15*	0.764" x 0.150" Microstrip
Z2*, Z3*	0.170" x 0.100" Microstrip	Z16, Z17	0.290" x 0.430" Microstrip
Z4*, Z5*	0.220" x 0.451" Microstrip	Z18, Z19	0.100" x 0.430" Microstrip
Z6, Z7	0.117" x 0.726" Microstrip	Z20, Z21, Z22, Z23	0.080" x 0.430" Microstrip
Z8*, Z9*	0.792" x 0.058" Microstrip	Z24	0.257" x 0.215" Microstrip
Z10, Z11	0.316" x 0.726" Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030", $\epsilon_r = 2.55$
Z12, Z13	0.262" x 0.507" Microstrip		

\* Line length includes microstrip bends

**Figure 2. MRF6VP41KHR6 Test Circuit Schematic**

**Table 5. MRF6VP41KHR6 Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
B1, B2	47 $\Omega$ , 100 MHz Short Ferrite Beads	2743019447	Fair-Rite
C1, C11	47 $\mu$ F, 50 V Electrolytic Capacitors	476KXM063M	Illinois
C2, C12, C28, C34	0.1 $\mu$ F Chip Capacitors	CDR33BX104AKYS	Kemet
C3, C13, C27, C33	220 nF, 50 V Chip Capacitors	C1812C224K5RAC	Kemet
C4, C14	2.2 $\mu$ F, 50 V Chip Capacitors	C1825C225J5RAC	Kemet
C5, C6, C8, C15	27 pF Chip Capacitors	ATC100B270JT500XT	ATC
C7, C10	0.8-8.0 pF Variable Capacitors	27291SL	Johanson Components
C9	33 pF Chip Capacitor	ATC100B330JT500XT	ATC
C16	12 pF Chip Capacitor	ATC100B120JT500XT	ATC
C17	10 pF Chip Capacitor	ATC100B100JT500XT	ATC
C18	9.1 pF Chip Capacitor	ATC100B9R1CT500XT	ATC
C19	8.2 pF Chip Capacitor	ATC100B8R2CT500XT	ATC
C20, C21, C22, C23, C25, C32	240 pF Chip Capacitors	ATC100B241JT200XT	ATC
C24	5.6 pF Chip Capacitor	ATC100B5R6CT500XT	ATC
C26, C31	2.2 $\mu$ F, 100 V Chip Capacitors	2225X7R225KT3AB	ATC
C29, C30, C35, C36	330 $\mu$ F, 63 V Electrolytic Capacitors	EMVY630GTR331MMH0S	Multicomp
Coax1, 2, 3, 4	25 $\Omega$ Semi Rigid Coax, 2.2" Long	UT-141C-25	Micro-Coax
L1, L2	2.5 nH, 1 Turn Inductors	A01TKLC	CoilCraft
L3, L4	43 nH, 10 Turn Inductors	B10TJLC	Coilcraft

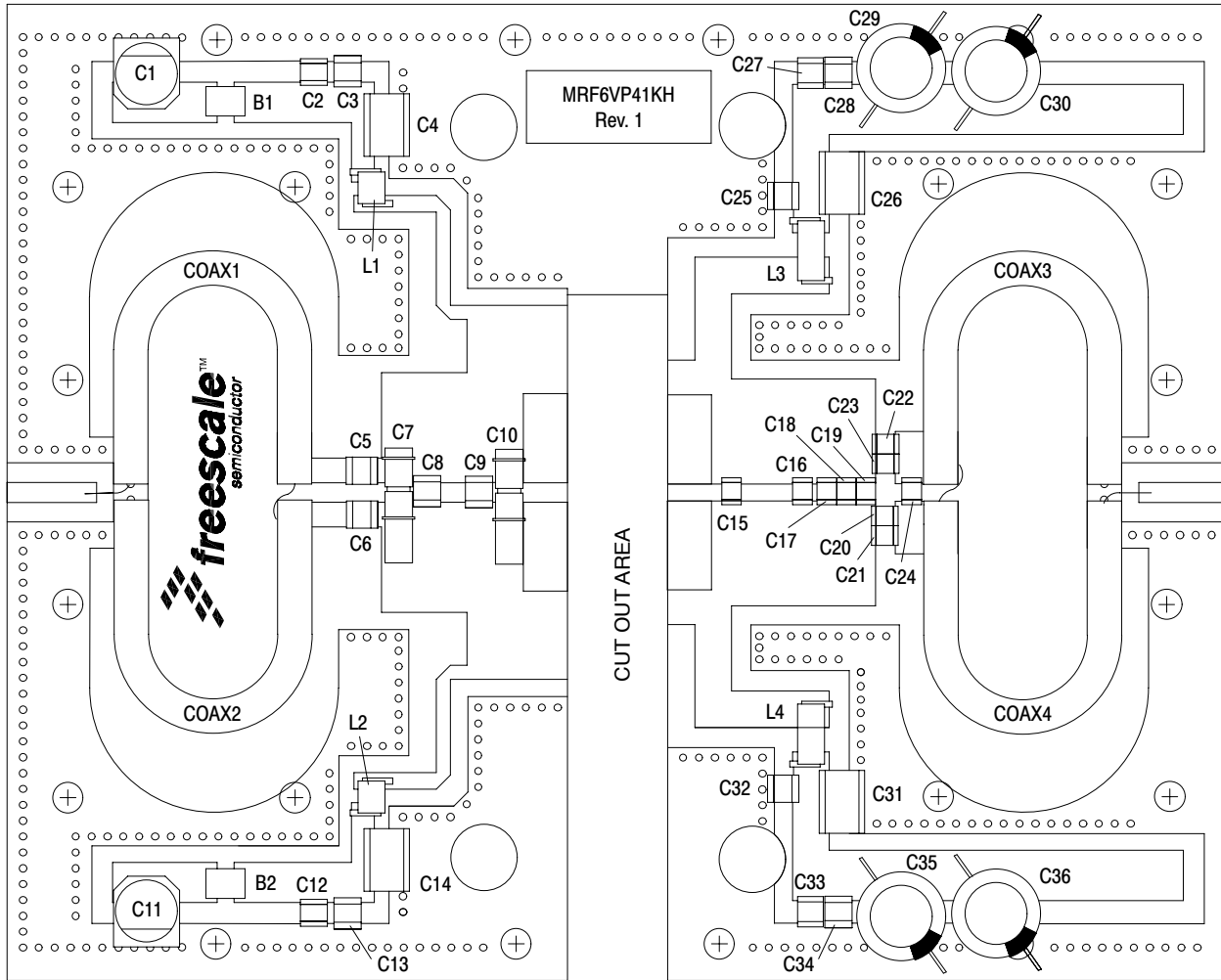
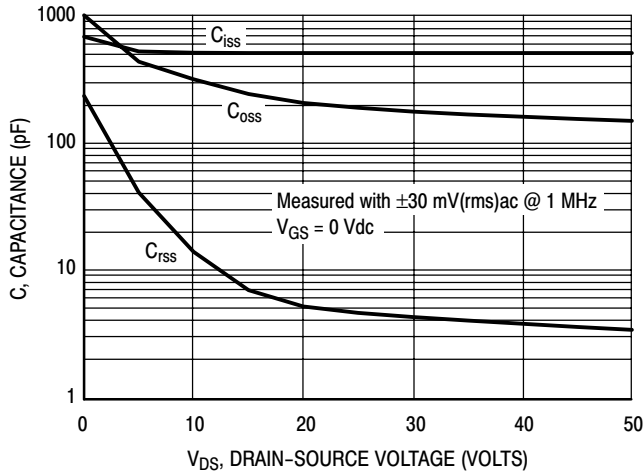
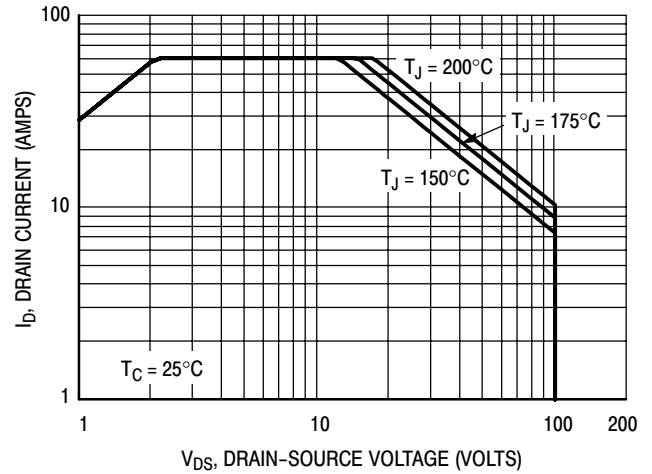


Figure 3. MRF6VP41KHR6 Test Circuit Component Layout

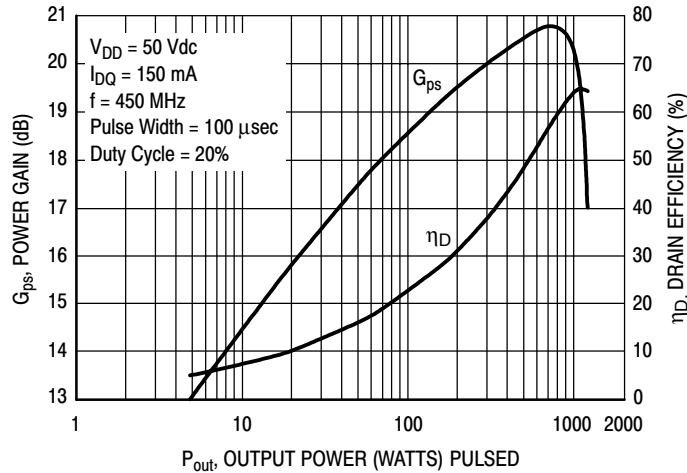
## TYPICAL CHARACTERISTICS



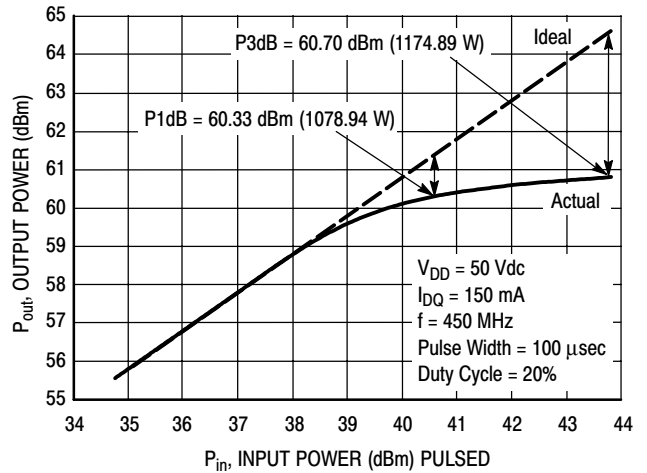
**Figure 4. Capacitance versus Drain-Source Voltage**



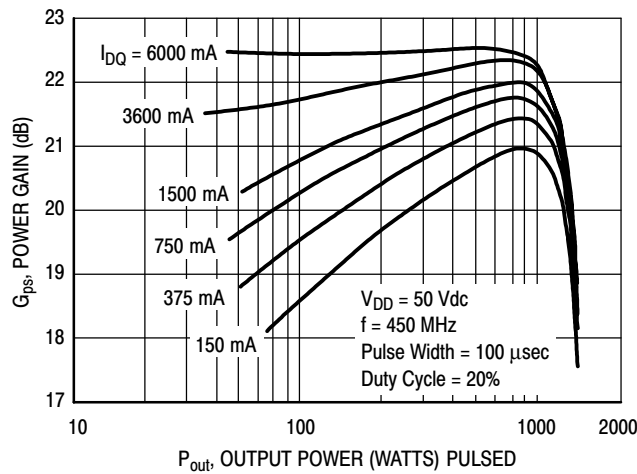
**Figure 5. DC Safe Operating Area**



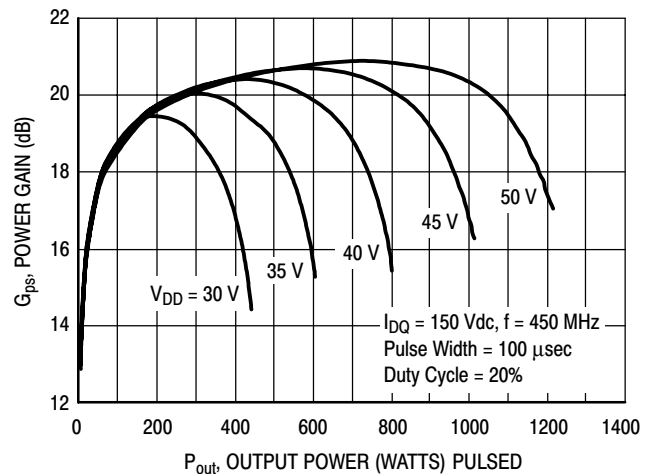
**Figure 6. Pulsed Power Gain and Drain Efficiency versus Output Power**



**Figure 7. Pulsed Output Power versus Input Power**

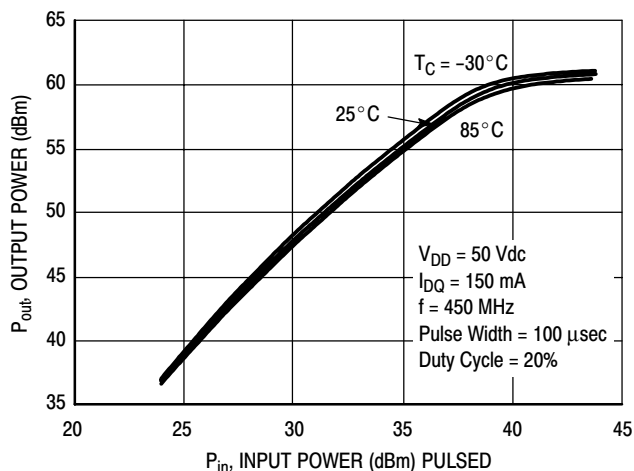


**Figure 8. Pulsed Power Gain versus Output Power**

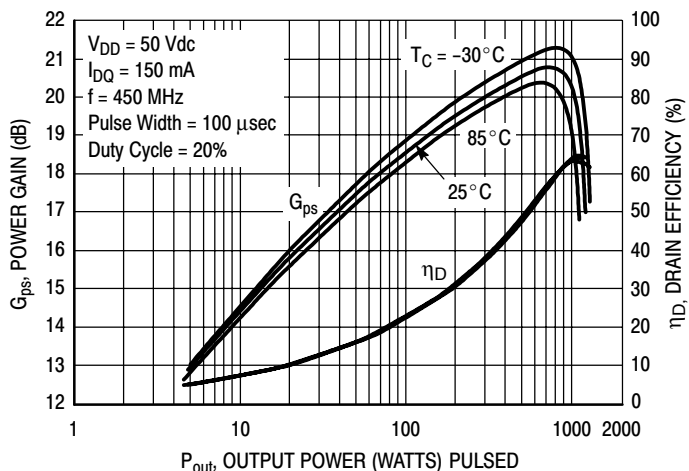


**Figure 9. Pulsed Power Gain versus Output Power**

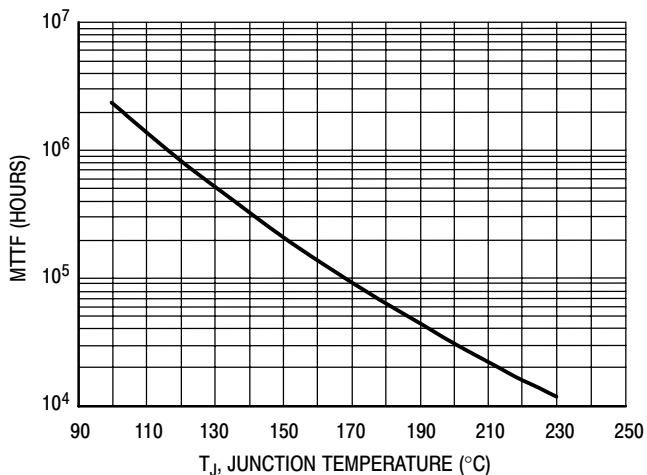
## TYPICAL CHARACTERISTICS



**Figure 10. Pulsed Output Power versus Input Power**



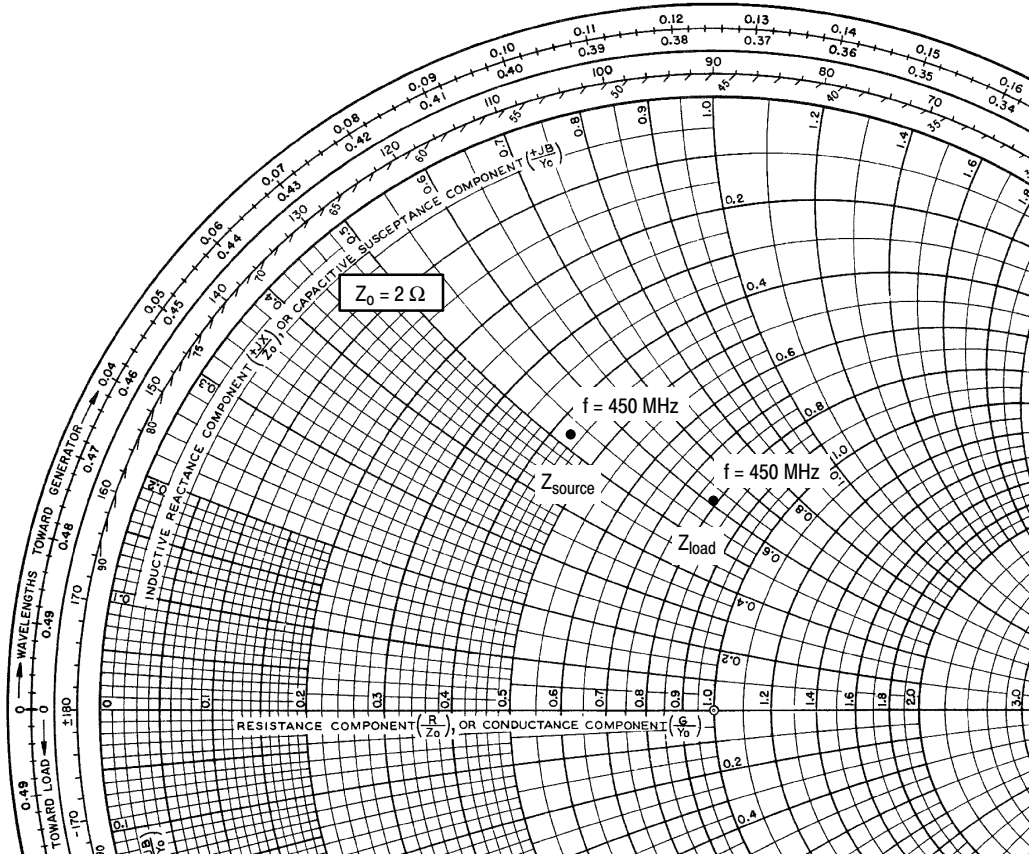
**Figure 11. Pulsed Power Gain and Drain Efficiency versus Output Power**



This above graph displays calculated MTTF in hours when the device is operated at  $V_{DD} = 50$  Vdc,  $P_{out} = 1000$  W Peak, Pulse Width = 100  $\mu$ sec, Duty Cycle = 20%, and  $\eta_D = 64\%$ .

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

**Figure 12. MTTF versus Junction Temperature**



$V_{DD} = 50 \text{ Vdc}$ ,  $I_{DQ} = 150 \text{ mA}$ ,  $P_{out} = 1000 \text{ W Peak}$

f MHz	Z <sub>source</sub> Ω	Z <sub>load</sub> Ω
450	0.86 + j1.06	1.58 + j1.22

Z<sub>source</sub> = Test circuit impedance as measured from gate to ground.

Z<sub>load</sub> = Test circuit impedance as measured from drain to ground.

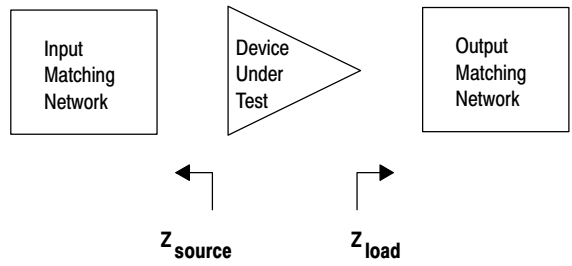
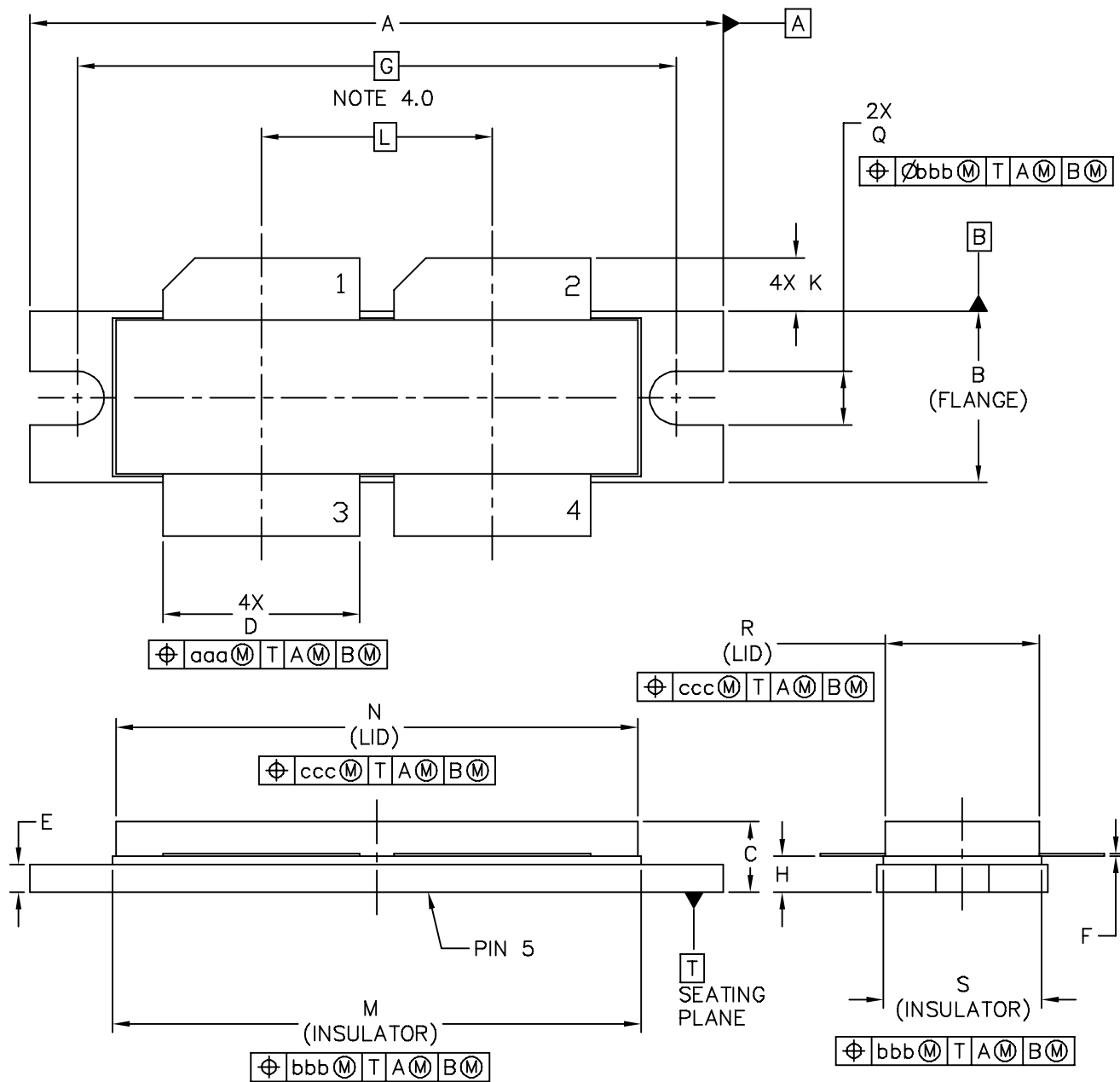


Figure 13. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



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TITLE:  NI-1230	DOCUMENT NO: 98ASB16977C	REV: E
	CASE NUMBER: 375D-05	31 MAR 2005
	STANDARD: NON-JEDEC	



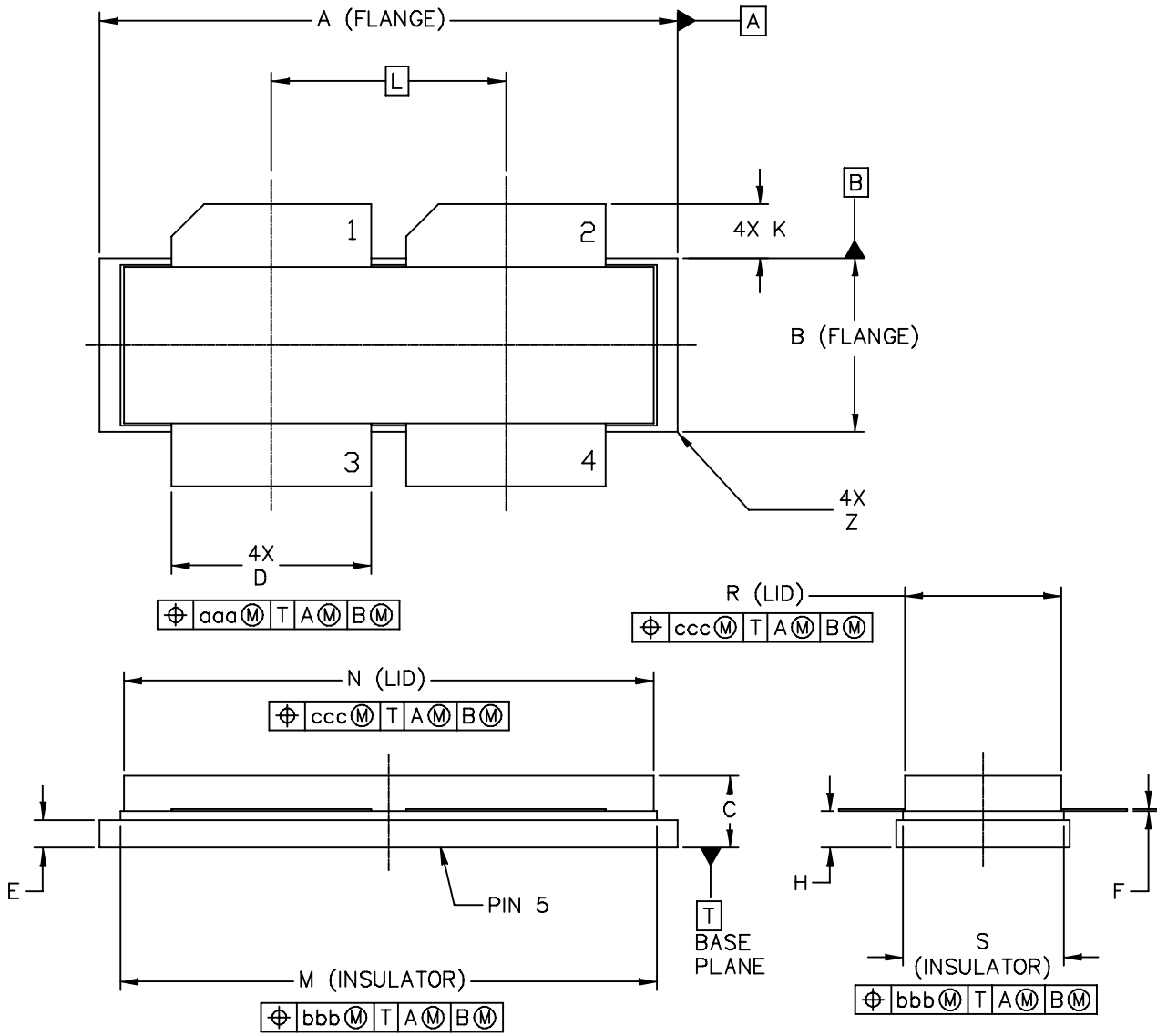
NOTES:

- 1.0 INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- 2.0 CONTROLLING DIMENSION: INCH
- 3.0 DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.
- 4.0 RECOMMENDED BOLT CENTER DIMENSION OF 1.52 (38.61) BASED ON M3 SCREW.

STYLE 1:

- PIN 1 - DRAIN
- 2 - DRAIN
- 3 - GATE
- 4 - GATE
- 5 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER		
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX	
A	1.615	1.625	41.02	41.28	N	1.218	1.242	30.94	31.55	
B	.395	.405	10.03	10.29	Q	.120	.130	3.05	3.3	
C	.150	.200	3.81	5.08	R	.355	.365	9.01	9.27	
D	.455	.465	11.56	11.81	S	.365	.375	9.27	9.53	
E	.062	.066	1.57	1.68						
F	.004	.007	0.1	0.18						
G	1.400 BSC		35.56 BSC		aaa	.013		0.33		
H	.082	.090	2.08	2.29	bbb	.010		0.25		
K	.117	.137	2.97	3.48	ccc	.020		0.51		
L	.540 BSC		13.72 BSC							
M	1.219	1.241	30.96	31.52						
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	CASE NUMBER: 375E-04	05 AUG 2005	
	STANDARD: NON-JEDEC		

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH
3. DIMENSION H IS MEASURED .030 AWAY FROM PACKAGE BODY

STYLE 1:

- PIN 1 - DRAIN
- 2 - DRAIN
- 3 - GATE
- 4 - GATE
- 5 - SOURCE

DIM	INCHES		MILLIMETERS		DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	1.265	1.275	32.13	32.38	R	.355	.365	9.01	9.27
B	.395	.405	10.03	10.29	S	.365	.375	9.27	9.53
C	.150	.200	3.81	5.08	Z	---	.040	---	1.02
D	.455	.465	11.56	11.81					
E	.062	.066	1.57	1.68	aaa	.013		0.33	
F	.004	.007	0.1	0.18	bbb	.010		0.25	
H	.082	.090	2.08	2.29	ccc	.020		0.51	
K	.117	.137	2.97	3.48					
L	.540 BSC		13.72 BSC						
M	1.219	1.241	30.96	31.52					
N	1.218	1.242	30.94	31.55					
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					STANDARD: NON-JEDEC				

## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Jan. 2008	<ul style="list-style-type: none"><li>• Initial Release of Data Sheet</li></ul>

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