

RAiO

RA8816

**144x65 Character/Graphic
LCD Driver
Specification**

Version 1.6

December 20, 2007

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|----------------|-------------------|---|
| Version | Date | Description |
| 1.0 | September 5, 2005 | First Release |
| 1.1 | December 19, 2005 | Update Table 5-3 |
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1. General Description

The RA8816 is a Dot-Matrix LCD Driver that supports both character and graphic mode. It built-in a 256Kbyte character ROM that consists of Chinese, English and ASCII fonts. The embedded 1170Byte display RAM supports up to 144x65 dots LCD panel. The RA8816 also provides a scrolling buffer memory for scrolling functions. It supports up, down, left and right scrolling features, and all of the scrolling is execute by hardware.

In character mode, the RA8816 supports Chinese BIG5 code or GB code. The system(MPU) does not need take a lot of time to show the Chinese font in graphic mode. It also provides small ASCII(8x8) and big ASCII(8x16) font for English character, Japanese, European and Latin. The RA8816 integrates much powerful hardware that including Contrast adjustment, 4x5 Key-Scan, eight General Purpose I/O and EL Backlight signals for EL driver.

The RA8816 is a high integration chip of LCD Controller. It reduce a lot of time for system develop, and save much cost for hardware system that due to it provides many features for related LCD display application.

2. Feature

- Support both Character and Graphic Mode
- Support 8080/6800 8/4-bit Parallel Interface, 3-Wire/4-Wire Serial Interface, IIC interface
- Built-in 256KB Font ROM: Chinese, English, ASCII, Japanese, Latin, Latin-ext A, Latin-ext B
- Support ASCII 8x8/8x16 Half Size Font, 16x16 Full Size Chinese Font
- Support Maximum 144Seg x 65Com LCD Panel. 4 x 9 Chinese Fonts(16x16), or 8 x 18 English Fonts(8x8)
- Built-in 1170 Bytes Display RAM and 450Byte Scrolling Buffer
- Support 1/65 Duty, 1/9~1/5 Bias Panel
- Built-in 2X~4X(Voltage Booster), Voltage Regulator, Voltage Follower
- Eight General Purpose I/O
- Built-in 4x5 Key-scan Circuit
- Support Horizontal/Vertical Scrolling Functions
- Built-in 256Byte SRAM for Create Font
- Provide Signals for EL Driver
- Provide 32-Steps Contrast Adjuster
- Build-in RC Oscillator
- Voltage Operation: VDD → 2.7~3.8V
- Package: Gold Bump Die

3. Block Diagram

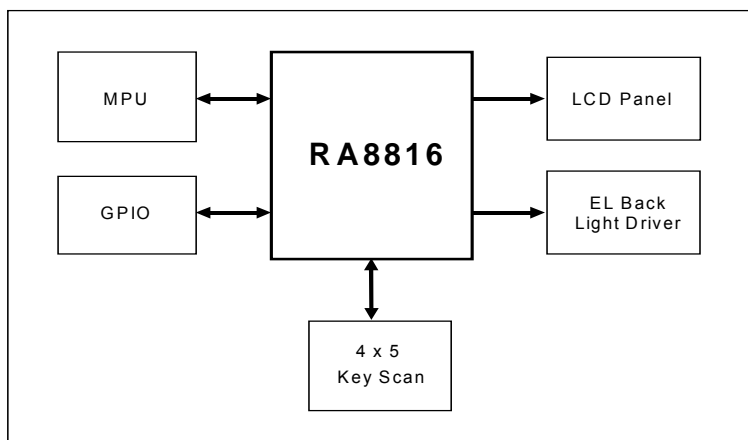


Figure 3-1: System Block

The RA8816 is consisted of Display RAM, 256Kbyte Font ROM, Command Registers, LCD Controller, LCD Driver, Voltage Booster, Voltage Regulator, MPU Interface and Key-Scan circuit.

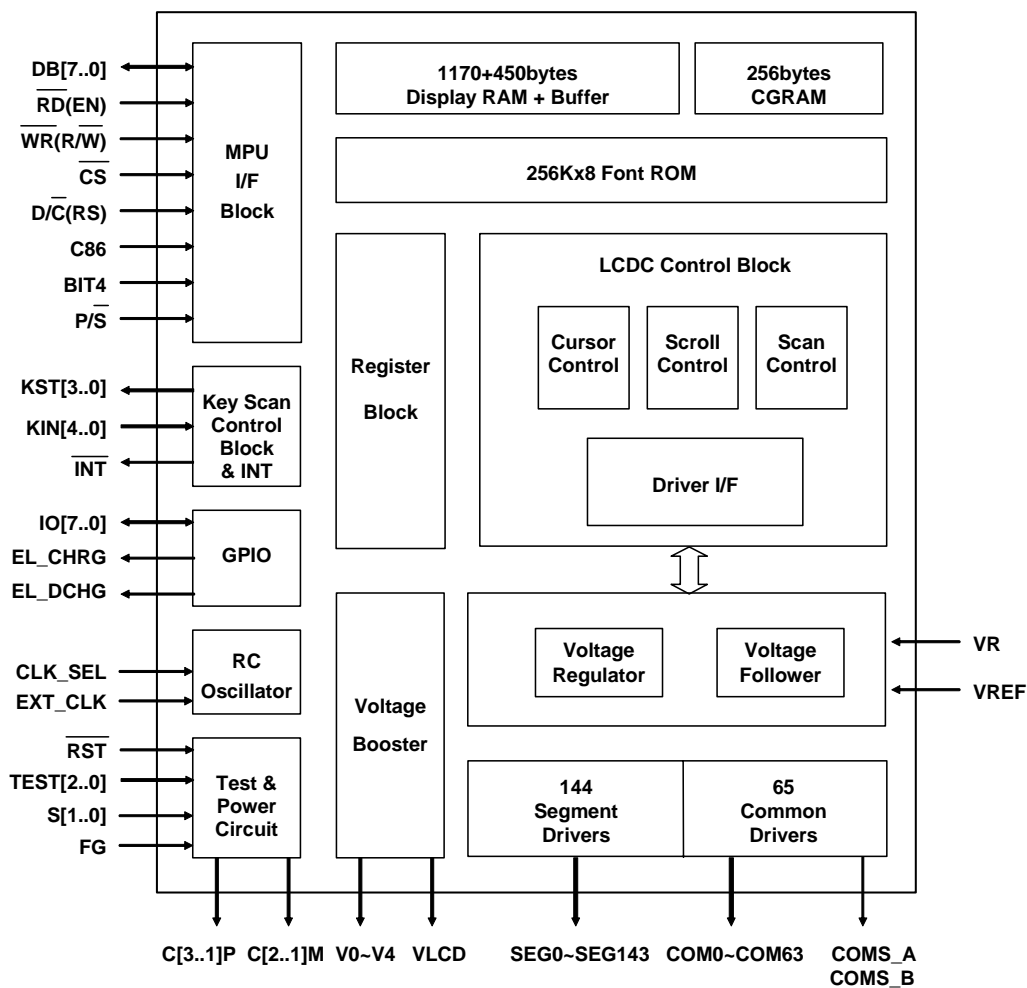


Figure 3-2: Internal Block

4. Pin Definition

4-1 MPU Interface

Table 4-1

| Pin Name | I/O | Description |
|---|-----|--|
| <p>DB[7..0]</p> <p>DB0: SCK DB1: SDA/SDO DB2: RS/SDI DB3: \overline{CS} DB[7..6]: SMOD</p> | I/O | <p>Data Bus</p> <p>When the MPU use parallel mode and 8-bit then all of the DB[7..0] are valid. When use 4-bit then only DB[3..0] are valid, and DB[7..4] have to keep floating.</p> <p>When P/\overline{S} is "0", then the interface between MPU and RA8816 is Serial Mode. The pins DB[7..6](SMOD[1..0]) are used to select which serial mode:</p> <p>SMOD : Serial Mode</p> <p>-----</p> <p>0 0 : IIC interface, SCK, SDA are used 0 1 : 3-Wire, SCK, SDA, \overline{CS} are used. 1 0 : 4-Wire, SCK, SDA, RS, \overline{CS} are used. 1 1 : 4-Wire, SCK, SDO, SDI, \overline{CS} are used.</p> <p>In serial mode, all of the related signals are defined by DB[3..0]: SCK(DB0) : Serial Clock. SDA(DB1) : Bi-direction Mode Serial Data. SDO(DB1) : Data Out. RS(DB2) : Memory/Register Cycle Select. SDI(DB2) : Serial Data In. \overline{CS}(DB3) : Chip Select, active low.</p> <p>In the IIC mode, \overline{WR}, \overline{RD} and DB[5..2] are used as the IIC device address - IICA[5..0] to avoid conflict with other IIC devices. The unused pin must keep NC for serial mode.</p> |
| <p>\overline{RD} EN</p> | I | <p>Read Control or Enable</p> <p>When use 8080 series interface, \overline{RD} is the read signal and active low. When use 6800 series interface, EN is the Enable signal and active high. In the IIC mode, \overline{RD} is used as IIC device address - IICA[4]. This pin must keep NC for 3 or 4-wires serial mode.</p> |
| <p>\overline{WR} R/\overline{W}</p> | I | <p>Write Control or Read-Write Control</p> <p>When use 8080 series interface, \overline{WR} is the write signal and active low. When use 6800 series interface, this pin is R/\overline{W}, active high for read cycle and active low for write cycle. In the IIC mode, \overline{WR} is used as IIC device address - IICA[5]. This pin must keep NC for 3 or 4-wires serial mode.</p> |
| <p>D/\overline{C} RS</p> | I | <p>Data/Command Select or Register Select)</p> <p>When use 8080 series interface, this is Data or Command signal. When D/\overline{C} is "0", means Register Cycle(or Command Cycle). When D/\overline{C} is "1", means Data Access Cycle(Data Cycle). When use 6800 series interface, this is the RS signal. When RS is "0",</p> |

| | | |
|------------------|---|---|
| | | means Register Cycle and "1" means Data Access Cycle. This pin must keep NC for serial mode. |
| \overline{CS} | I | Chip Select This is a chip enable for RA8816. This pin must keep NC for serial mode. |
| \overline{INT} | O | Interrupt Signal This is an interrupt output for MPU. Active low ◦ |
| C86 | I | MPU Select C86 = 0 → The MPU interface is 8080 series. C86 = 1 → The MPU interface is 6800 series(Default). This pin must keep NC for serial mode. |
| BIT4 | I | Data Bit Select BIT4 = 0 → The parallel mode is use 8-bit data bus. BIT4 = 1 → The parallel mode is use 4-bit data bus(Default). This pin must keep NC for serial mode. |
| P/\overline{S} | I | Parallel/Serial Select $P/\overline{S} = 0$ → The MPU interface is serial mode(Default). See the setting of DB[7..6]. $P/\overline{S} = 1$ → The MPU interface is parallel mode. |

4-2 Clock and Power

Table 4-3

| Pin Name | I/O | Description |
|-------------|-----|---|
| V0~V4 | O | Voltage Source of LCD Driver The relationship of the power is $V_{LCD} > V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ ◦ |
| C1P, C1M | I | Capacitor Input These are used to connect a capacitor for internal Booster. |
| C2P, C2M | I | Capacitor Input These are used to connect a capacitor for internal Booster. |
| C3P | I | Capacitor Input These are used to connect a capacitor for internal Booster. |
| VLCD | O | Booster Output |
| VREF | I | Reference Voltage Input This is the reference voltage input when use an external regulator. |
| VR | I | Voltage Adjustment Applies voltage between V0 and VSS. Using a resistive divider. |
| CLK_SEL | I | Clock Select This pin is used to select the clock source. When CLK_SEL is "1", the clock is generated by internal RC oscillator. When CLK_SEL is "0", the system clock is driven by external pin - EXT_CLK. |
| EXT_CLK | I | External Clock When CLK_SEL is "0", this pin is the external clock input. When CLK_SEL is "1", this pin do not used and has to connect VDD or GND. |
| VDD VDDP | P | VDD Power |
| GND GNDP | P | Ground |

4-3 LCD Panel Interface

Table 4-2

| Pin Name | I/O | Description |
|------------------|-----|-------------------------------|
| SEG0 ~ SEG143 | O | Segment Signals for Panel |
| COM0 ~ COM63 | O | Common Signals for Panel |
| COMS_A COMS_B | O | Icon Common Signals for Panel |
| DUMMY[5..0] | O | Dummy PAD |

4-4 Misc.

Table 4-4

| Pin Name | I/O | Description |
|-------------|-----|--|
| KST[3..0] | O | Key Strobe Output |
| KIN[4..0] | I | Key Data Input |
| IO[7..0] | I/O | General Purpose I/O |
| EL_CHRG | O | EL Charge Signal |
| EL_DCHG | O | EL Discharge Signal |
| RST | I | Reset |
| TEST[2..0] | I | Test Pins These pins must contact to GND in normal mode. |
| S[1..0], FG | I | Test Pins These pins must keep NC for normal mode. |

Table 4-5: Pin Definition of Parallel/Serial Mode of MPU

| Pin Name | I/O | Parallel Mode | | | | Serial Mode | | | |
|-------------------------------------|-----|-------------------|-------------------|-------------------|-------------------|-------------|-----------------|-----------------|-----------------|
| | | 8080 | | 6800 | | IIC | 3-Wire | 4-Wire (A-Typ) | 4-Wire (B-Typ) |
| | | 8Bit | 4Bit | 8Bit | 4Bit | | | | |
| DB7 | I/O | DB7 | --* ¹ | DB7 | -- | 0 | 0 | 1 | 1 |
| DB6 | I/O | DB6 | -- | DB6 | -- | 0 | 1 | 0 | 1 |
| DB5 | I/O | DB5 | -- | DB5 | -- | IICA3 | -- | -- | -- |
| DB4 | I/O | DB4 | -- | DB4 | -- | IICA2 | -- | -- | -- |
| DB3 | I/O | DB3 | DB3 | DB3 | DB3 | IICA1 | \overline{CS} | \overline{CS} | \overline{CS} |
| DB2 | I/O | DB2 | DB2 | DB2 | DB2 | IICA0 | -- | RS | SDI |
| DB1 | I/O | DB1 | DB1 | DB1 | DB1 | SDA | SDA | SDA | SDO |
| DB0 | I/O | DB0 | DB0 | DB0 | DB0 | SCK | SCK | SCK | SCK |
| \overline{RD} , EN | I | \overline{RD} | \overline{RD} | EN | EN | IICA4 | 1* ² | 1 | 1 |
| \overline{WR} , R/ \overline{W} | I | \overline{WR} | \overline{WR} | R/ \overline{W} | R/ \overline{W} | IICA5 | 1 | 1 | 1 |
| D/ \overline{C} , RS | I | D/ \overline{C} | D/ \overline{C} | RS | RS | 1 | 1 | 1 | 1 |
| \overline{CS} | I | \overline{CS} | \overline{CS} | \overline{CS} | \overline{CS} | 1 | 1 | 1 | 1 |
| C86 | I | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| BIT4 | I | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| P/ \overline{S} | I | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

Note1: "--" means not used and keep floating(NC).

Note2: In serial mode the unused parallel pins have to connect to 1(VDD).

5. Registers Description

5-1 Register Table

Table 5-1: Register Table

| ID | Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Description |
|----|--------|----------|----------|---------|----------|----------|----------|-----------|-------------|---------------------|
| 0 | DWFR | B/C | -- | NW5 | NW4 | NW3 | NW2 | NW1 | NW0 | Wave Form Select |
| 1 | PWRR | SRST | MCLR | -- | IO_IEN | KWK | IOWK | DOFF_Z | SLP | Power Control |
| 2 | SYSR | LS3 | LS2 | LS1 | LS0 | GB_EN | -- | RS1 | RS0 | System Setting |
| 3 | MWMR | BMOD1 | BMOD0 | BIEN | ASCS | BOLD | INV | MD1 | MD0 | Memory Mode |
| 4 | CURCR | H3 | H2 | H1 | H0 | -- | BLK | CR | CUR_EN | Cursor Control |
| 5 | X-CUR | -- | -- | X5 | X4 | X3 | X2 | X1 | X0 | Cursor X Position |
| 6 | Y-CUR | -- | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 | Y0 | Cursor Y Position |
| 7 | KEYR | KSB | KDB1 | KDB0 | KSTB_SEL | K_AUTO | IRE | KF1/KSTB1 | KF0/KSTB0 | Key-scan Control |
| | KSDR | SIRQ | KSTB1 | KSTB0 | KSD4 | KSD3 | KSD2 | KSD1 | KSD0 | Key-scan Data |
| 8 | SWSXR | -- | -- | -- | SSX4 | SSX3 | SSX2 | SSX1 | SSX0 | X-Scroll Start |
| 9 | SWSYR | -- | -- | SSY5 | SSY4 | SSY3 | SSY2 | SSY1 | SSY0 | Y-Scroll Start |
| A | SWRXR | -- | -- | -- | SRX4 | SRX3 | SRX2 | SRX1 | SRX0 | X-Scroll Range |
| B | SWRYR | PINV | -- | SRY5 | SRY4 | SRY3 | SRY2 | SRY1 | SRY0 | Y-Scroll Range |
| C | SCOR | SL7 | SL6 | SL5/SR5 | SL4/SR4 | SL3/SR3 | SL2/SR2 | SL1/SR1 | SL0/SR0 | Scroll Unit |
| D | ASCR | SPD3 | SPD2 | SPD1 | SPD0 | STP3 | STP2 | STP1 | STP0 | Auto Scroll Control |
| E | SCCR | SCR_IMD1 | SCR_IMD0 | SCR_MD | SBUF | SCR_DIR1 | SCR_DIR0 | SCR_INTEN | AUTO_SCROLL | Scroll Control |
| F | ISR | BF | -- | -- | -- | IO_I | SCR_I | KI | BI | Interrupt Status |
| 10 | CSTR | BR2 | BR1 | BR0 | CT4 | CT3 | CT2 | CT1 | CT0 | Contrast |
| 11 | DRCR_A | BOFF | EN_R | EN_G | ROFF | IDIR | -- | CDIR | SDIR | Driver Control |
| 12 | DRCR_B | CK_BS1 | CK_BS0 | RR2 | RR1 | RR0 | IRS | HD1 | HD0 | Driver Control |
| 13 | BLTR | BLK_EN | PBK_EN | -- | INV | BLT3 | BLT2 | BLT1 | BLT0 | Blink Setting |
| 14 | IODR | OE7 | OE6 | OE5 | OE4 | OE3 | OE2 | OE1 | OE0 | I/O Port Direction |
| 15 | IODAR | IOD7 | IOD6 | IOD5 | IOD4 | IOD3 | IOD2 | IOD1 | IOD0 | I/O Port Data |
| 16 | ELCR | EL_EN | -- | -- | -- | ELT3 | ELT2 | ELT1 | ELT0 | EL Control |
| 17 | CGMI | -- | -- | -- | -- | -- | UMI2 | UMI1 | UMI0 | Create Font Select |
| 18 | CGMD | CGMD7 | CGMD6 | CGMD5 | CGMD4 | CGMD3 | CGMD2 | CGMD1 | CGMD0 | Create Font Data |

5-2 Register Contents

The RA8816 accept two Command Cycle from MPU. One is Register Cycle(RS = 0) and the other is Memory Cycle(RS = 1). The MPU has to assign the register number of RA8816 that before access these registers. Therefore, the first byte that MPU pass to RA8816 will be store into Index Register. And RA8816 will assume the next byte is read from or write into the register which Index Register assigned.

IR (Index Register)

| RW | RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | ID4 | ID3 | ID2 | ID1 | ID0 |

ID[4..0]: These bits are used to store the register number that MPU want to access on next cycle.

The ID[[4..0] provide 32 register number(00h~1Fh). But currently the RA8816 only used 25 registers (00h~18h). All of these registers are be initially to "00h" after RESET.

Memory Data (RAMD)

| RW | RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0/1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

If RS is "1", It means MPU execute the Memory Cycle for RA8816. When RW is "0", MPU will write data to Display RAM or ICON RAM that according the setting of MD[1..0](REG[03h] bit1-0). For example, MPU write Big5/CG code to memory in Text Mode, or write bitmap data to display memory in Graphic mode. When RW is "1", the MPU read data from different paths of RA8816. It depend on the operation mode as following:

1. Full Size Text Mode: From up to down of Left side(16-Bytes), and then up to down of Right side(16-Bytes), total is 32-Bytes.
2. Half Size Text Mode: From up to down, total 16-Bytes data.
3. Small ASCII Text Mode: From up to down, total 8-Bytes data.
4. Graphics Mode: From left to right, each reading is one byte(8-Pixels).

[00h] Driver Waveform Register (DWFR)

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | B/C | -- | NW5 | NW4 | NW3 | NW2 | NW1 | NW0 |

B/C: Select waveform of drive. 0 → B-Type waveform. 1 → C-Type waveform.

NW[5..0]: These bits are used to assign the Segment/Row number that when internal Frame signals can to it and want to change the state. This function support only when B/C is "1" (C-Type wave form).

[01h] Power Control Register (PWRR)

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|------|------|-----|--------|-----|------|--------|-----|
| 0 | SRST | MCLR | -- | IO_IEN | KWK | IOWK | DOFF_Z | SLP |

SRST: S/W reset. 1 → All of the register will be initialed again except the display memory. Once this bit set to 1 then RA8816 has to take 50us for operation and cannot accept any new command from MCU. 0 → No action.

MCLR: Clear memory. 1 → Clear the Display RAM data to "00h". Once this bit set to 1 then RA8816 has to take 50us for operation and cannot accept any new command from MCU. 0 → No action. If both MCLR and SRST set to "1" then RA8816 will clear the display RAM and then Reset.

IO_IEN : I/O Interrupt Setup. 0 → I/O port Interrupt Disable. 1 → I/O Interrupt Enable.

KWK: Key-scan wake up Setting. 0 → Key-scan Wake up function off. 1 → Key-scan wake up function on.

IOWK: I/O wake up Setting. 0 → I/O port wake up function off. 1 → I/O port wake up function on.

DOFF_Z: Display off. 0 → LCD driver and display off. 1 → LCD driver and display on.

SLP: Sleep mode setting. 1 → Enter sleep mode, and turn off the clock. 0 → RA8816 wake up. This bit was clear to “0” when wake up from I/O port or Key-scan.

[02h] System Register (SYSR)

| | | | | | | | | |
|----|-----|-----|-----|-----|-------|-----|-----|-----|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | LS3 | LS2 | LS1 | LS0 | GB_EN | -- | RS1 | RS0 |

LS[3..0]: Setup the segment number. The maximum segment of RA8816 is 144.

Table 5-2

| LS3 | LS2 | LS1 | LS0 | Line No. |
|-----|-----|-----|-----|----------|
| 0 | 0 | 0 | 0 | 16 |
| 0 | 0 | 0 | 1 | 32 |
| 0 | 0 | 1 | 0 | 48 |
| 0 | 0 | 1 | 1 | 64 |
| 0 | 1 | 0 | 0 | 80 |
| 0 | 1 | 0 | 1 | 96 |
| 0 | 1 | 1 | 0 | 112 |
| 0 | 1 | 1 | 1 | 128 |
| 1 | 0 | 0 | 0 | 144 |
| ⋮ | | | | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

GB_EN: Setup the GB code or BIG5 code. 1 → GB Code. 0 → BIG5 Code.

RS[1..0]: Setup the common number. The maximum common of RA8816 is 64(Not including Icon).

Table 5-3

| Duty | RS1 | RS0 | Status | Common Output Pads | | | | | | | | |
|------|-----|-----|---------|--------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------|
| | | | | COM [0-15] | COM [16-23] | COM [24-26] | COM [27-36] | COM [37-39] | COM [40-47] | COM [48-63] | COMS | |
| 1/33 | 0 | 0 | Normal | COM [0-15] | NC | | | | | | COM [16-31] | COMS |
| | | | Reverse | COM [31-16] | NC | | | | | | COM [15-0] | |
| 1/49 | 0 | 1 | Normal | COM[0-23] | | NC | | | COM[24-47] | | | COMS |
| | | | Reverse | COM[47-24] | | NC | | | COM[23-0] | | | |
| 1/55 | 1 | 0 | Normal | COM[0-26] | | | NC | COM[27-53] | | | | COMS |
| | | | Reverse | COM[53-27] | | | NC | COM[26-0] | | | | |
| 1/65 | 1 | 1 | Normal | COM[0-63] | | | | | | | | COMS |
| | | | Reverse | COM[63-0] | | | | | | | | |

[03h] Memory Write Mode Register (MWMR)

| | | | | | | | | |
|----|-------|-------|------|------|------|-----|-----|-----|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | BMOD1 | BMOD0 | BIEN | ASCS | BOLD | INV | MD1 | MD0 |

BMOD[1..0]: Setup the range for memory written.

Table 5-4

| BMOD1 | BMOD0 | Memory Range of Write |
|-------|-------|-------------------------------|
| 0 | 0 | Normal Display Range |
| 0 | 1 | Display Range + Scroll-Buffer |
| 1 | x | Scroll-Buffer |

BIEN: Busy interrupt control. 1 → Busy interrupt enable (After write data to memory). 0 → Busy interrupt disable.

ASCS: Select ASCII Table. 0 → Select ASCII Table-1. 1 → Select ASCII Table-2. Refer Chapter 6-9.

BOLD: Select Bold Font to write Display RAM. 0 → Normal font. 1 → Bold font.

INV: Select reverse font to write Display RAM. 0 → Normal font. 1 → Reverse font.

MD[1..0]: Select operation mode for Display RAM.

Table 5-5

| MD1 | MD0 | Operation Mode |
|-----|-----|-------------------|
| 0 | 0 | Graphic Mode |
| 0 | 1 | Small ASCII (8X8) |
| 1 | 0 | Big ASCII(8X16) |
| 1 | 1 | Full Size(16X16) |

When Full-Size mode(MD[1..0] = 11), if the first byte data is less than 80h, RA8816 will assume it's an ASCII code and show the Big ASCII font. But if want to show the Big ASCII font that code is large than 80h, then the operation mode has to change to Big ASCII mode(MD[1..0] = 10).

[04h] Cursor Control Register (CURCR)

| | | | | | | | | |
|----|-----|-----|-----|-----|-----|-----|-----|--------|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | H3 | H2 | H1 | H0 | -- | BLK | CR | CUR_EN |

H[3..0]: Setup the cursor height.

Table 5-6

| H3 | H2 | H1 | H0 | Height(Pixel) |
|----|----|----|----|---------------|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 1 | 0 | 3 |
| 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 0 | 0 | 5 |
| 0 | 1 | 0 | 1 | 6 |
| 0 | 1 | 1 | 0 | 7 |
| 0 | 1 | 1 | 1 | 8 |
| 1 | 0 | 0 | 0 | 9 |
| 1 | 0 | 0 | 1 | 10 |
| 1 | 0 | 1 | 0 | 11 |
| 1 | 0 | 1 | 1 | 12 |
| 1 | 1 | 0 | 0 | 13 |
| 1 | 1 | 0 | 1 | 14 |
| 1 | 1 | 1 | 0 | 15 |
| 1 | 1 | 1 | 1 | 16 |

In Small ASCII mode(8X8), the H3 is reserved. The setting of cursor height is only form 1~8pixels(H[3..0] = x000b~x111b).

BLK: Cursor blink select. 0 → No Blinking. 1 → Cursor Blinking.

CR: Cursor return. 0 → No action. 1 → Cursor return. Cursor will return to the left of panel.

CUR_EN: Cursor display select. 0 → Cursor hides. 1 → Cursor Display.

[05h] Cursor Position Register of X (X-CUR)

| | | | | | | | | |
|----|-----|-----|-----|-----|-----|-----|-----|-----|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | -- | -- | X5 | X4 | X3 | X2 | X1 | X0 |

X[5..0]: Setup the cursor position on segment. The unit is 8-pixels. Because maximum segment of RA8816 is 144-pixels, therefore the range of X[5..0] is 0~11h. When the X[5..0] is 20h or 21h, then the cursor position is assign to horizontal Scroll-Buffer.

[06h] Cursor Position Register of Y (Y-CUR)

| | | | | | | | | |
|----|-----|-----|-----|-----|-----|-----|-----|-----|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | -- | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 | Y0 |

Y[6..0]: Setup the cursor position on common. The unit is 1-pixels. Because maximum common of RA8816 is 64-pixels, therefore the range of Y[6..0] is 0~3Fh. When the Y[6..0] is 40h~4Fh, then the cursor position is assign to vertical Scroll-Buffer. When Y[6..0] is 50h then cursor is located at COMS(lcon).

[07h] Key-scan Control Register (KEYR) (Write Only)

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|------|------|---------------|--------|-----|---------------|---------------|
| 0 | KSB | KDB1 | KDB0 | KSTB_SEL L | K_AUTO | IRE | KF1/ KSTB1 | KF0/ KSTB0 |

KSB: Key-scan control. 0 → Key-scan disable. 1 → Key-scan enable.

KDB[1..0]: Setup the de-bounce times of Key-scan in Auto-Mode. The one time means the time that Key-scan for one loop.

Table 5-7

| KDB1 | KDB0 | Times |
|------|------|-------|
| 0 | 0 | 8 |
| 0 | 1 | 16 |
| 1 | 0 | 32 |
| 1 | 1 | 64 |

KSTB_SEL: In non-Auto-mode, 0 → the DB[1..0] are defined as KF[1..0]. 1 → The DB[1..0] are defined as KSTB[1..0]. In Auto-Mode, the DB[1..0] is also defined as KF[1..0].

K_AUTO: Setup the scan mode. 1 → Auto-Mode. The RA8816 will auto detect the key and store the code into AKD[6..0] for MPU reading. 0 → Non-Auto-Mode. The RA8816 will not store the code to AKD[6..0]. The MPU has to read data from KSTB[1..0] and KSD[4..0] to make sure which key was pressed. Of course, MPU could know if not only one key pressed at the same time In Non-Auto-Mode.

IRE: Setup the Interrupt of Key-scan. 0 → Hardware Interrupt disable while key was pressed. 1 → Generate hardware interrupt while key was pressed.

KF[1..0]: Setup the frequency of Key-scan.

Table 5-8

| KF1 | KF0 | Pulse Width | Key-scan Cycle Time (4x5) |
|-----|-----|-------------|------------------------------|
| 0 | 0 | 256us | 1.024ms |
| 0 | 1 | 512us | 2.048ms |
| 1 | 0 | 1.024ms | 4.096ms |
| 1 | 1 | 2.048ms | 9.182ms |

KSTB[1..0]: In Non-Auto-Mode, These two bits are used to setup the strobe for the Row of key matrix. If any key pressed, the MPU can read data from KSTB[1..0] and KSD[4..0] to make sure which key was pressed. The strobe data are also readable from Bit[6..5] of register KSDR.

[07h] Key-scan Data Register (KSDR) (Read Only)

If K_AUTO = 0:

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|------|-------|-------|------|------|------|------|------|
| 1 | SIRQ | KSTB1 | KSTB0 | KSD4 | KSD3 | KSD2 | KSD1 | KSD0 |

SIRQ: Indicate the interrupt of Key-scan. This bit was clear when REG[0Fh] bit 1 write "0".

KSTB[1..0]: These two bit show which pin of KST[3..0] active.

KSD[4..0]: KIN Return Data. These bits are used in Non-Auto-Mode. The MPU can read data from KSTB[1..0] and KSD[4..0] to make sure which key was pressed.

If K_AUTO = 1:

| | | | | | | | | |
|----|------|------|------|------|------|------|------|------|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 1 | SIRQ | AKD6 | AKD5 | AKD4 | AKD3 | AKD2 | AKD1 | AKD0 |

SIRQ: Indicate the interrupt of Key-scan. This bit was clear when REG[0Fh] bit 1 write “0”.

AKD[6..0]: Scan Data(Code). In Auto-Mode, the MPU read data from this register to know the status of key matrix. The RA8816 supports 4x5 key matrix -- total 20Keys. The BCD number of 0~19h are mapping to these keys.

Table 5-9

| AKD[6..0] | Scan Data |
|-----------|--------------------|
| 0~19 | Key No. Input |
| 20~39 | Long Key No. Input |
| 42 | Key Release |
| Other | Reserved |

[08h] Scroll Window Start X Register (SWSXR)

| | | | | | | | | |
|----|-----|-----|-----|------|------|------|------|------|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | -- | -- | -- | SSX4 | SSX3 | SSX2 | SSX1 | SSX0 |

SSX[4..0]: Setup Segment (X) start point of scroll window. The unit is half size width(8-Pixels).

[09h] Scroll Window Start Y Register (SWSYR)

| | | | | | | | | |
|----|-----|-----|------|------|------|------|------|------|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | -- | -- | SSY5 | SSY4 | SSY3 | SSY2 | SSY1 | SSY0 |

SSY[5..0]: Setup the Common (Y) start point of scroll window. The unit is pixel.

[0Ah] Scroll Window Range X Register (SWRXR)

| | | | | | | | | |
|----|-----|-----|-----|------|------|------|------|------|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | -- | -- | -- | SRX4 | SRX3 | SRX2 | SRX1 | SRX0 |

SRX[4..0]: Setup Segment (X) offset of scroll window. The unit is half size width(8-Pixels).

[0Bh] Scroll Window Range Y Register (SWRYR)

| | | | | | | | | |
|----|-------------|-----|------|------|------|------|------|------|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | PINV | -- | SRY5 | SRY4 | SRY3 | SRY2 | SRY1 | SRY0 |

PINV : Invert area select. 0 → Whole screen invert. 1 → Partial screen invert.

SRY[5..0]: Setup the Common (Y) offset of scroll window. The unit is pixel.

[0Ch] Scroll Offset Register (SCOR)

| | | | | | | | | |
|----|-----|-----|---------|---------|---------|---------|---------|---------|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | SL7 | SL6 | SL5/SR5 | SL4/SR4 | SL3/SR3 | SL2/SR2 | SL1/SR1 | SL0/SR0 |

SL[7..0]: Setup the shift unit of horizontal scroll. The unit is pixel and active when register SCR_MD (REG[0Eh]bit 5) is clear to “0”.

SR[5..0]: Setup the shift unit of vertical scroll. The unit is pixel and active when register SCR_MD (REG[0Eh]bit 5) is set to “1”.

In auto scroll mode, this register is also used to setup the start position of scroll of Common or Segment.
In Non-Auto-Scroll mode, the shift unit of this register cannot over the range of scroll area – REG[08h~0Bh].

[0Dh] Auto-Scroll Control Register (ASCR)

| | | | | | | | | |
|----|------|------|------|------|------|------|------|------|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | SPD3 | SPD2 | SPD1 | SPD0 | STP3 | STP2 | STP1 | STP0 |

SPD[3..0]: Setup the speed of auto scroll.

Table 5-10

| SPD3 | SPD2 | SPD1 | SPD0 | Scroll Time |
|------|------|------|------|-------------|
| 0 | 0 | 0 | 0 | 1 Unit |
| 0 | 0 | 0 | 1 | 3 Units |
| 0 | 0 | 1 | 0 | 5 Units |
| 0 | 0 | 1 | 1 | 7 Units |
| 0 | 1 | 0 | 0 | 17 Units |
| 0 | 1 | 0 | 1 | 19 Units |
| 0 | 1 | 1 | 0 | 21 Units |
| 0 | 1 | 1 | 1 | 23 Units |
| 1 | 0 | 0 | 0 | 129 Units |
| 1 | 0 | 0 | 1 | 131 Units |
| 1 | 0 | 1 | 0 | 133 Units |
| 1 | 0 | 1 | 1 | 135 Units |
| 1 | 1 | 0 | 0 | 145 Units |
| 1 | 1 | 0 | 1 | 147 Units |
| 1 | 1 | 1 | 0 | 149 Units |
| 1 | 1 | 1 | 1 | 151 Units |

1 Unit = 1 Frame Times

STP[3..0]: Setup the shift unit on auto scroll mode.

Table 5-11

| SPD3 | SPD2 | SPD1 | SPD0 | Shift Pixel |
|------|------|------|------|-------------|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 1 | 0 | 3 |
| 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 0 | 0 | 5 |
| 0 | 1 | 0 | 1 | 6 |
| 0 | 1 | 1 | 0 | 7 |
| 0 | 1 | 1 | 1 | 8 |
| 1 | 0 | 0 | 0 | 9 |
| 1 | 0 | 0 | 1 | 10 |
| 1 | 0 | 1 | 0 | 11 |
| 1 | 0 | 1 | 1 | 12 |
| 1 | 1 | 0 | 0 | 13 |
| 1 | 1 | 0 | 1 | 14 |
| 1 | 1 | 1 | 0 | 15 |
| 1 | 1 | 1 | 1 | 16 |

[0Eh] Scroll Control Register (SCCR)

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|--------------|--------------|--------|------|--------------|--------------|---------------|--------------|
| 0 | SCR_IM D1 | SCR_IM D0 | SCR_MD | SBUF | SCR_DI R1 | SCR_DI R0 | SCR_INT EN | AUTO_S CR |

SCR_IMD[1..0]: The definition is as following and they are available at Auto-Scroll-Mode.

0X: Setup 1-pixel shift to caused interrupt(SCR_INTEN must be 1).

10: Setup 8-pixel shift to caused interrupt(SCR_INTEN must be 1)

11: Setup 16-pixel shift to caused interrupt(SCR_INTEN must be 1)

SCR_MD: Scroll Mode Select. 0 → Non-Auto-Scroll, the scroll offset clear to “0”. 1 → Auto-Scroll Mode.

SBUF: Scroll-Buffer Control. 0 → Scroll-Buffer disable. The scroll will not including the Scroll-Buffer, only for display area. 1 → Scroll-Buffer enable. The scroll area is including the display and Scroll-Buffer.

SCR_DIR[1..0]: Select the direction of scroll.

Table 5-12

| SCR_DIR1 | SCR_DIR0 | Direction of Scroll |
|----------|----------|---------------------------|
| 0 | 0 | Left to Right(Horizontal) |
| 0 | 1 | Right to Left(Horizontal) |
| 1 | 0 | Up to Down(Vertical) |
| 1 | 1 | Down to Up(Vertical) |

SCR_INTEN: Setup the scroll interrupt. 0 → Scroll interrupt disable. 1 → In auto scroll mode, when scroll 1, 8 or 16-pixels generate an interrupt to MPU.

AUTO_SCR: Auto-Scroll control. 0 → Stop the Auto-Scroll. If want to close the Auto-Scroll mode or display new data on the screen, then the Bit5 - SCR_MD must clear to 0 first. 1 → Auto-Scroll going.

[0Fh] Interrupt Status Register (ISR)

| | | | | | | | | |
|----|-----|-----|-----|-----|------|-------|-----|-----|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 1 | BF | -- | -- | -- | IO_I | SCR_I | KI | BI |

BF: Busy Flag. 1 → Display RAM is in busy(Data Write). 0 → Display RAM is idle(Write complete).

IO_I: I/O Port Interrupt. 1 → Interrupt for I/O port. 0 → No I/O port interrupt.

SCR_I: Scroll interrupt. 1 → Interrupt for scroll complete. 0 → No scroll Interrupt.

KI: Key-scan interrupt. 1 → Interrupt for key pressed. 0 → No Key pressed Interrupt.

BI: Busy Interrupt. 1 → Interrupt for the activity of writing data to display RAM completed. 0 → No busy Interrupt

[10h] Contrast Adjust Register (CSTR)

| | | | | | | | | |
|----|-----|-----|-----|-----|-----|-----|-----|-----|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | BR2 | BR1 | BR0 | CT4 | CT3 | CT2 | CT1 | CT0 |

BR[2..0]: Setup the LCD Bias(Base on 144x65).

Table 5-13

| BR2 | BR1 | BR0 | Bias |
|-----|-----|-----|------|
| 0 | 0 | 0 | 1/5 |
| 0 | 0 | 1 | 1/6 |
| 0 | 1 | 0 | 1/7 |
| 0 | 1 | 1 | 1/8 |
| 1 | 0 | 0 | 1/9 |
| 1 | 0 | 1 | 1/9 |
| 1 | 1 | 0 | 1/9 |
| 1 | 1 | 1 | 1/9 |

CT[4..0]: Setup the Contrast(32 Level). Normally depend on the liquid, power and panel size to adjust the best display quality.

Table 5-14

| CT4 | CT3 | CT2 | CT1 | CT0 | Contrast |
|-----|-----|-----|-----|-----|----------|
| 0 | 0 | 0 | 0 | 0 | Light |
| 0 | 0 | 0 | 0 | 1 | ↓ |
| ⋮ | | | | | |
| 1 | 1 | 1 | 1 | 1 | |

[11h] Driver Control Register1 (DRCR_A)

| | | | | | | | | |
|----|------|------|------|------|------|-----|------|------|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | BOFF | EN_R | EN_G | ROFF | IDIR | -- | CDIR | SDIR |

- BOFF:** Booster control. 1 → Internal Booster enable. 0 → Internal Booster disabled and used external voltage.
- EN_R:** Reference voltage control. 1 → Internal reference voltage enable for Regulator. 0 → Disable the internal reference voltage. The Regulator use external reference voltage.
- EN_G:** V0 control. 1 → The V0 is generated by internal Regulator. 0 → Use external power for V0, and the EN_R and BOFF have to clear "0"(Off) to reduce power consumption.
- ROFF:** Voltage Follower control. 1 → Internal Voltage Follower enable for LCD Bias voltage. 0 → Disable internal Voltage Follower, and use external voltage to generate LCD Bias voltage. If use external Voltage Follower, then EN_G, EN_R and BOFF have to clear "0"(Off) to reduce power consumption.
- IDIR :** Icon sequence select. 0 → Icon sequence is fixed. 1 → Icon sequence follow the setting of CDIR/SDIR.
- CDIR:** Common sequency select. 0 → Pins COM0~63 are mapping to Common 0~63. 1 → Pins COM0~63 are mapping to Common 63~0.
- SDIR:** Segment sequency select. 0 → Pins SEG0~143 are mapping to Segment 0~143. 1 → Pins SEG0~143 are mapping to Segment 143~0.

[12h] Driver Control Register (DRCR_B)

| | | | | | | | | |
|----|--------|--------|-----|-----|-----|-----|-----|-----|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | CK_BS1 | CK_BS0 | RR2 | RR1 | RR0 | IRS | HD1 | HD0 |

CK_BS[1..0]: Select the clock of Booster. Assume the RC oscillator clock is 100KHz.

Table 5-15

| CK_BS1 | CK_BS0 | Clock of Booster |
|--------|--------|---------------------|
| 0 | 0 | SYS_CLK/2 → 50KHz |
| 0 | 1 | SYS_CLK/4 → 25KHz |
| 1 | 0 | SYS_CLK/6 → 16.7KHz |
| 1 | 1 | SYS_CLK/8 → 12.5KHz |

RR[2..0]: Setup the Resistor Ratio of Regulator. The ratio is $V_{REF} : V_0$. Please refer to Section 6-4-2.

Table 5-16

| RR2 | RR1 | RR0 | Resistor Ratio |
|-----|-----|-----|----------------|
| 0 | 0 | 0 | X3 |
| 0 | 0 | 1 | X3.5 |
| 0 | 1 | 0 | X4 |
| 0 | 1 | 1 | X4.5 |
| 1 | 0 | 0 | X5 |
| 1 | 0 | 1 | X5.5 |
| 1 | 1 | 0 | X6 |
| 1 | 1 | 1 | X6.4 |

Note: The VREF is 2.1V.

IRS: Select the resistors for the V0 voltage level adjustment. 1 → Use the internal resistors. 0 → Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider that is attached to the VR signal.

HD[1..0]: Setup the LCD driving current. Normally big panel use bigger driving current to void bad display quality.

Table 5-17

| HD1 | HD0 | Driving Current |
|-----|-----|-------------------|
| 0 | 0 | Min. ↓ Max. |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

[13h] Blink Timer Register (BLTR)

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|--------|--------|-----|-----|------|------|------|------|
| 0 | BLK_EN | PBK_EN | -- | INV | BLT3 | BLT2 | BLT1 | BLT0 |

BLK_EN: Blinking. 0 → Blinking off. 1 → Blinking on.

PBK_EN: Whole or Partial Blinking selection. 0 → Whole screen Blinking. 1 → Partial screen Blinking. The blinking area is depending on the scroll window. That means the partial area is setting by register SWSXR, SWSYR, SWRXR and SWRYR. When the Partial Blinking off, the above four registers had better clear to 0. Note, only BLK_EN set to “1” when blink is active.

INV: Setup display reverse. 0 → Normal display. 1 → Display reverse. The reverse area is depend on the Bit7(PINV) of register SWRYR.

BLT[3..0]: Setup blinking time.

Table 5-18

| BLT3 | BLT2 | BLT1 | BLT0 | Blink Time (Unit: Frames) |
|------|------|------|------|------------------------------|
| 0 | 0 | 0 | 0 | 8 |
| 0 | 0 | 0 | 1 | 16 |
| 0 | 0 | 1 | 0 | 24 |
| 0 | 0 | 1 | 1 | 32 |
| 0 | 1 | 0 | 0 | 40 |
| 0 | 1 | 0 | 1 | 48 |
| 0 | 1 | 1 | 0 | 56 |
| 0 | 1 | 1 | 1 | 64 |
| 1 | 0 | 0 | 0 | 72 |
| 1 | 0 | 0 | 1 | 80 |
| 1 | 0 | 1 | 0 | 88 |
| 1 | 0 | 1 | 1 | 96 |
| 1 | 1 | 0 | 0 | 104 |
| 1 | 1 | 0 | 1 | 112 |
| 1 | 1 | 1 | 0 | 120 |
| 1 | 1 | 1 | 1 | 128 |

[14h] I/O Direction Control Register (IODR)

| | | | | | | | | |
|----|-----|-----|-----|-----|-----|-----|-----|-----|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | OE7 | OE6 | OE5 | OE4 | OE3 | OE2 | OE1 | OE0 |

OE[7..0]: Select the I/O port direction. 0 → Input. 1 → Output.

[15h] I/O Data Register (IODAR)

| | | | | | | | | |
|----|------|------|------|------|------|------|------|------|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | IOD7 | IOD6 | IOD5 | IOD4 | IOD3 | IOD2 | IOD1 | IOD0 |

IO[7..0]: This register stores the input data of I/O port when I/O port is input mode.

[16h] EL Control Register (ELCR)

| | | | | | | | | |
|----|-------|-----|-----|-----|------|------|------|------|
| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | EL_EN | -- | -- | -- | ELT3 | ELT2 | ELT1 | ELT0 |

EL_EN: EL signals output . 0 → Off. 1 → On.

ELT[3..0]: Setup the output time of EL signals. The following table is base on the RC oscillator fix at 45KHz. The output time is longer when RC oscillator clock is slower.

Table 5-19

| ELT3 | ELT2 | ELT1 | ELT0 | Output Time(Sec) |
|------|------|------|------|------------------|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 1 | 0 | 4 |
| 0 | 0 | 1 | 1 | 6 |
| 0 | 1 | 0 | 0 | 8 |
| 0 | 1 | 0 | 1 | 10 |
| 0 | 1 | 1 | 0 | 12 |
| 0 | 1 | 1 | 1 | 14 |
| 1 | 0 | 0 | 0 | 16 |
| 1 | 0 | 0 | 1 | 18. |
| 1 | 0 | 1 | 0 | 20 |
| 1 | 0 | 1 | 1 | 22 |
| 1 | 1 | 0 | 0 | 24 |
| 1 | 1 | 0 | 1 | 26 |
| 1 | 1 | 1 | 0 | 28 |
| 1 | 1 | 1 | 1 | 30 |

[17h] CGRAM Register (CGMI)

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|------|------|------|
| 0 | -- | -- | -- | -- | -- | UMI2 | UMI1 | UMI0 |

UMI[2..0]: Select the create font number. The RA8816 allow user create eight 16x16 full size font. The mapping font code is FFF0h~FFF7h.

Table 5-20

| UMI2 | UMI1 | UMI0 | Font Code |
|------|------|------|-----------|
| .0 | 0 | 0 | FFF0h |
| 0 | 0 | 1 | FFF1h |
| 0 | 1 | 0 | FFF2h |
| 0 | 1 | 1 | FFF3h |
| 1 | 0 | 0 | FFF4h |
| 1 | 0 | 1 | FFF5h |
| 1 | 1 | 0 | FFF6h |
| 1 | 1 | 1 | FFF7h |

[18h] CGRAM Data Register (CGMD)

| RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | CGMD7 | CGMD6 | CGMD5 | CGMD4 | CGMD3 | CGMD2 | CGMD1 | CGMD0 |

CGMD[7..0]: This register is used to transfer or read the data of 16x16 full size font. The MPU write continuous 32-bytes data of bit-map of 16x16 full size font into this register that after program the REG[17h]. If user want to show the self-create font, just write the two bytes font code to RA8816.

6. Function Description

6-1 MPU Interface

6-1-1 Parallel Interface

The MPU interface of RA8816 supports both 8080 and 6800 series with in 4-Bit or 8-bit bus width. If the “C86” connects to GND, then the MPU is defined as 8080 type interface. If pin “C86” connects to VDD, then it’s defined as 6800 type interface. Refer to the Figure 6-1 and 6-2.

If the pin “BIT4” connects to GND, then the bus width of MPU interface is 8-Bit. If the pin “BIT4” connects to VDD, then the bus width is 4-Bit. And only the DB[3..0] of data bus are available.

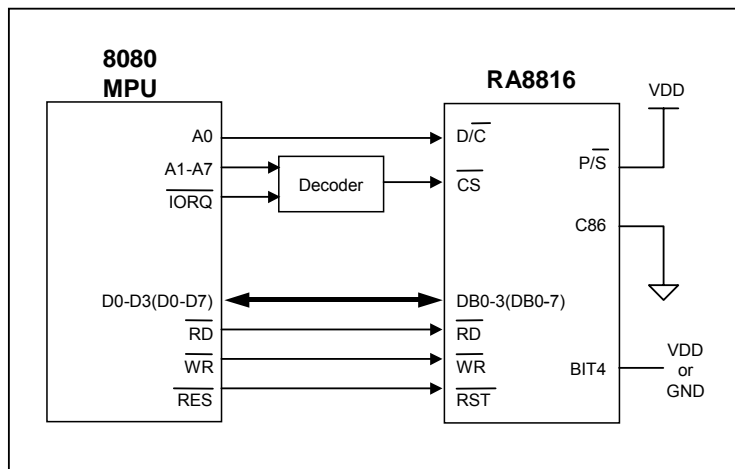


Figure 6-1: 8080 (4/8-Bit) MPU Interface

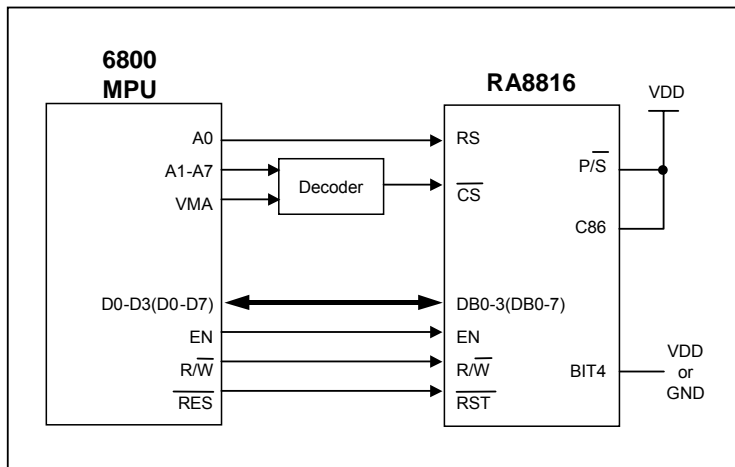


Figure 6-2: 6800 (4/8-Bit) MPU Interface

6-1-2 Serial Interface

The RA8816 also support three type serial interface. One is 3-Wires, one is IIC mode, and the others are 4-Wires(A-Type, B-Type). This feature is control by the pin “P/S” and DB[7..6]. Refer to Table 4-1. In serial mode the DB[7..6] are used as SMOD[1..0] to select the different serial mode. Please also refer to Table 6-1. The Figure 6-3 to 6-5 are the interface diagram of MPU and RA8816 which in serial mode.

Table 6-1

| SMOD | Serial Interface Mode |
|------|---|
| 0 0 | IIC(2-Wire). Use signals SCK, SDA and IICA[5..0] |
| 0 X | 3-Wires. Use signals SCK, SDA and \overline{CS} . |
| 1 0 | 4-Wires (A-Type). Use signals SCK, SDA, RS and \overline{CS} . |
| 1 1 | 4-Wires (B-Type). Use signals SCK, SDO, SDI and \overline{CS} . |

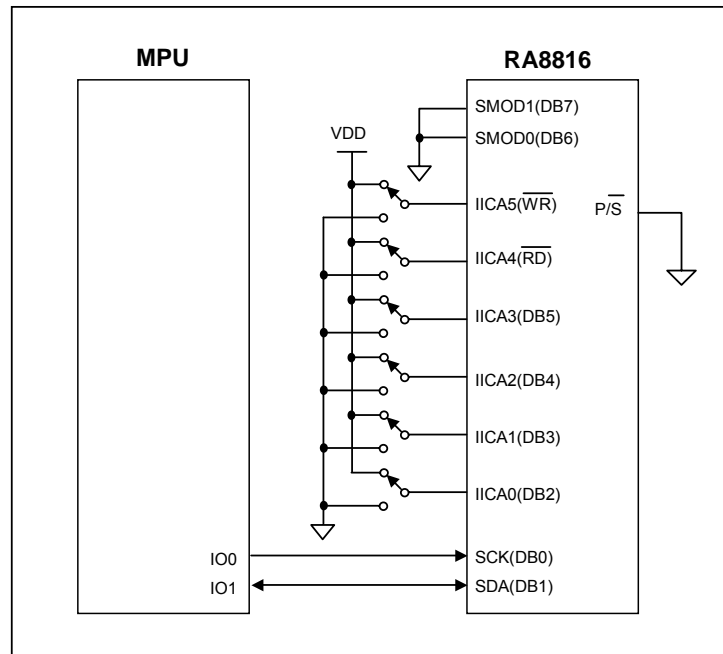


Figure 6-3 : IIC interface Diagram

In the IIC mode, \overline{WR} 、 \overline{RD} and DB[5..2] are consist to the IICA[5..0] for the address selection of IIC Bus device. The address setting is available only not conflict to other device.

In the 4-wire B-Type serial mode, the SCK signal has to add an external pull-up resistor as Figure 6-6.

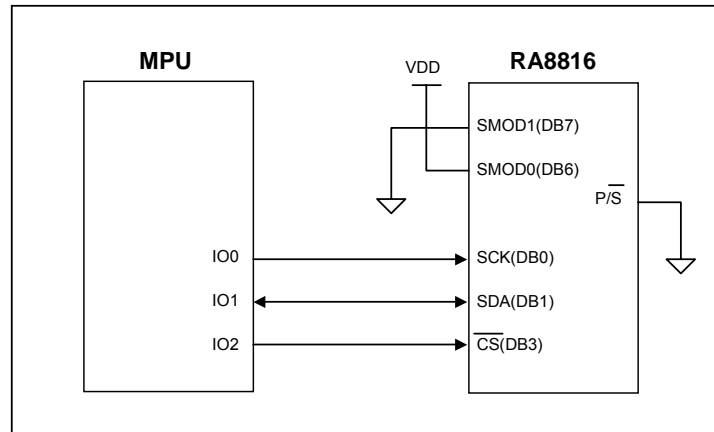


Figure 6-4: 3-Wires MPU interface

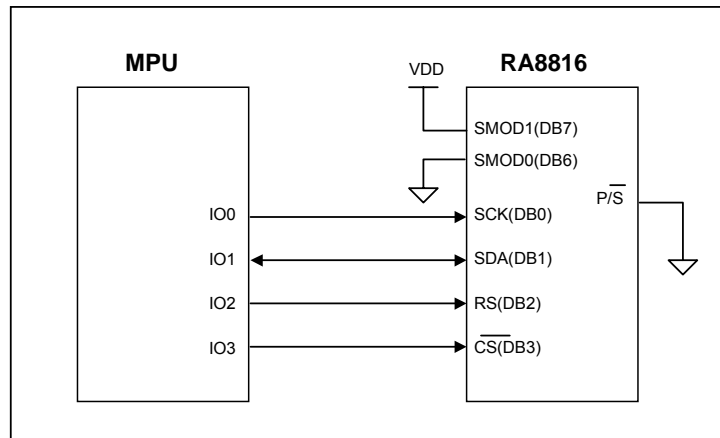


Figure 6-5: 4-Wires(A-Type) MPU interface

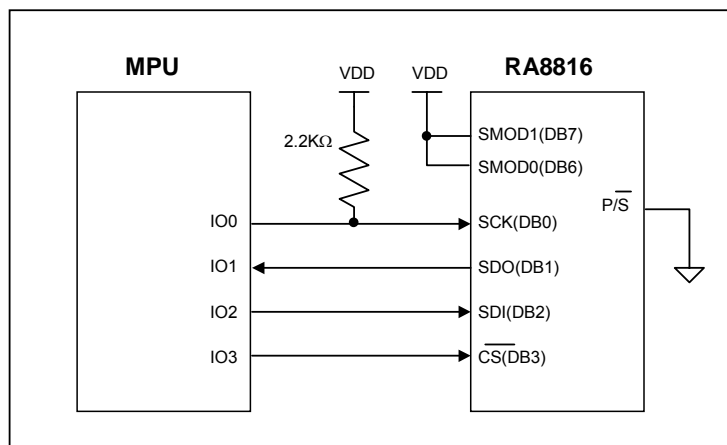


Figure 6-6: 4-Wires(B-Type) MPU interface

6-1-3 Register Read/Write

The RA8816 accepts two access cycles from MPU. One is read data from register or write data to register. Another is read data from memory or write data to memory. As description of Chapter 5-2, MPU must tell the RA8816 that which register will be access. Therefore the first data that write to RA8816 is to select the register number. And the second data is the exact data that writing into or reading from this register.

Because the features of RA8816 are controlled by the contents of internal registers. So if we write data to register is like to give a command to RA8816. Therefore we can say that the Register Access Cycle is same as Command Cycle.

The Figure 6-7 and 6-8 show the register access timing of 8080 MPU(8-Bit) with RA8816. Figure 6-9 and 6-10 show the register access timing of 6800MPU(8-Bit) interface. Figure 6-11 to 6-14 show the register access timing of serial interface.

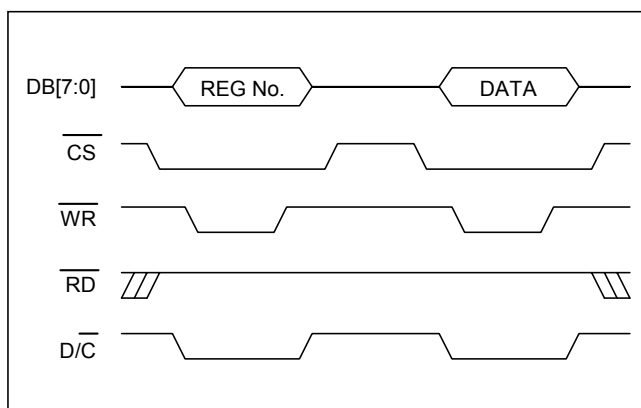


Figure 6-7: Register Write on 8080(8-Bit) I/F

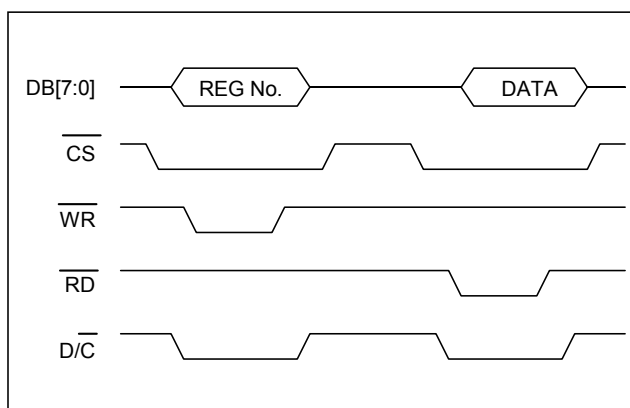


Figure 6-8: Register Read on 8080(8-Bit) I/F

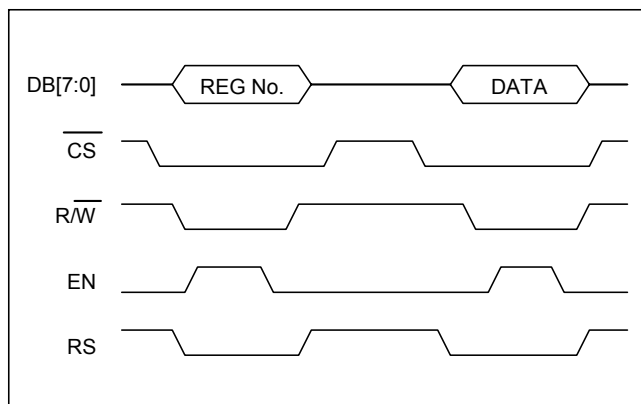


Figure 6-9: Register Write on 6800(8-Bit) I/F

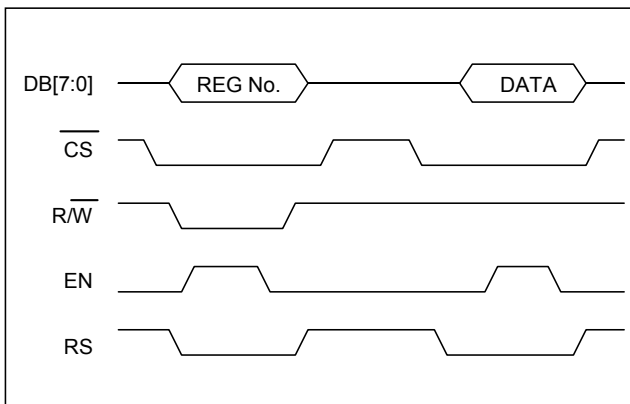


Figure 6-10: Register Read on 6800(8-Bit) I/F

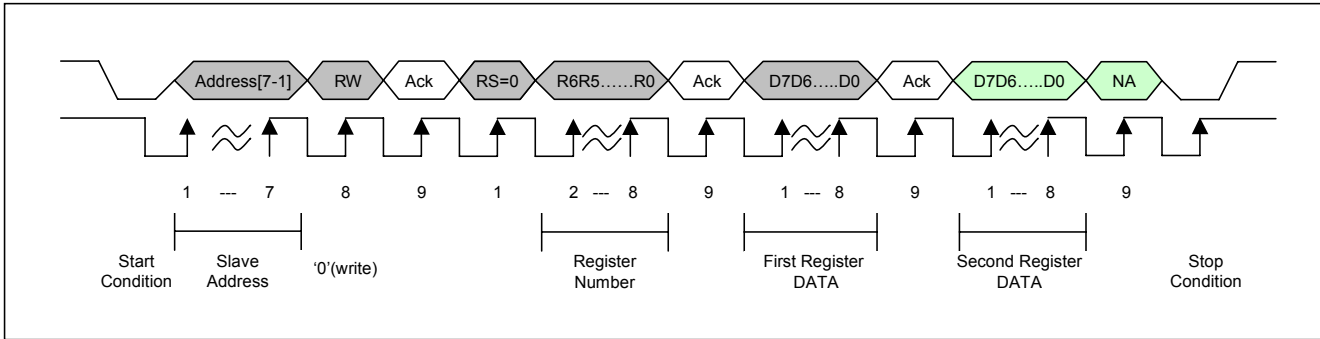


Figure 6-11a : Register Write on IIC I/F

- From Master to Slave
- From Slave to Master
- May be not need

Ack : Acknowledge(SDA LOW)
 NA : Not Acknowledge(SDA HIGH)
 RW : Master Read(1) / Write(0) Command

RS : Select Register(0) / Memory(1)

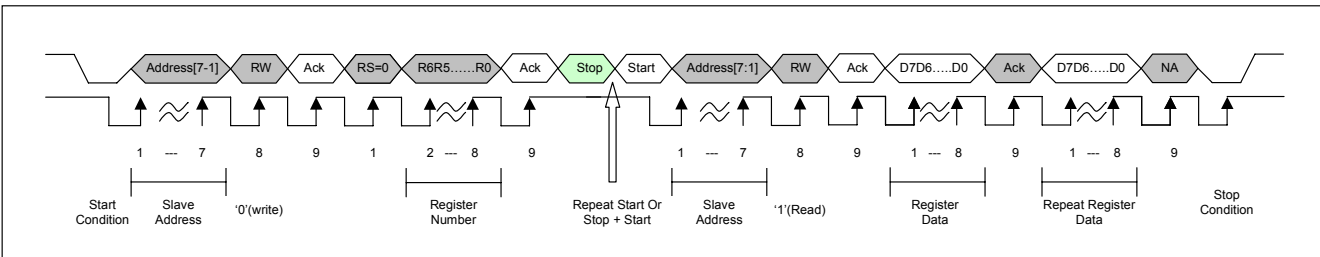


Figure 6-11b : Register Read on IIC I/F

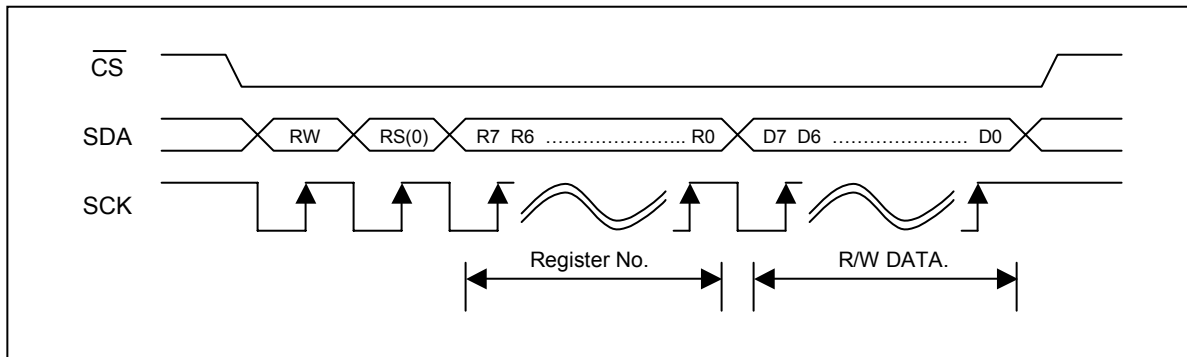


Figure 6-12: Register Read/Write Access on 3-Wires I/F

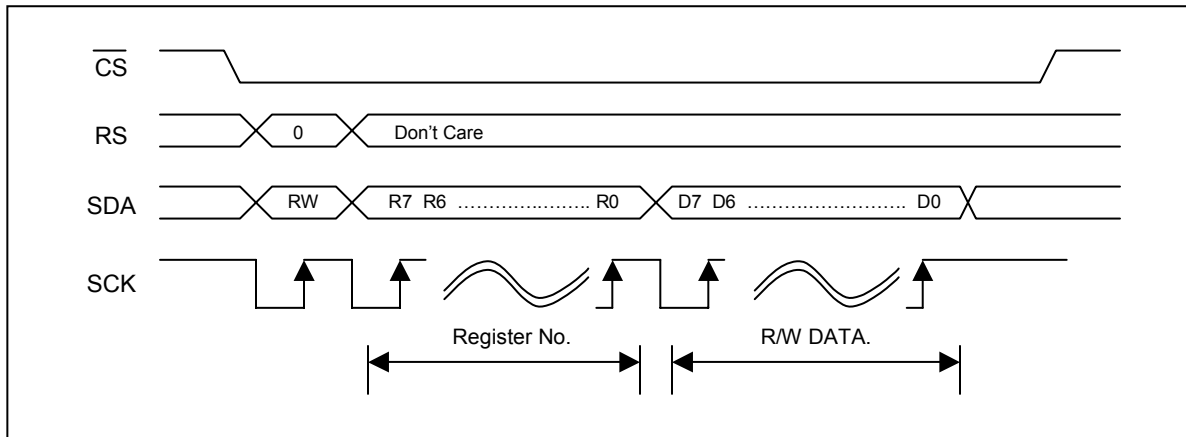


Figure 6-13: Register Read/Write Access on 4-Wires(A-Type) I/F

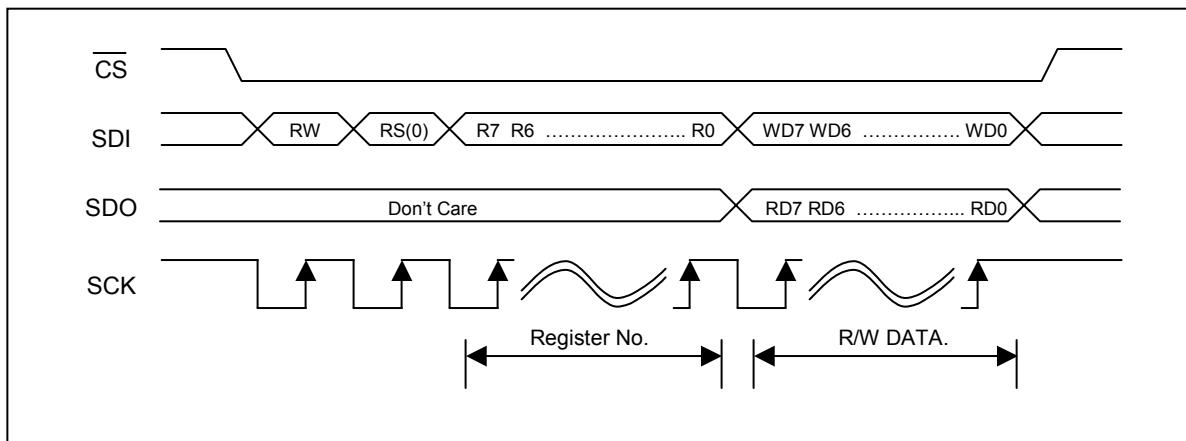


Figure 6-14: Register Read/Write Access on 4-Wires(B-Type) I/F

6-1-4 Memory Read/Write

Another cycle for MPU to RA8816 is memory Read/Write cycle. Normally it used to show information on the LCD screen. A memory writing means to write a data into the mapping address that cursor located in the memory. After a memory writing is completed, the cursor will auto increase. And the data of next memory write will fill into the new memory address that new cursor position located. Because all of the memory read/write cycles are transfer the display data, so we can abbreviate the name of Memory Access Cycle to Data Cycle.

The Figure 6-15 and 6-16 show the memory access timing of 8080 MPU(8-Bit) with RA8816. Figure 6-17 and 6-18 show the memory access timing of 6800MPU(8-Bit) interface. Figure 6-19 to 6-22 show the memory access timing of serial interface.

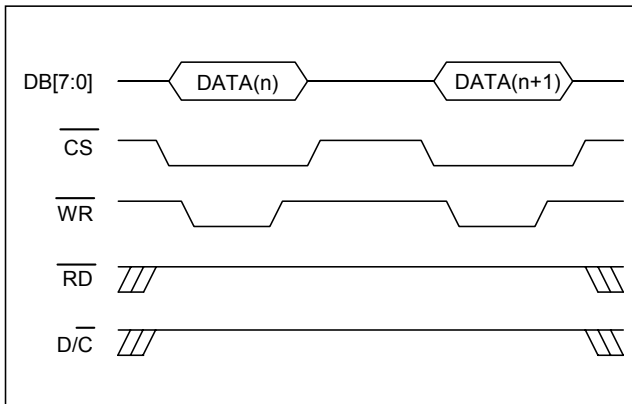


Figure 6-15: Memory Write on 8080(8-Bit) I/F

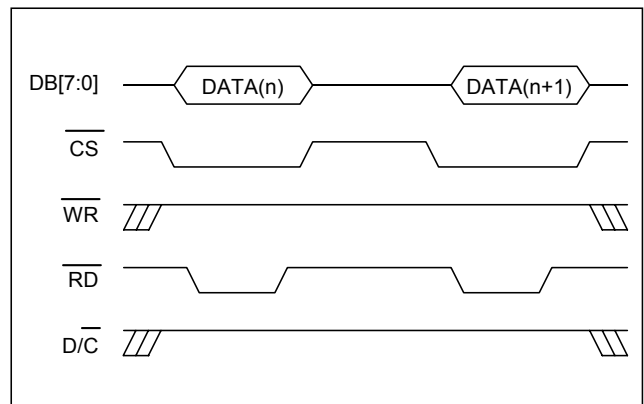


Figure 6-16: Memory Read on 8080(8-Bit) I/F

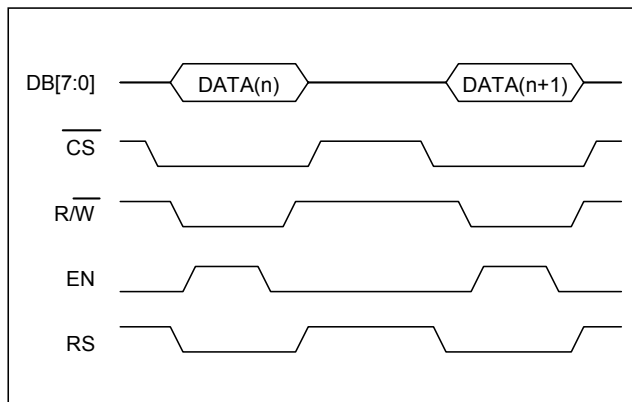


Figure 6-17: Memory Write on 6800(8-Bit) I/F

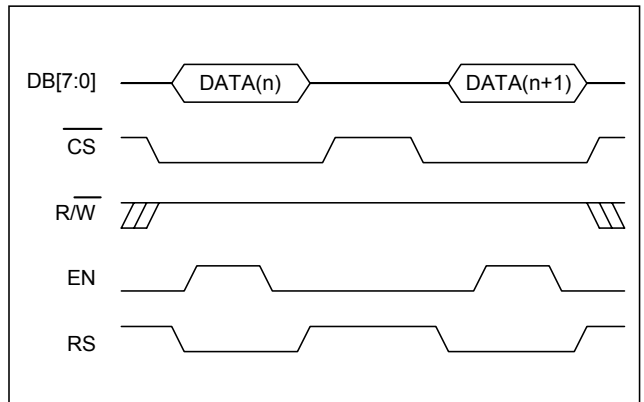


Figure 6-18: Memory Read on 6800(8-Bit) I/F

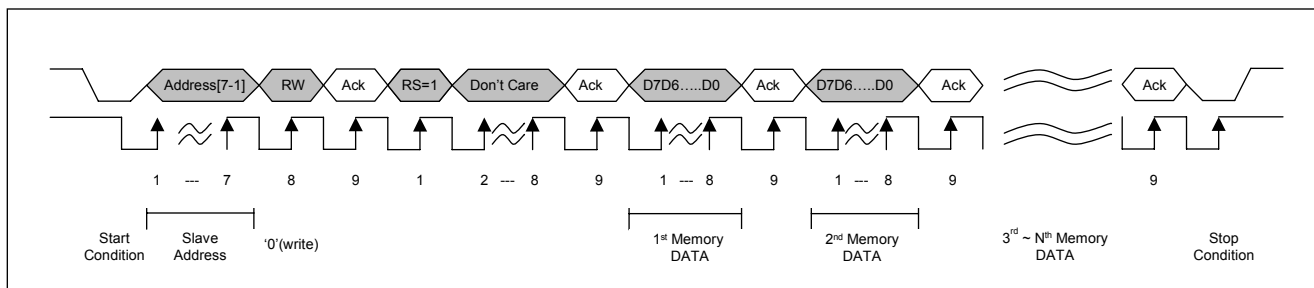


Figure 6-19a : Memory Write Access on IIC

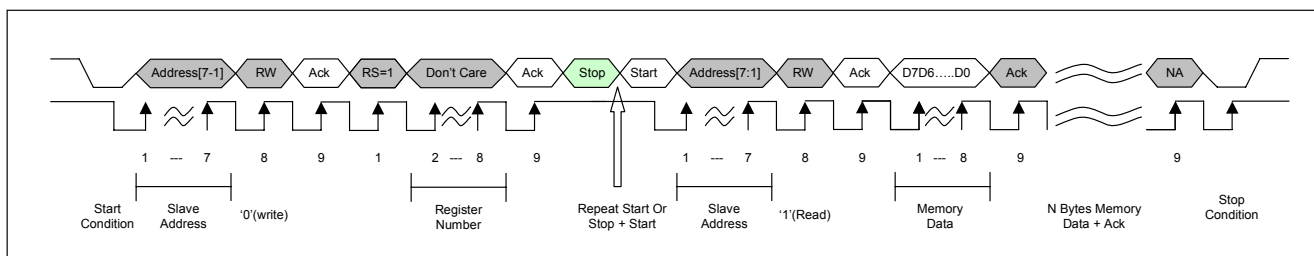


圖 6-19b : Memory Read Access on IIC

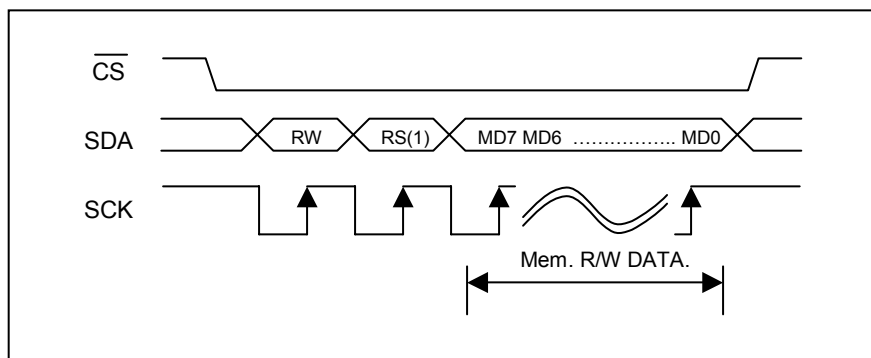


Figure 6-20: Memory Read/Write Access on 3-Wires I/F

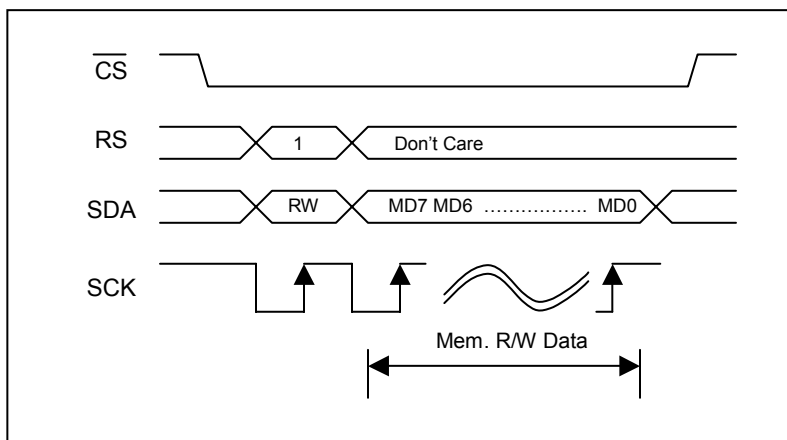


Figure 6-21: Memory Read/Write Access on 4-Wires(A-Type) I/F

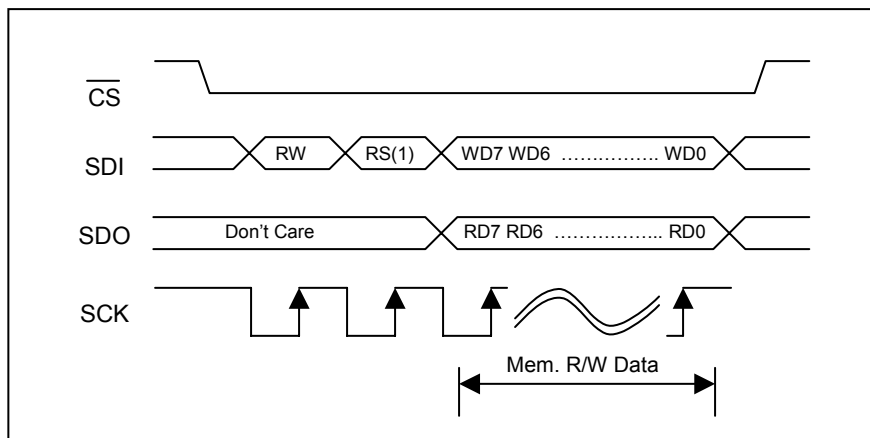


Figure 6-22: Memory Read/Write Access on 4-Wires(B-Type) I/F

6-2 Memory

The RA8816 built-in three memory:

1. 256Kbyte Font ROM
2. [1170Byte Display RAM](#)
3. Character Generator RAM(CGRAM)

The 256Kbyte Font ROM stores bit map data of Chinese font. It also including English, Japanese, European, Latin(Latin-ext A, Latin-ext B) and ASCII. In text mode, RA8816 will read the bit map data from Font ROM and pass to display RAM that when RA8816 received the standard code from MPU. The LCD control circuit will read data of display RAM continuous and send to driver circuit. So the text will show on the LCD screen. Therefore, the MPU will save a lot of time to calculate the position of cursor and read mant bit map data from font ROM then write to display RAM. The MPU will promote the display efficiency to handle Chinese text display. And it will reduce the system develop time.

The display range of RA8816 is 144x65 dots. So it needs 1170Byte(144*65/8) display RAM. In addition, RA8816 also built-in a scroll buffer to provide the scrolling and shifting functions.

The Character Generator RAM(CGRAM) is used for user to create special fonts. There are eight space of full size font to reserved for user. Their codes are fixed from FFF0h to FFF7h. The MPU could write the mapping code to RA8816 and show the bit map font on screen that after the user font(writing 32 byte to CGRAM) was created.

6-3 System Clock

The clock of RA8816 is generated by the internal circuit. Normally the clock frequency is around 55KHz. When the bit0(SLP) of register PWRR set to "1", then the clock will be stop.

When the input pin "CLK_SEL" set to "0", then system clock can also input from external clock through pin "EXT_CLK".

6-4 LCD Driver and Power Circuit

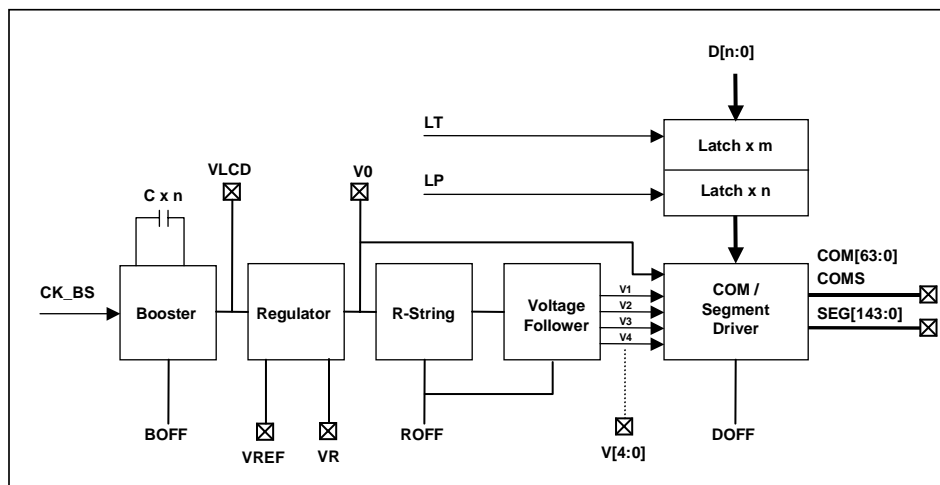


Figure 6-23: LCD Driver and Power Supply Circuit Block

The driver circuit of RA8816 is a low power design. The power supply circuit is consist of Booster, Voltage Regulator and Voltage Follower. For different requirement of power, the Driver Control Register(REG[11h]) is used to enable or disaable for related circuit.

The user could use the setting of register REG[11h] to select the internal or external power. Please refer to the following of Table 6-2.

Table 6-2: Setting Table of Power Circuit

| Driver Control Register (DRCR_A) | | | | Booster | Voltage Regulator | Reference Voltage(VREF) of Voltage Regulator | Voltage Follower | External Power |
|----------------------------------|----|----|----|---------|-------------------|--|------------------|-----------------|
| D7 | D6 | D5 | D4 | | | | | |
| 1 | 1 | 1 | 1 | ON | ON | Internal | ON | VDD |
| 0 | 1 | 1 | 1 | OFF | ON | Internal | ON | VLCD, VDD |
| 1 | 0 | 1 | 1 | ON | ON | External | ON | VREF, VDD |
| 0 | 0 | 1 | 1 | OFF | ON | External | ON | VLCD, VREF, VDD |
| 0 | 0 | 0 | 1 | OFF | OFF | Don't Need | ON | V0, VDD |
| 0 | 0 | 0 | 0 | OFF | OFF | Don't Need | OFF | V0~V4, VDD |

6-4-1 Booster Circuit

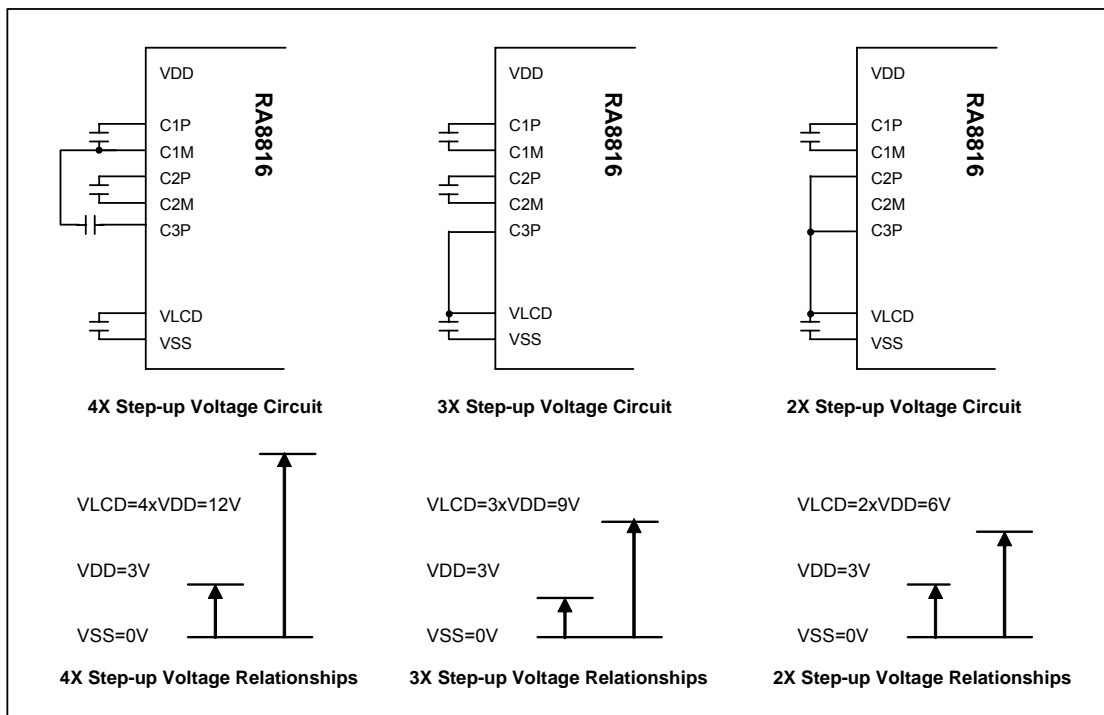


Figure 6-24: Application circuit of Booster

The RA8816 built-in a Booster which create 2~4 times of “ $V_{DD}-V_{SS}$ ” that we called “VLCD”. The VLCD is supply the power for next stage circuit – Voltage Regulator and internal Driver circuit. If connect an 1uF capacitor on pin C1P and C1M, then the VLCD is equal to 2*VDD. If the pin C2P and C2M also connect n 1uF capacitor then the VLCD is 3*VDD. If the pin C3P and C1M connect n 1uF capacitor then the VLCD is 4*VDD. Refer to the following description of Figure 6-24.

Because the RA8816 supports maximum LCD panel is 144x65. Therefore sometimes you can get the good display quality that base on lower power such as 5V only. In that case, user only need to connect 5V to VDD, VLCD, C1P and C2P. And you do not need to add capacitor on C1P/C1M and C2P/C2M.

The clock source of Booster is also control by register DRCR_B. Please refer to the description of REG[12h] in Chapter 5-2. Normally, if use the internal Driver Power, then the application circuit is follow Figure 6-25. If use external VLCD, that means do not use the internal Booster, then the connection is show as Figure 6-26.

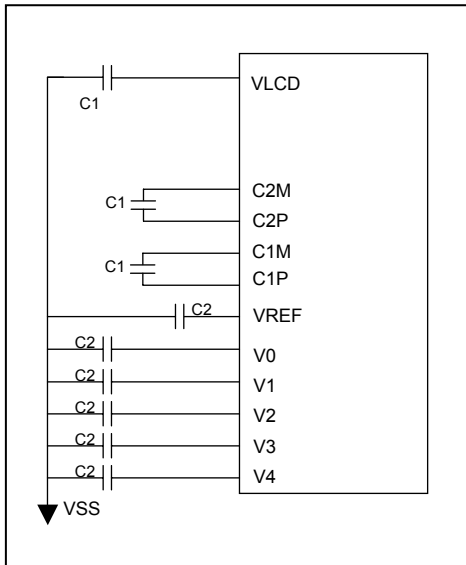


Figure 6-25: Internal VLCD(3*VDD)

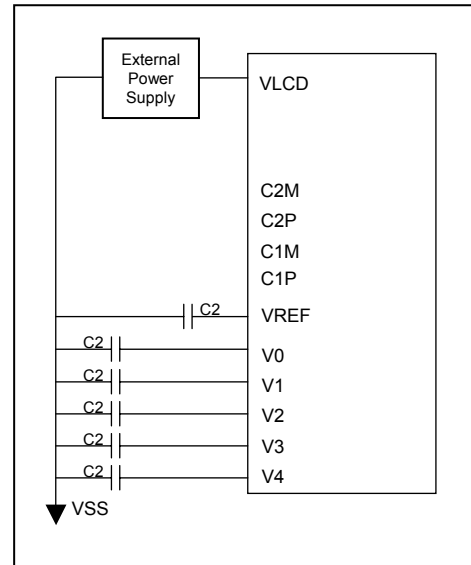


Figure 6-26: External VLCD

Note: The capacitor value of C1 is 1uF and C2 is 1uF.

6-4-2 Voltage Regulator

The Voltage Regulator is consists of Band-Gap and OP-Amp. The purpose is used to generated a stable power - V_0 for Voltage Follower. The RA8816 also built-in a 32-level adjust circuit and a fixed voltage - V_{IREF} to generate a reference voltage V_{REF} . This V_{REF} is for for Voltage Regulator to generated V_0 . The basic formula is as following:

$$V_0 = (1+R1/R2) * V_{REF} = (1+R1/R2)*(1-(62-2\alpha)/162)*V_{IREF}$$

The α is the setting of CT[4:0] of Register CSTR. When CT[4:0]=1Fh then $V_{REF}=V_{IREF}$.

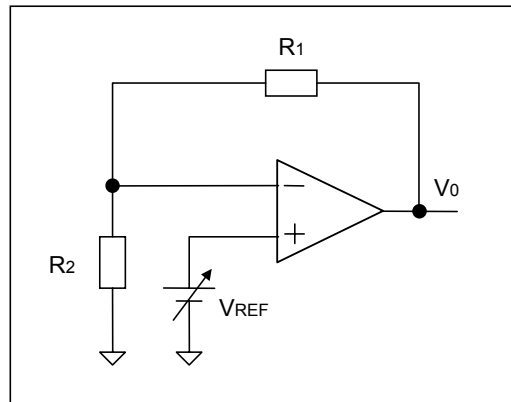


Figure 6-24: Voltage Regulator

The resistor ratio(V_{REF} and V_0) of Voltage Regulator is adjustable by register DRCCR_B. There are total eight cases - 3/3.5/4/4.5/5/5.5/6/6.4. Refer to the description of Bit[5..3] of register RCR_B on Chapter 5-2. If want to use external resistor divisor then refer to the Bit2 of register DRCCR_B and Figure 6-27b.

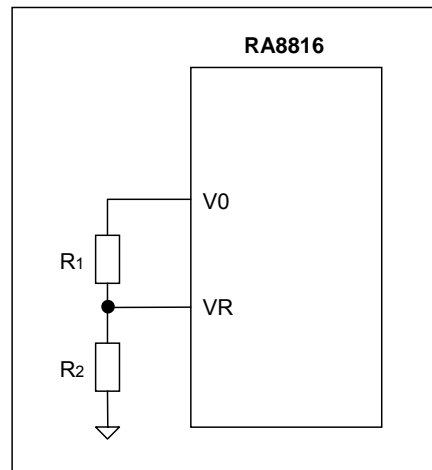


Figure 6-27b: Use external Resistor Divisor

The V_{REF} of RA8816 is supplied from internal circuit or external V_{REF} Pin. Please refer to Table 6-3:

Table 6-3: Select V_{REF}

| V _{REF} Type | DRCR-A Bit6 (EN_R) | DRCR-A Bit5 (EN_G) | Temperature Gradient | Unit | V _{REF} |
|---------------------------|--------------------|--------------------|----------------------|------|--------------------------------|
| Internal V _{REF} | 1 | 1 | -0.05 | %/°C | $(1-(63-\alpha)/162)*V_{IREF}$ |
| External V _{REF} | 0 | 1 | - | - | V _{REF} Pin |
| | X | 0 | - | - | |

Normally the internal V_{IREF} value is 2.1V. When Voltage Regulator Circuit off(EN_G=0) then the Reference Voltage Circuit is be off too. The Voltage Regulator also provide -0.05% auto adjust for temperature compensation.

6-4-3 Voltage Follower

The internal Voltage Follower provides V0~V4 power for LCD Driver circuit. Of course, the user could select internal or external Voltage Follower. The relationship of V0~V4 and VLCD is as following:

$$VLCD > V0 > V1 > V2 > V3 > V4 > GND$$

Figure 6-28A shows the circuit of using internal Voltage Follower. For external V0~V4, the connection is show as Figure 6-28B.

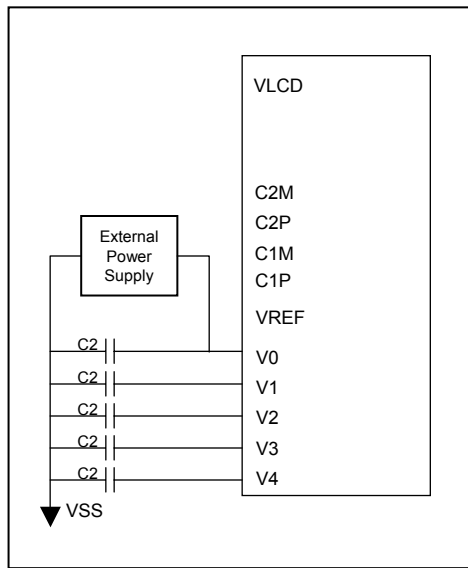


Figure 6-28A: Use Internal Voltage Follower

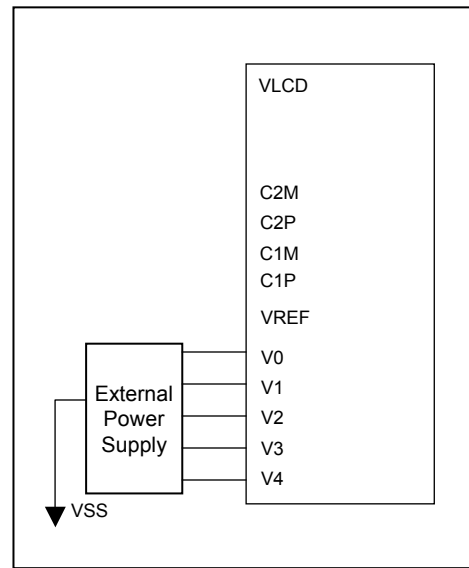


Figure 6-28B Use External Voltage Follower

6-4-4 LCD Driver

The Segment/Common Driver of RA8816 is used to latch the data of pre-stage, then send to Level Shifter for combination. The combined data will follow the Timing Generator to control the switches then pass the V0~V4 to Common and Segment.

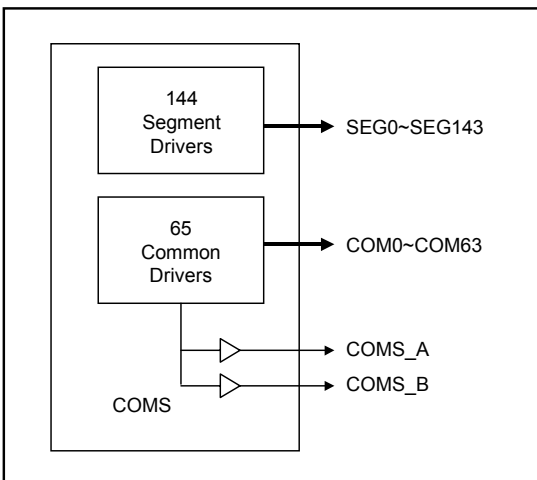


Figure 6-29: The Segment and Common Driver

The LCD Bias of RA8816 is adjustable by register CSTR that from 1/5 to 1/9. The user can also adjust the display quality from this register. Meanwhile, the driving current is also adjustable by register DRCR_B that in order to meet different panel.

The DOFF_Z of register PWRR is used to control the On/Off of LCD Panel, When DOFF_Z is set to "0" then LCD Driver was closed. At this state, the driver output signals COM0~COM63, SEG0~SEG143, COMS_A and COMS_B are connected to GND, and the screen of LCD Panel turned Off.

6-5 Interrupt

The RA8816 provide an interrupt signal(\overline{INT}) to response three possible interrupt:

- ◆ Busy Interrupt– When the data write to display RAM was complete.
- ◆ Scroll Interrupt - When the scroll window shifted 1, 8 or 16-pixels.
- ◆ Key-scan Interrupt - When a key was pressed.

The interrupt of above can be enabled or disable by register. The MPU can read the interrupt message form interrupt status register. The \overline{INT} is active low, so when MPU detect the interrupt happen then must clear interrupt status for \overline{INT} return to high. If user do not use the hardware interrupt(\overline{INT}), then MPU can get the interrupt message by reading the status register.

6-6 Key-Scan

The RA8816 built-in 4x5 key-scan circuit for extra key board function to help user integrate a key matrix application. In auto-mode, MPU can read the key code from register to know the key was short-press, long-press or key released. User can also adjust the cycle time of key-scan. Figure 6-30 is the simple application circuit. Table 6-4 is the mapping keyboard code of key matrix as Figure 6-30. So MPU knows which key be pressed by reading register – KSDR.

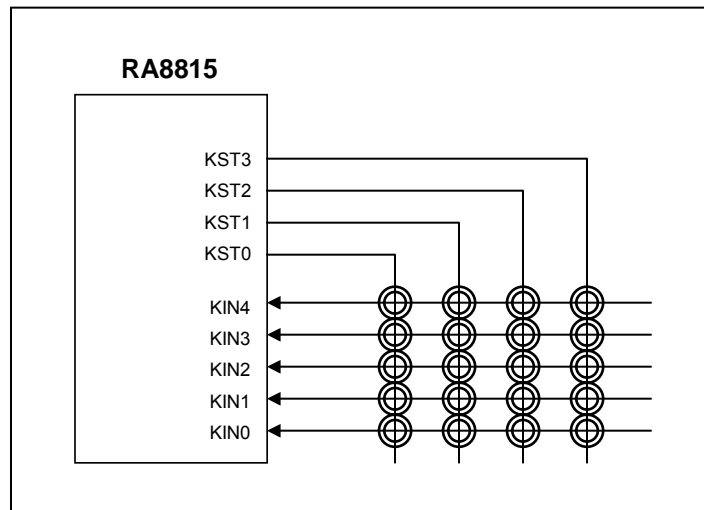


Figure 6-30: 4x5 Key Matrix Circuit

Table 6-4: Keyboard Code(BCD Code) of Auto-Mode

| | Short-Press | | | | Long-Press | | | |
|------|-------------|------|------|------|------------|------|------|------|
| | KST3 | KST2 | KST1 | KST0 | KST3 | KST2 | KST1 | KST0 |
| KIN0 | 15 | 10 | 05 | 00 | 35 | 30 | 25 | 20 |
| KIN1 | 16 | 11 | 06 | 01 | 36 | 31 | 26 | 21 |
| KIN2 | 17 | 12 | 07 | 02 | 37 | 32 | 27 | 22 |
| KIN3 | 18 | 13 | 08 | 03 | 38 | 33 | 28 | 23 |
| KIN4 | 19 | 14 | 09 | 04 | 39 | 34 | 29 | 24 |

In Auto-Mode of Key-Scan function, if the key pressed over one second, then the RA8816 will cause interrupt and change the data of register – KSDR to a long-press code. Therefore MPU knows which key was pressed over one second.

6-7 I/O Port

The RA8816 provide eight general purpose I/O pins. Each I/O pin is easy to setup as input or output. They can use to drive LED, wakeup the RA8816 or provide information for whole system.

6-8 EL Signals

The RA8816 provides two special signals for EL driver circuit. The signals active time can also setup by register ELCR. The waveform and application are show as Figure 6-31 and 6-32.

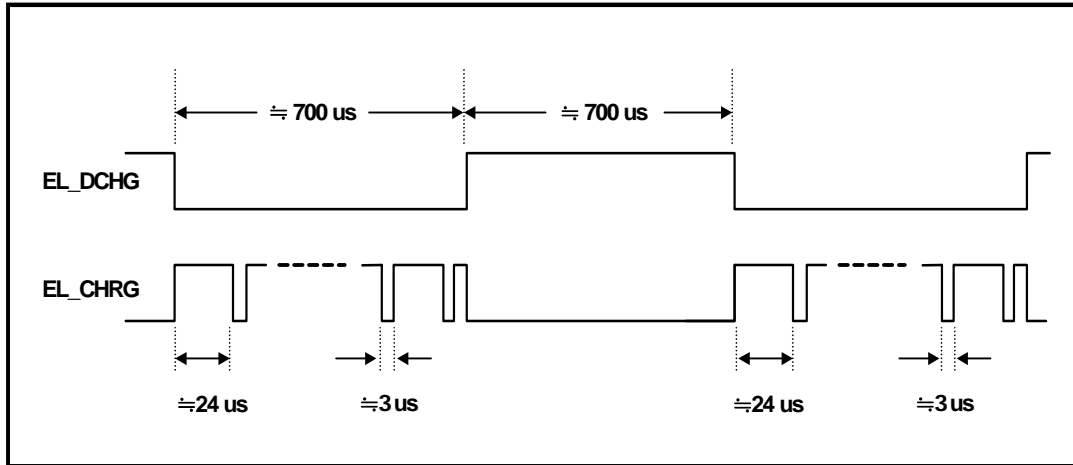


Figure 6-31: Control Signals for EL Driver

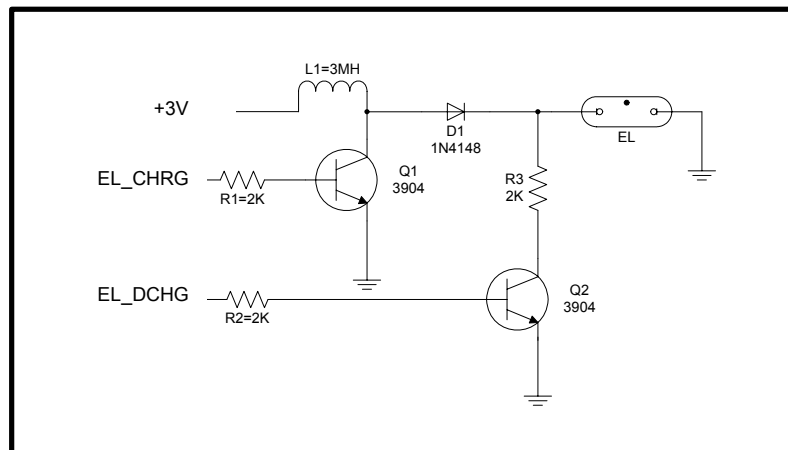


Figure 6-32: EL Driver Circuit

6-9 ASCII Block

The RA8816 built-in three ASCII block which contains ASCII and special symbol for user to show on display directly in text mode. Actually these three ASCII block are stored in 256Kbyte Font ROM (see Chapter 6-2). As the Figures 6-33~6-35, the left of each table is the High Nibble, and the right is the Low Nibble. The selection of these blocks is by MD0 and MD1 of register MWMR.

The Figure 6-33 is the table of small ASCII. Each character size is 8x8 dots. Therefore if the LCD panel size is 144Segx65Com then it can show eight rows, and each row has 18 small ASCII font. Figure 6-34 and 6-35 are the tables of big ASCII. For the same panel size, it can show four rows, and each row has 18 characters.

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0 | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ |
| 1 | ▶◀ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ |
| 2 | ! | " | # | \$ | % | & | ' | (|) | * | + | , | - | . | / | |
| 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | : | ; | < | = | > | ? |
| 4 | @ | A | B | C | D | E | F | G | H | I | J | K | L | M | N | O |
| 5 | P | Q | R | S | T | U | V | W | X | Y | Z | [| \ |] | ^ | _ |
| 6 | ` | a | b | c | d | e | f | g | h | i | j | k | l | m | n | o |
| 7 | p | q | r | s | t | u | v | w | x | y | z | { | | } | ~ | |
| 8 | đ | á | é | á | á | á | á | á | é | é | é | í | í | í | á | á |
| 9 | é | é | é | é | é | é | é | é | é | é | é | é | é | é | é | é |
| A | á | í | ó | ú | ñ | ñ | á | á | á | á | é | é | é | é | í | í |
| B | í | í | ó | ó | ó | ó | ó | ó | ó | ó | ó | ó | ó | ó | ó | ó |
| C | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |
| D | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |
| E | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |
| F | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |

Figure 6-33: Small ASCII (Table 0)

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0 | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ |
| 1 | ▶◀ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ |
| 2 | ! | " | # | \$ | % | & | ' | (|) | * | + | , | - | . | / | |
| 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | : | ; | < | = | > | ? |
| 4 | @ | A | B | C | D | E | F | G | H | I | J | K | L | M | N | O |
| 5 | P | Q | R | S | T | U | V | W | X | Y | Z | [| \ |] | ^ | _ |
| 6 | ` | a | b | c | d | e | f | g | h | i | j | k | l | m | n | o |
| 7 | p | q | r | s | t | u | v | w | x | y | z | { | | } | ~ | |
| 8 | đ | á | é | á | á | á | á | á | é | é | é | í | í | í | á | á |
| 9 | á | á | á | á | á | á | á | á | á | á | á | á | á | á | á | á |
| A | á | í | ó | ú | ñ | ñ | á | á | á | á | é | é | é | é | í | í |
| B | í | í | ó | ó | ó | ó | ó | ó | ó | ó | ó | ó | ó | ó | ó | ó |
| C | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |
| D | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |
| E | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |
| F | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |

Figure 6-34: Big ASCII (Table 1)

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0 | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ | ☉☉ |
| 1 | ▶◀ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ | ◀▶ |
| 2 | ! | " | # | \$ | % | & | ' | (|) | * | + | , | - | . | / | |
| 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | : | ; | < | = | > | ? |
| 4 | @ | A | B | C | D | E | F | G | H | I | J | K | L | M | N | O |
| 5 | P | Q | R | S | T | U | V | W | X | Y | Z | [| \ |] | ^ | _ |
| 6 | ` | a | b | c | d | e | f | g | h | i | j | k | l | m | n | o |
| 7 | p | q | r | s | t | u | v | w | x | y | z | { | | } | ~ | |
| 8 | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |
| 9 | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |
| A | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |
| B | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |
| C | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |
| D | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |
| E | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |
| F | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ | ☉ |

Figure 6-35: Big ASCII (Table 2)

6-10 Power Control

The RA8816 supports Normal Mode and Sleep Mode for operation. If write "0" to bit0 of register PWRR, then RA8816 will enter sleep mode. The functions of LCD display and driver will stop. All of the signals of COM and SEG will keep low, Key Strobe signals will keep high, and I/O keep the original state. Because the RC clock was stop, so the power consumption is very low.

The RA8816 provide three way to wake up the system:

1. Write "1" to the bit0 of register PWRR.
2. Key-scan to wake up
3. I/O wake up

In wake up phase, the RA8816 will wake up the RC oscillator first, and it will take around 250ms. Then the RA8816 is enable to accept the command from MPU and LCD driver wake up for activity.

The VDD power operation range of RA8816 is 2.5~3.6V. But on the COG module, some power consumption will lose on the connection of FPC and chip that due to the ITO layout issue. So normally the VDD power range of COG module on the FPC side is around V2.7~3.8V.

7. Display Functions

7-1 Text Mode

The RA8816 built-in a 256KB Font ROM that including Traditional Chinese or Simplified Chinese, English, Japanese, ASCII, European and Latin(Latin-ext A, Latin-ext B). In text mode, it supports full-size font(Chinese or English) display or half-size(English) display. The full-size font is consist of 16x16 bit map. And half-size is consist of 8x16 or 8x8. Refer to the following Figure 7-1:

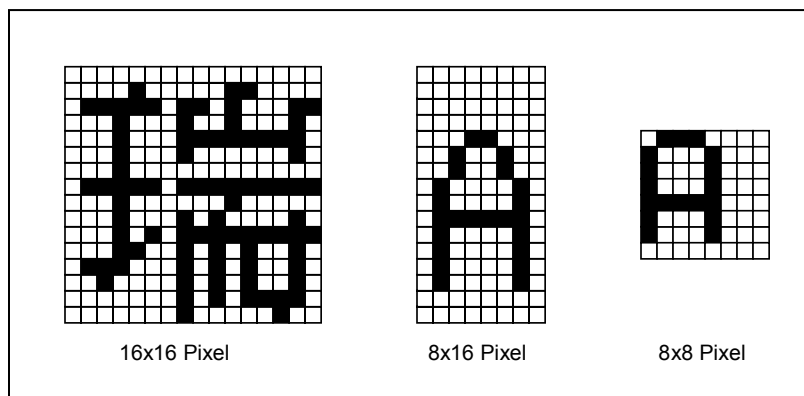


Figure 7-1: Full-Size and Half-Size Font

The Chinese display is operating at text mode. So if the RA8816 received two Chinese codes(BIG5 or GB) then the mapped font will show on the cursor position. Because each Chinese code including two bytes data, therefore the MPU has to send the code twice – High byte and Low byte. For English or Numeric, only one byte is need. The maximum supports panel size of RA8816 is 144x65dots. So in text mode it could show 9x4 Chinese fonts and 18x8 English fonts.

The register MWMR is used to setup the font size for display. The user can also select the different display mode such as bold, inverse or normal mode in this register.

7-2 Graphic Mode

In the graphics mode, the RA8816 is fill the bit map data into display memory directly. So if the [MD1, MD0] of register is set to "00" (Graphics Mode), then write the data into memory, the data will show on the screen that cursor pointed.

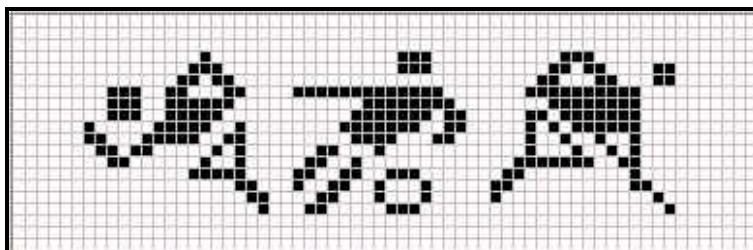


Figure 7-2: Graphics Mode Display

The display RAM size of RA8816 is 1170Byte(144*65/8). Each memory bit is mapping to the LCD panel. If the data is "1" then the mapped dot is turn on. Please refer the Figure 7-3.

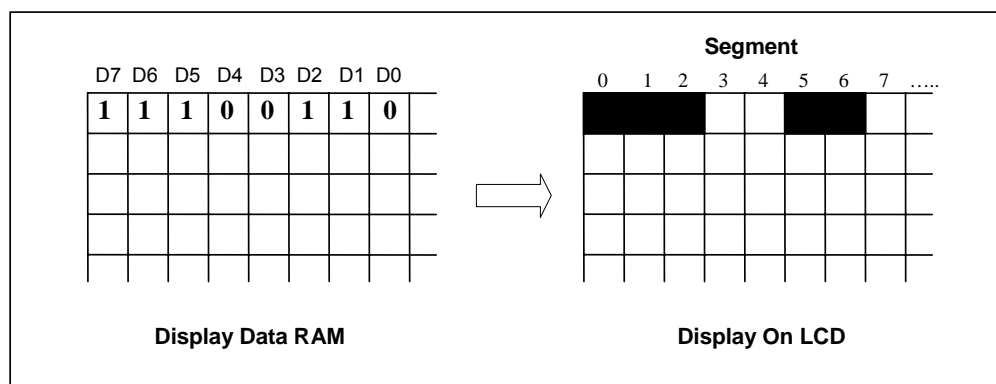


Figure 7-3: Display Data Mapping to the Screen

The RA8816 also provide a clean feature to clear all of the display RAM. If the "MCLR" of register PWRR is set to "1", then all of contents of Display RAM will be clear to "0". In the graphics mode, the user could select the blinking or inverse through register BLTR. The blinking are is assigned by the size of Scroll Window.

7-3 Cursor Setting

7-3-1 Cursor Position and Shift

The unit of Segment Address is 8-Bit, Common is 1-Bit. For example, if user want to show a font “制” on the third position(full-size) of top, then the register X-CUR has to set 04h and Y-CUR set to 00h. If the second row want to show “器” as Figure 7-4, then the X-CUR set to 00h and Y-CUR set to 10h.

Both of text mode and graphics mode, the cursor position are use the same resgister X-CUR and Y-CUR. If fill data to display RAM or show a Chinese font on the screen, the cursor will auto increase, and the boundary is the display window.

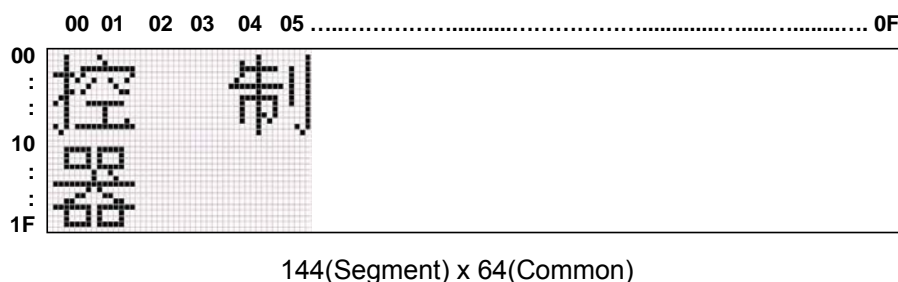


Figure 7-4: An Example for Cursor Setting

7-3-2 Cursor Display and Blink

The RA8816 provides cursor On/Off and blinking features. These functions are control by register CURCR. The cycle time of blinking is depend on the setting of register BLTR. The range is from 8 to 128 frames.

7-3-3 Cursor Height

The cursor height is also setting by register CURCR. For full-size mode the cursor height is adjustable from 1 to16 pixels, and half size is form 1 to 8 pixels. Please refer to Figure 7-5.

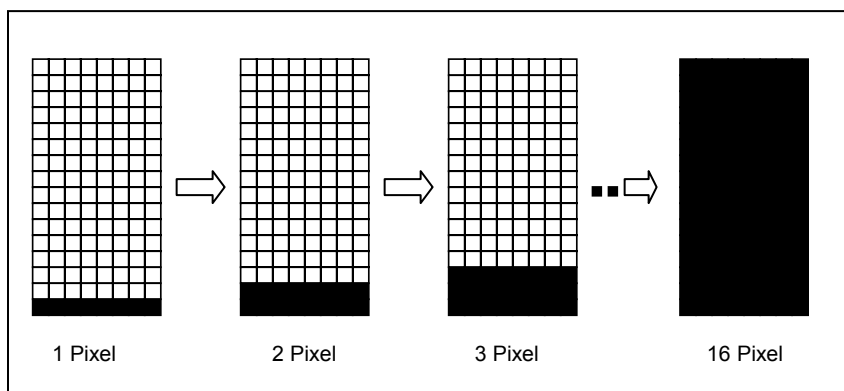


Figure 7-5: Cursor Height

7-4 Display Window

Normally, the Display Window size is same as LCD panel. It's setting by register SYSR. The maximum range is 144(Segment)x64(Common). The RA8816 provide a extra Common(Com-S) as the selection of Icon. Therefore the total 144 Icon for usage. Before access the Com-S, the register Y-CUR has set to 50h, then program the X-CUR to select Icon.

The RA8816 provides two positions for the panel layout of COM-S. It's convenient for user to deisgn the position of Icon for their application. Refer to the Figure 7-6.

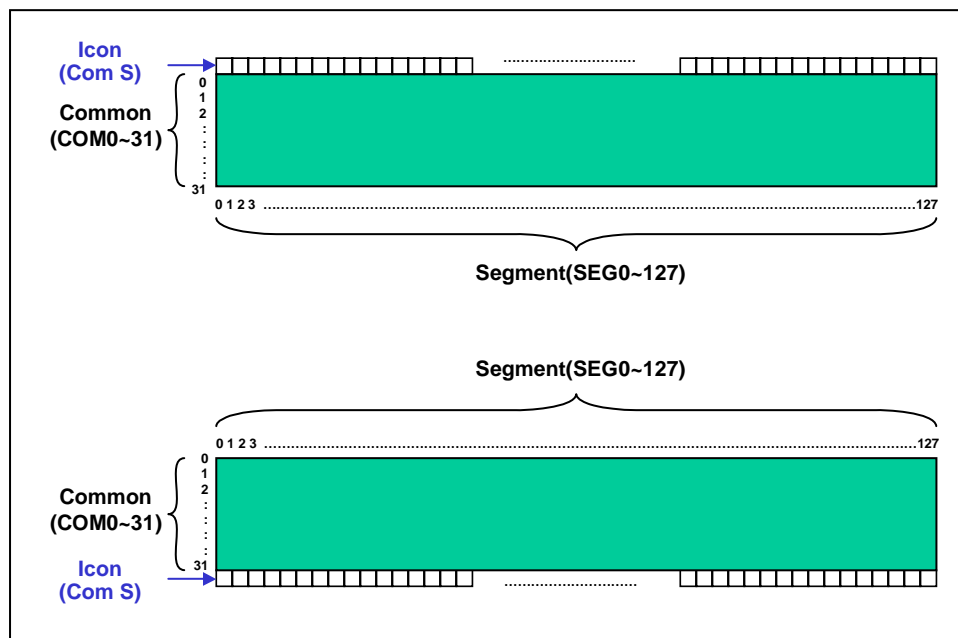


Figure 7-6: Display Window and Icon

7-5 Horizontal Scroll

The RA8816 provides Horizontal Scroll feature. User could assign the range of scrolling, scroll unit and speed. Refer to the following example as Figure 7-7. The scroll unit is set to 2 pixels.

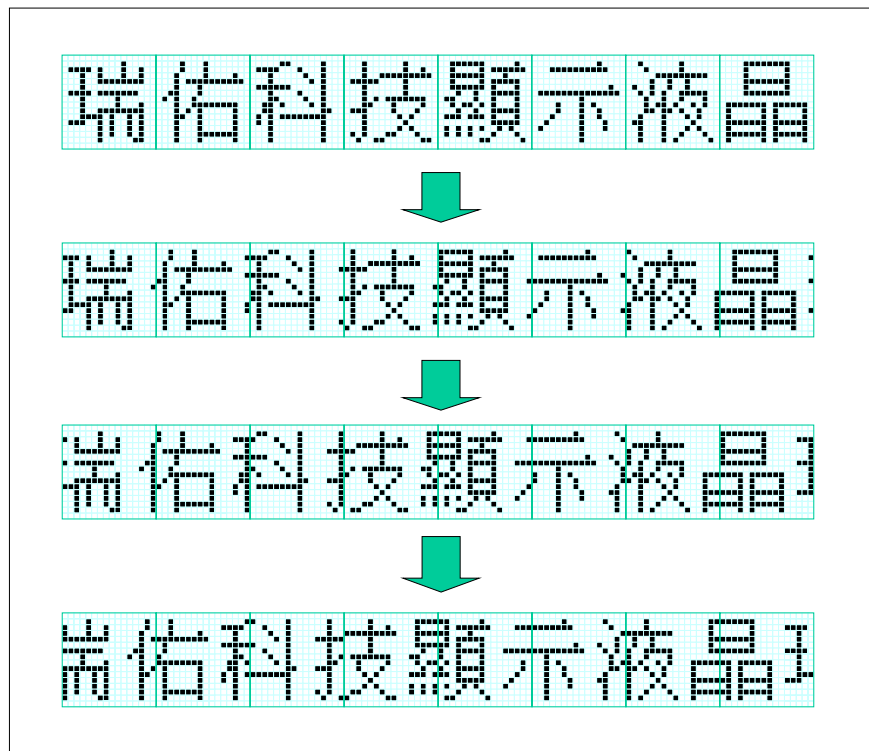


Figure 7-7: Horizontal Scroll

The RA8816 allows horizontal scroll for right or left way. The user could use the scrolling buffer to show the Shift function. For example, store the data or text on the Horizontal Scroll Buffer first, then fill the new data/text into the buffer that after the screen shift 16pixels. You can repeat these action and find the screen is shift like caption of advertisement. The Figure 7-8 is an example to show the Horizontal Shift. The shift unit is 8pixels and the gray area is the scroll buffer. The display data will not show on the screen.

Please refer to application note for the related horizontal scroll feature.

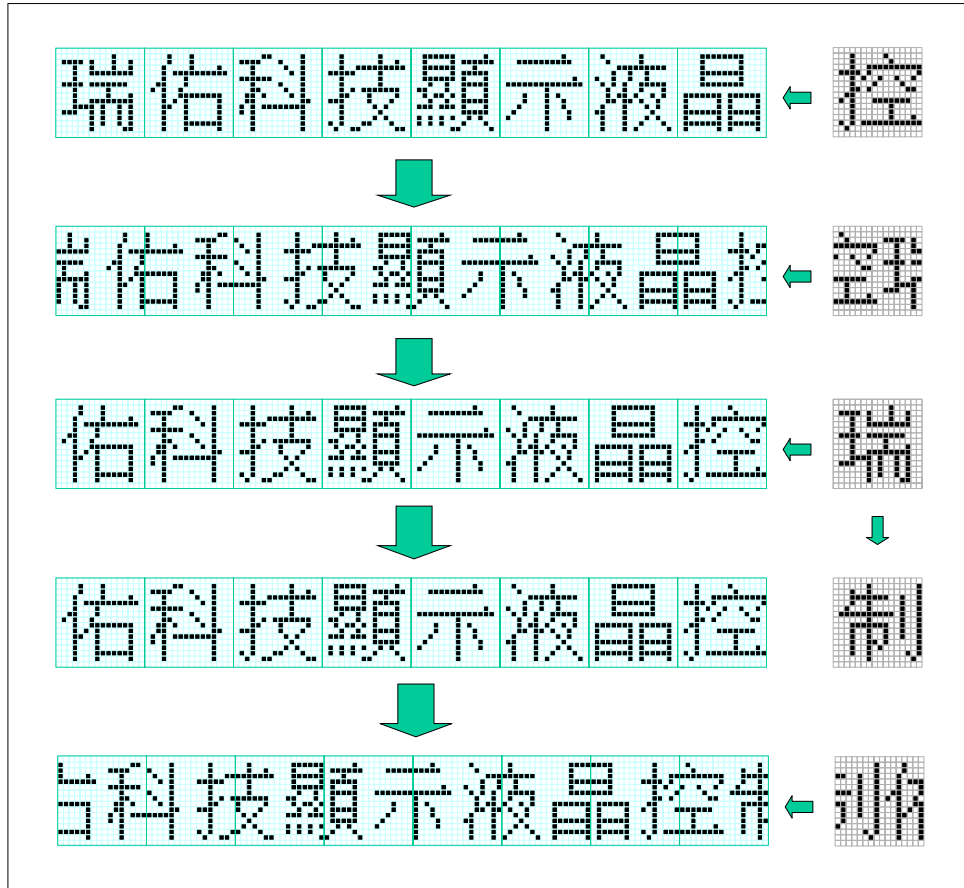


Figure 7-8: Horizontal Shift

7-6 Vertical Scroll

The RA8816 also provides the Vertical Scroll and Shift features that like horizontal function. User could assign the range of scrolling, scroll unit and speed. Refer to the following example as Figure 7-9. The vertical scroll unit is set to 2 pixels.

The RA8816 allows vertical scroll for up or down way. The user could use the scrolling buffer to show the Shift function. For example, store the data or text on the Vertical Scroll Buffer first, then fill the new data/text into the buffer that after the screen shift 16pixels. Please refer to application note for the related vertical scroll features.

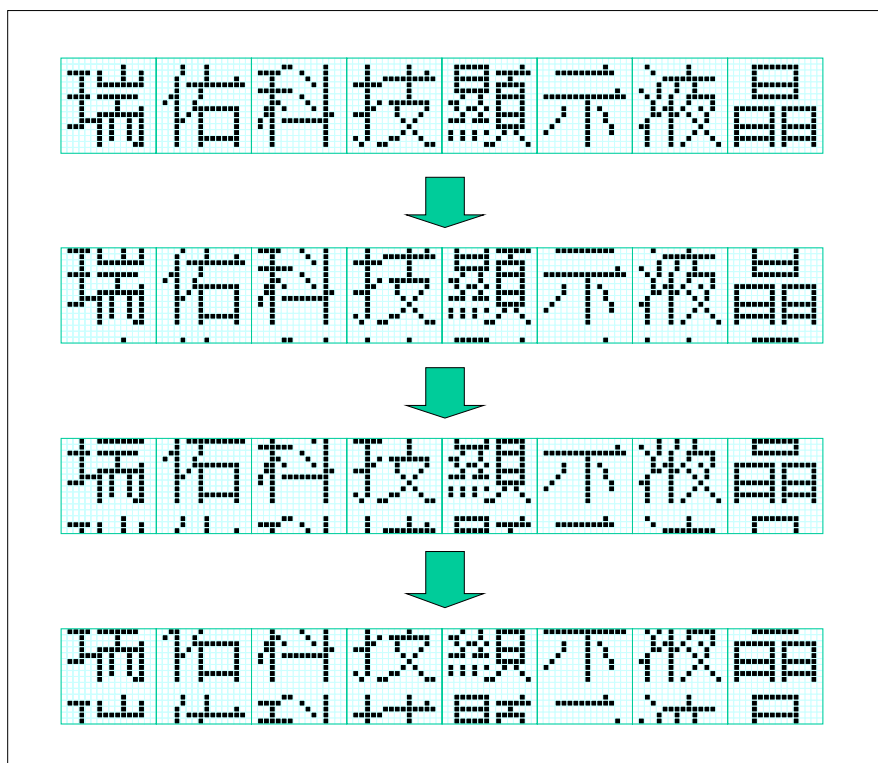


Figure 7-9: Vertical Scroll

8. Pin Diagram

8-1 COG Pad

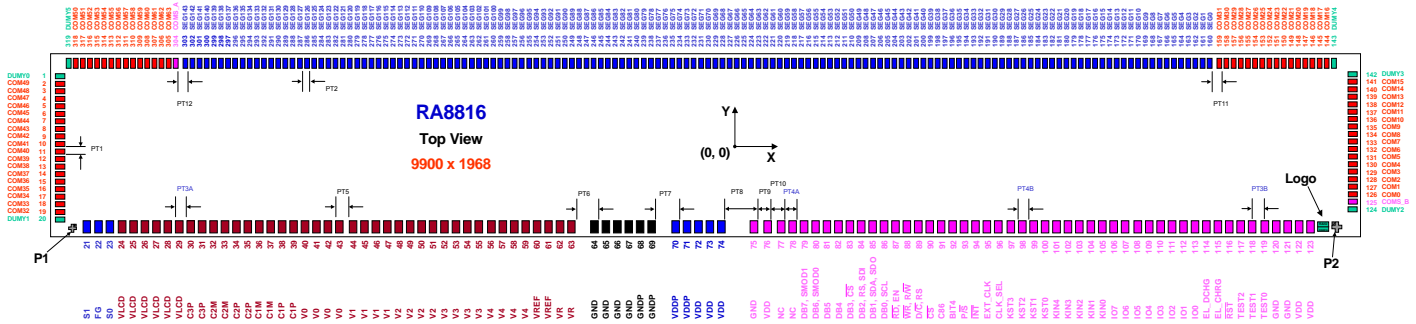


Figure 8-1 : Pin Diagram

Table 8-1: Bump Size and Pitch

| | | |
|----------------------|---|-------------------------------------|
| Chip Size: | 9900 μm x 1968 μm | |
| Bump Size: | PAD 1~20, PAD 124~142 (COM Pads) | 74 μm x 30 μm |
| | PAD 143~319 (COM/SEG Pads) | 30 μm x 74 μm |
| | PAD 24~123 (MCU/Power Pads) | 60 μm x 84 μm |
| | PAD 21~23 (S1, FG, S0) | 55 μm x 84 μm |
| Bump Pitch: | PT1: PAD 1~20, PAD 124~142 | 60 μm |
| | PT2: PAD 143~319 | 50 μm |
| | PT3A: PAD 21~74, PAD 119~123 | 80 μm |
| | PT3B: PAD 118~119 | 88.28 μm |
| | PT4A: PAD 77 to 78 | 88 μm |
| | PT4B: PAD 78 to 118 | 88.4~88.6 μm |
| | PT5: PAD 44 to 43 | 90 μm |
| | PT6: PAD 63 to 64 | 130 μm |
| | PT7: PAD 69 to 70 | 150 μm |
| | PT8: PAD 74 to 75 | 220 μm |
| | PT9: PAD 75 to 76 | 95.76 μm |
| | PT10: PAD 76 to 77 | 81.37 μm |
| PT11: PAD 159 to 160 | 90 μm | |
| PT12: PAD 303 to 304 | 90 μm | |
| Bump Height | 15 \pm 3 μm | |

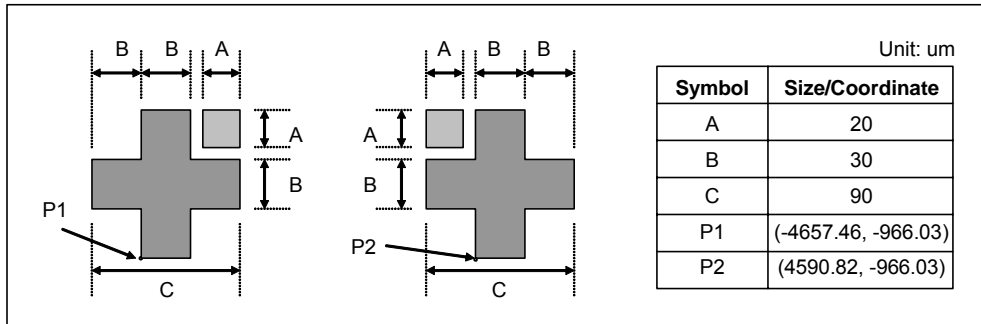


Figure 8-3 : Fixed Point Dimension

8-2 Pad X/Y Coordinate

| Pad No. | Pad Name | X | Y |
|---------|----------|----------|---------|
| 1 | DUMY0 | -4883.61 | 471.47 |
| 2 | COM49 | -4883.61 | 411.47 |
| 3 | COM48 | -4883.61 | 351.47 |
| 4 | COM47 | -4883.61 | 291.47 |
| 5 | COM46 | -4883.61 | 231.47 |
| 6 | COM45 | -4883.61 | 171.47 |
| 7 | COM44 | -4883.61 | 111.47 |
| 8 | COM43 | -4883.61 | 51.47 |
| 9 | COM42 | -4883.61 | -8.53 |
| 10 | COM41 | -4883.61 | -68.53 |
| 11 | COM40 | -4883.61 | -128.53 |
| 12 | COM39 | -4883.61 | -188.53 |
| 13 | COM38 | -4883.61 | -248.53 |
| 14 | COM37 | -4883.61 | -308.53 |
| 15 | COM36 | -4883.61 | -368.53 |
| 16 | COM35 | -4883.61 | -428.53 |
| 17 | COM34 | -4883.61 | -488.53 |
| 18 | COM33 | -4883.61 | -548.53 |
| 19 | COM32 | -4883.61 | -608.53 |
| 20 | DUMY1 | -4883.61 | -668.53 |
| 21 | S1 | -4421.31 | -917.53 |
| 22 | FG | -4341.31 | -917.53 |
| 23 | S0 | -4261.31 | -917.53 |
| 24 | VOUT | -4178.61 | -917.78 |
| 25 | VOUT | -4098.61 | -917.78 |
| 26 | VOUT | -4018.61 | -917.78 |
| 27 | VOUT | -3938.61 | -917.78 |
| 28 | VOUT | -3858.61 | -917.78 |
| 29 | VOUT | -3778.61 | -917.78 |
| 30 | C3P | -3698.61 | -917.78 |
| 31 | C3P | -3618.61 | -917.78 |
| 32 | C2N | -3538.61 | -917.78 |

| Pad No. | Pad Name | X | Y |
|---------|----------|----------|---------|
| 33 | C2N | -3458.61 | -917.78 |
| 34 | C2P | -3378.61 | -917.78 |
| 35 | C2P | -3298.61 | -917.78 |
| 36 | C1N | -3218.61 | -917.78 |
| 37 | C1N | -3138.61 | -917.78 |
| 38 | C1P | -3058.61 | -917.78 |
| 39 | C1P | -2978.61 | -917.78 |
| 40 | V0 | -2898.61 | -917.78 |
| 41 | V0 | -2818.61 | -917.78 |
| 42 | V0 | -2738.61 | -917.78 |
| 43 | V0 | -2658.61 | -917.78 |
| 44 | V1 | -2568.61 | -917.78 |
| 45 | V1 | -2488.61 | -917.78 |
| 46 | V1 | -2408.61 | -917.78 |
| 47 | V1 | -2328.61 | -917.78 |
| 48 | V2 | -2248.61 | -917.78 |
| 49 | V2 | -2168.61 | -917.78 |
| 50 | V2 | -2088.61 | -917.78 |
| 51 | V2 | -2008.61 | -917.78 |
| 52 | V3 | -1928.61 | -917.78 |
| 53 | V3 | -1848.61 | -917.78 |
| 54 | V3 | -1768.61 | -917.78 |
| 55 | V3 | -1688.61 | -917.78 |
| 56 | V4 | -1608.61 | -917.78 |
| 57 | V4 | -1528.61 | -917.78 |
| 58 | V4 | -1448.61 | -917.78 |
| 59 | V4 | -1368.61 | -917.78 |
| 60 | VREF | -1288.61 | -917.78 |
| 61 | VREF | -1208.61 | -917.78 |
| 62 | VR | -1128.61 | -917.78 |
| 63 | VR | -1048.61 | -917.78 |
| 64 | GND | -918.61 | -917.78 |

| Pad No. | Pad Name | X | Y |
|---------|-------------------------|---------|---------|
| 65 | GND | -838.61 | -917.78 |
| 66 | GND | -758.61 | -917.78 |
| 67 | GND | -678.61 | -917.78 |
| 68 | GNDP | -598.61 | -917.78 |
| 69 | GNDP | -518.61 | -917.78 |
| 70 | VDDP | -368.61 | -917.78 |
| 71 | VDDP | -288.61 | -917.78 |
| 72 | VDD | -208.61 | -917.78 |
| 73 | VDD | -128.61 | -917.78 |
| 74 | VDD | -48.61 | -917.78 |
| 75 | GND | 171.39 | -917.78 |
| 76 | VDD | 267.15 | -917.78 |
| 77 | NC | 348.52 | -917.78 |
| 78 | NC | 436.52 | -917.78 |
| 79 | DB7 | 525.04 | -917.78 |
| 80 | DB6 | 613.55 | -917.78 |
| 81 | DB5 | 702.06 | -917.78 |
| 82 | DB4 | 790.58 | -917.78 |
| 83 | DB3 | 879.09 | -917.78 |
| 84 | DB2 | 967.6 | -917.78 |
| 85 | DB1 | 1056.11 | -917.78 |
| 86 | DB0 | 1144.63 | -917.78 |
| 87 | $\overline{\text{RD}}$ | 1233.21 | -917.78 |
| 88 | $\overline{\text{WR}}$ | 1321.72 | -917.78 |
| 89 | $\overline{\text{D/C}}$ | 1410.24 | -917.78 |
| 90 | $\overline{\text{CS}}$ | 1498.75 | -917.78 |
| 91 | C86 | 1587.26 | -917.78 |
| 92 | BIT4 | 1675.78 | -917.78 |
| 93 | $\overline{\text{P/S}}$ | 1764.29 | -917.78 |
| 94 | $\overline{\text{INT}}$ | 1852.73 | -917.78 |
| 95 | EXT_CLK | 1941.31 | -917.78 |
| 96 | CLK_SEL | 2029.83 | -917.78 |
| 97 | KST3 | 2118.27 | -917.78 |
| 98 | KST2 | 2206.78 | -917.78 |

| Pad No. | Pad Name | X | Y |
|---------|-------------------------|---------|---------|
| 99 | KST1 | 2295.3 | -917.78 |
| 100 | KS0 | 2383.81 | -917.78 |
| 101 | KIN4 | 2472.39 | -917.78 |
| 102 | KIN3 | 2560.91 | -917.78 |
| 103 | KIN2 | 2649.42 | -917.78 |
| 104 | KIN1 | 2737.93 | -917.78 |
| 105 | KIN0 | 2826.44 | -917.78 |
| 106 | IO7 | 2914.89 | -917.78 |
| 107 | IO6 | 3003.4 | -917.78 |
| 108 | IO5 | 3091.91 | -917.78 |
| 109 | IO4 | 3180.43 | -917.78 |
| 110 | IO3 | 3268.94 | -917.78 |
| 111 | IO2 | 3357.45 | -917.78 |
| 112 | IO1 | 3445.97 | -917.78 |
| 113 | IO0 | 3534.48 | -917.78 |
| 114 | EL_DCHG | 3622.99 | -917.78 |
| 115 | EL_CHRG | 3711.5 | -917.78 |
| 116 | $\overline{\text{RST}}$ | 3800.09 | -917.78 |
| 117 | TEST2 | 3888.6 | -917.78 |
| 118 | TEST1 | 3977.11 | -917.78 |
| 119 | TEST0 | 4065.39 | -917.78 |
| 120 | GND | 4145.39 | -917.78 |
| 121 | GND | 4225.39 | -917.78 |
| 122 | VDD | 4305.39 | -917.78 |
| 123 | VDD | 4385.39 | -917.78 |
| 124 | DUMY2 | 4883.61 | -657.03 |
| 125 | COMS_B | 4883.61 | -597.03 |
| 126 | COM0 | 4883.61 | -537.03 |
| 127 | COM1 | 4883.61 | -477.03 |
| 128 | COM2 | 4883.61 | -417.03 |
| 129 | COM3 | 4883.61 | -357.03 |
| 130 | COM4 | 4883.61 | -297.03 |
| 131 | COM5 | 4883.61 | -237.03 |
| 132 | COM6 | 4883.61 | -177.03 |

| Pad No. | Pad Name | X | Y |
|---------|----------|---------|---------|
| 133 | COM7 | 4883.61 | -117.03 |
| 134 | COM8 | 4883.61 | -57.03 |
| 135 | COM9 | 4883.61 | 2.97 |
| 136 | COM10 | 4883.61 | 62.97 |
| 137 | COM11 | 4883.61 | 122.97 |
| 138 | COM12 | 4883.61 | 182.97 |
| 139 | COM13 | 4883.61 | 242.97 |
| 140 | COM14 | 4883.61 | 302.97 |
| 141 | COM15 | 4883.61 | 362.97 |
| 142 | DUMY3 | 4883.61 | 422.97 |
| 143 | DUMY4 | 4445.15 | 917.78 |
| 144 | COM16 | 4385.64 | 917.78 |
| 145 | COM17 | 4335.64 | 917.78 |
| 146 | COM18 | 4285.64 | 917.78 |
| 147 | COM19 | 4235.64 | 917.78 |
| 148 | COM20 | 4185.64 | 917.78 |
| 149 | COM21 | 4135.64 | 917.78 |
| 150 | COM22 | 4085.64 | 917.78 |
| 151 | COM23 | 4035.64 | 917.78 |
| 152 | COM24 | 3985.64 | 917.78 |
| 153 | COM25 | 3935.64 | 917.78 |
| 154 | COM26 | 3885.64 | 917.78 |
| 155 | COM27 | 3835.64 | 917.78 |
| 156 | COM28 | 3785.64 | 917.78 |
| 157 | COM29 | 3735.64 | 917.78 |
| 158 | COM30 | 3685.64 | 917.78 |
| 159 | COM31 | 3635.64 | 917.78 |
| 160 | SEG0 | 3545.64 | 917.78 |
| 161 | SEG1 | 3495.64 | 917.78 |
| 162 | SEG2 | 3445.64 | 917.78 |
| 163 | SEG3 | 3395.64 | 917.78 |
| 164 | SEG4 | 3345.64 | 917.78 |
| 165 | SEG5 | 3295.64 | 917.78 |
| 166 | SEG6 | 3245.64 | 917.78 |

| Pad No. | Pad Name | X | Y |
|---------|----------|---------|--------|
| 167 | SEG7 | 3195.64 | 917.78 |
| 168 | SEG8 | 3145.64 | 917.78 |
| 169 | SEG9 | 3095.64 | 917.78 |
| 170 | SEG10 | 3045.64 | 917.78 |
| 171 | SEG11 | 2995.64 | 917.78 |
| 172 | SEG12 | 2945.64 | 917.78 |
| 173 | SEG13 | 2895.64 | 917.78 |
| 174 | SEG14 | 2845.64 | 917.78 |
| 175 | SEG15 | 2795.64 | 917.78 |
| 176 | SEG16 | 2745.64 | 917.78 |
| 177 | SEG17 | 2695.64 | 917.78 |
| 178 | SEG18 | 2645.64 | 917.78 |
| 179 | SEG19 | 2595.64 | 917.78 |
| 180 | SEG20 | 2545.64 | 917.78 |
| 181 | SEG21 | 2495.64 | 917.78 |
| 182 | SEG22 | 2445.64 | 917.78 |
| 183 | SEG23 | 2395.64 | 917.78 |
| 184 | SEG24 | 2345.64 | 917.78 |
| 185 | SEG25 | 2295.64 | 917.78 |
| 186 | SEG26 | 2245.64 | 917.78 |
| 187 | SEG27 | 2195.64 | 917.78 |
| 188 | SEG28 | 2145.64 | 917.78 |
| 189 | SEG29 | 2095.64 | 917.78 |
| 190 | SEG30 | 2045.64 | 917.78 |
| 191 | SEG31 | 1995.64 | 917.78 |
| 192 | SEG32 | 1945.64 | 917.78 |
| 193 | SEG33 | 1895.64 | 917.78 |
| 194 | SEG34 | 1845.64 | 917.78 |
| 195 | SEG35 | 1795.64 | 917.78 |
| 196 | SEG36 | 1745.64 | 917.78 |
| 197 | SEG37 | 1695.64 | 917.78 |
| 198 | SEG38 | 1645.64 | 917.78 |
| 199 | SEG39 | 1595.64 | 917.78 |
| 200 | SEG40 | 1545.64 | 917.78 |

| Pad No. | Pad Name | X | Y |
|---------|----------|---------|--------|
| 201 | SEG41 | 1495.64 | 917.78 |
| 202 | SEG42 | 1445.64 | 917.78 |
| 203 | SEG43 | 1395.64 | 917.78 |
| 204 | SEG44 | 1345.64 | 917.78 |
| 205 | SEG45 | 1295.64 | 917.78 |
| 206 | SEG46 | 1245.64 | 917.78 |
| 207 | SEG47 | 1195.64 | 917.78 |
| 208 | SEG48 | 1145.64 | 917.78 |
| 209 | SEG49 | 1095.64 | 917.78 |
| 210 | SEG50 | 1045.64 | 917.78 |
| 211 | SEG51 | 995.64 | 917.78 |
| 212 | SEG52 | 945.64 | 917.78 |
| 213 | SEG53 | 895.64 | 917.78 |
| 214 | SEG54 | 845.64 | 917.78 |
| 215 | SEG55 | 795.64 | 917.78 |
| 216 | SEG56 | 745.64 | 917.78 |
| 217 | SEG57 | 695.64 | 917.78 |
| 218 | SEG58 | 645.64 | 917.78 |
| 219 | SEG59 | 595.64 | 917.78 |
| 220 | SEG60 | 545.64 | 917.78 |
| 221 | SEG61 | 495.64 | 917.78 |
| 222 | SEG62 | 445.64 | 917.78 |
| 223 | SEG63 | 395.64 | 917.78 |
| 224 | SEG64 | 345.64 | 917.78 |
| 225 | SEG65 | 295.64 | 917.78 |
| 226 | SEG66 | 245.64 | 917.78 |
| 227 | SEG67 | 195.64 | 917.78 |
| 228 | SEG68 | 145.64 | 917.78 |
| 229 | SEG69 | 95.64 | 917.78 |
| 230 | SEG70 | 45.64 | 917.78 |
| 231 | SEG71 | -4.36 | 917.78 |
| 232 | SEG72 | -54.36 | 917.78 |
| 233 | SEG73 | -104.36 | 917.78 |
| 234 | SEG74 | -154.36 | 917.78 |

| Pad No. | Pad Name | X | Y |
|---------|----------|----------|--------|
| 235 | SEG75 | -204.36 | 917.78 |
| 236 | SEG76 | -254.36 | 917.78 |
| 237 | SEG77 | -304.36 | 917.78 |
| 238 | SEG78 | -354.36 | 917.78 |
| 239 | SEG79 | -404.36 | 917.78 |
| 240 | SEG80 | -454.36 | 917.78 |
| 241 | SEG81 | -504.36 | 917.78 |
| 242 | SEG82 | -554.36 | 917.78 |
| 243 | SEG83 | -604.36 | 917.78 |
| 244 | SEG84 | -654.36 | 917.78 |
| 245 | SEG85 | -704.36 | 917.78 |
| 246 | SEG86 | -754.36 | 917.78 |
| 247 | SEG87 | -804.36 | 917.78 |
| 248 | SEG88 | -854.36 | 917.78 |
| 249 | SEG89 | -904.36 | 917.78 |
| 250 | SEG90 | -954.36 | 917.78 |
| 251 | SEG91 | -1004.36 | 917.78 |
| 252 | SEG92 | -1054.36 | 917.78 |
| 253 | SEG93 | -1104.36 | 917.78 |
| 254 | SEG94 | -1154.36 | 917.78 |
| 255 | SEG95 | -1204.36 | 917.78 |
| 256 | SEG96 | -1254.36 | 917.78 |
| 257 | SEG97 | -1304.36 | 917.78 |
| 258 | SEG98 | -1354.36 | 917.78 |
| 259 | SEG99 | -1404.36 | 917.78 |
| 260 | SEG100 | -1454.36 | 917.78 |
| 261 | SEG101 | -1504.36 | 917.78 |
| 262 | SEG102 | -1554.36 | 917.78 |
| 263 | SEG103 | -1604.36 | 917.78 |
| 264 | SEG104 | -1654.36 | 917.78 |
| 265 | SEG105 | -1704.36 | 917.78 |
| 266 | SEG106 | -1754.36 | 917.78 |
| 267 | SEG107 | -1804.36 | 917.78 |
| 268 | SEG108 | -1854.36 | 917.78 |

| Pad No. | Pad Name | X | Y |
|---------|----------|----------|--------|
| 269 | SEG109 | -1904.36 | 917.78 |
| 270 | SEG110 | -1954.36 | 917.78 |
| 271 | SEG111 | -2004.36 | 917.78 |
| 272 | SEG112 | -2054.36 | 917.78 |
| 273 | SEG113 | -2104.36 | 917.78 |
| 274 | SEG114 | -2154.36 | 917.78 |
| 275 | SEG115 | -2204.36 | 917.78 |
| 276 | SEG116 | -2254.36 | 917.78 |
| 277 | SEG117 | -2304.36 | 917.78 |
| 278 | SEG118 | -2354.36 | 917.78 |
| 279 | SEG119 | -2404.36 | 917.78 |
| 280 | SEG120 | -2454.36 | 917.78 |
| 281 | SEG121 | -2504.36 | 917.78 |
| 282 | SEG122 | -2554.36 | 917.78 |
| 283 | SEG123 | -2604.36 | 917.78 |
| 284 | SEG124 | -2654.36 | 917.78 |
| 285 | SEG125 | -2704.36 | 917.78 |
| 286 | SEG126 | -2754.36 | 917.78 |
| 287 | SEG127 | -2804.36 | 917.78 |
| 288 | SEG128 | -2854.36 | 917.78 |
| 299 | SEG129 | -2904.36 | 917.78 |
| 290 | SEG130 | -2954.36 | 917.78 |
| 291 | SEG131 | -3004.36 | 917.78 |
| 292 | SEG132 | -3054.36 | 917.78 |
| 293 | SEG133 | -3104.36 | 917.78 |
| 294 | SEG134 | -3154.36 | 917.78 |
| 295 | SEG135 | -3204.36 | 917.78 |
| 296 | SEG136 | -3254.36 | 917.78 |
| 297 | SEG137 | -3304.36 | 917.78 |
| 298 | SEG138 | -3354.36 | 917.78 |
| 299 | SEG139 | -3404.36 | 917.78 |
| 300 | SEG140 | -3454.36 | 917.78 |
| 301 | SEG141 | -3504.36 | 917.78 |
| 302 | SEG142 | -3554.36 | 917.78 |

| Pad No. | Pad Name | X | Y |
|---------|----------|----------|--------|
| 303 | SEG143 | -3604.36 | 917.78 |
| 304 | COMS_A | -3694.36 | 917.78 |
| 305 | COM63 | -3744.36 | 917.78 |
| 306 | COM62 | -3794.36 | 917.78 |
| 307 | COM61 | -3844.36 | 917.78 |
| 308 | COM60 | -3894.36 | 917.78 |
| 309 | COM59 | -3944.36 | 917.78 |
| 310 | COM58 | -3994.36 | 917.78 |
| 311 | COM57 | -4044.36 | 917.78 |
| 312 | COM56 | -4094.36 | 917.78 |
| 313 | COM55 | -4144.36 | 917.78 |
| 314 | COM54 | -4194.36 | 917.78 |
| 315 | COM53 | -4244.36 | 917.78 |
| 316 | COM52 | -4294.36 | 917.78 |
| 317 | COM51 | -4344.36 | 917.78 |
| 318 | COM50 | -4394.36 | 917.78 |
| 319 | DUMY5 | -4445.15 | 917.78 |

9. Electrical Characteristic

9-1 Absolute Maximum Ratings

Table 9-1

| Parameter | Symbol | Rating | Unit |
|-----------------------------|-----------|----------------------|------|
| Supply Voltage Range | V_{DD} | -0.3 to 6.5 | V |
| Input Voltage Range | V_{IN} | -0.3 to $V_{DD}+0.3$ | V |
| External VLCD Voltage Range | V_{LCD} | -0.3 to 14 | V |
| Operation Temperature Range | T_{OPR} | -40 to 85 | °C |
| Storage Temperature Range | T_{ST} | -55 to 125 | °C |

9-2 DC Characteristic

Table 9-2

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---------------|---------------------|------|---------------------|------|--|
| Operating Voltage | V_{DD} | 2.9 | 3.3 | 3.8 | V | COG Module |
| VLCD Voltage | V_{LCD} | 6 | -- | 12 | V | |
| Input High Voltage | V_{IH} | $0.8 \times V_{DD}$ | -- | V_{DD} | V | |
| Input Low Voltage | V_{IL} | Gnd | -- | $0.2 \times V_{DD}$ | V | |
| Output High Voltage | V_{OH} | $0.8 \times V_{DD}$ | -- | V_{DD} | V | |
| Output Low Voltage | V_{OL} | Gnd | -- | $0.2 \times V_{DD}$ | V | |
| Input Leakage Current | I_{IL} | -1 | -- | +1 | μA | $V_{IN} = V_{DD}$ to V_{SS} |
| Output Leakage Current | I_{OL} | -3 | -- | +2 | μA | $V_{IN} = V_{DD}$ to V_{SS} |
| Oscillator Frequency | F_{CL} | 85 | 95 | 105 | Khz | |
| Standby Mode Current (Normal Mode Current) | I_{SB} | -- | 70 | -- | μA | No MPU I/F Access $V_{DD}=3.3V$, $F_{CL} = 100KHz$ Segment=144, Common=64 FRM = 60Hz $T_A=25^\circ C$ |
| Display Off Current | $I_{DISPLAY}$ | -- | 25 | -- | μA | The same as above |
| Sleep Mode Current | I_{SLEEP} | -- | 0.2 | 0.5 | μA | The same as above |

$V_{DD} = 3.0$ to $3.6V$, Gnd = $0V$, $T_a = -20$ to $80^\circ C$

9-3 Timing Characteristic

9-3-1 Parallel Interface

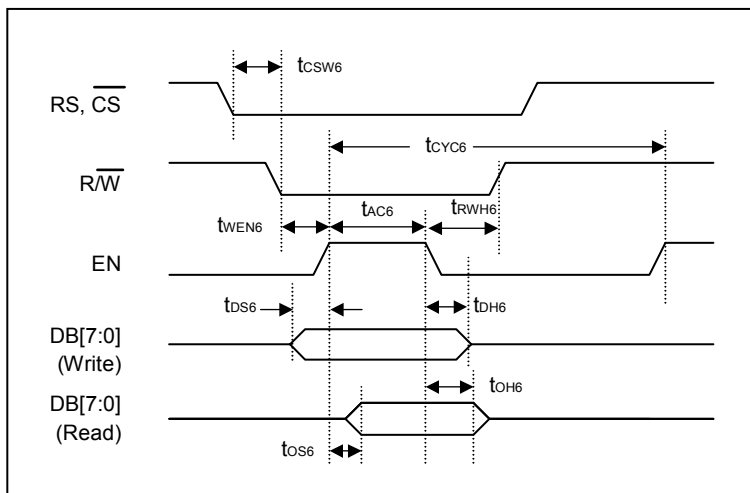


Figure 9-1 : 6800 MPU Timing

6800 MPU Interface

Table 9-3

| Item | Signal | Symbol | Condition | Rating | | Unit |
|-----------------------|---------------------|------------|---------------|--------|------|------|
| | | | | Min. | Max. | |
| Address Setup Time | RS, \overline{CS} | t_{csw6} | | 0 | -- | ns |
| Read/Write Setup Time | R/ \overline{W} | t_{wen6} | | 10 | -- | |
| Read/Write Hold Time | | t_{rwh6} | | 10 | -- | |
| Enable Access Time | EN | t_{ac6} | | 90 | -- | |
| Access Cycle Time | | t_{cyc6} | Command Cycle | 200 | -- | |
| | | | Data Cycle | 400 | -- | |
| Write Data Setup Time | DB[7..0] | t_{ds6} | | 10 | -- | |
| Write Data Hold Time | | t_{dh6} | | 10 | -- | |
| Read Data Access Time | | t_{os6} | | 30 | 50 | |
| Read Data Hold Time | | t_{oh6} | | 10 | -- | |

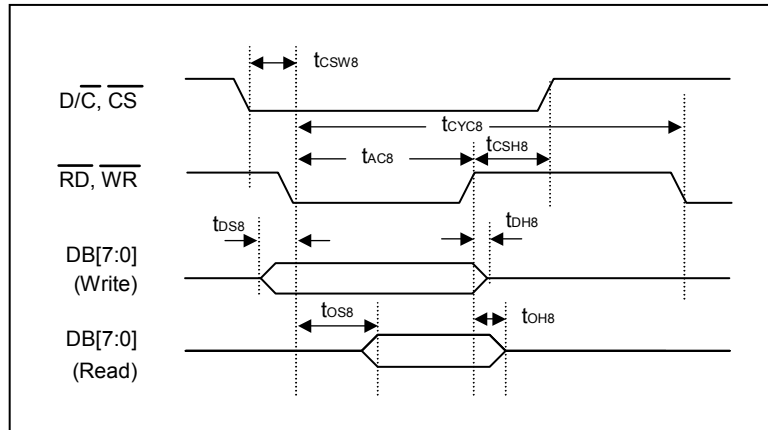


Figure 9-2 : 8080 MPU Timing

8080 MPU Interface

Table 9-4

| Item | Signal | Symbol | Condition | Rating | | Unit |
|------------------------|--------------------------------|------------|---------------|--------|------|------|
| | | | | Min. | Max. | |
| Address Setup Time | $\overline{RS}, \overline{CS}$ | t_{CSW8} | | 10 | -- | ns |
| Address Hold Time | | t_{CSH8} | | 10 | -- | |
| Read/Write Access Time | $\overline{RD}, \overline{WR}$ | t_{AC8} | | 90 | -- | |
| Access Cycle Time | | t_{CYC8} | Command Cycle | 200 | -- | |
| | Data Cycle | | 400 | -- | | |
| Write Data Setup Time | $DB[7..0]$ | t_{DS8} | | 10 | -- | |
| Write Data Hold Time | | t_{DH8} | | 10 | -- | |
| Read Data Setup Time | | t_{OS8} | | 30 | 50 | |
| Read Data Hold Time | | t_{OH8} | | 10 | -- | |

9-3-2 Serial Interface

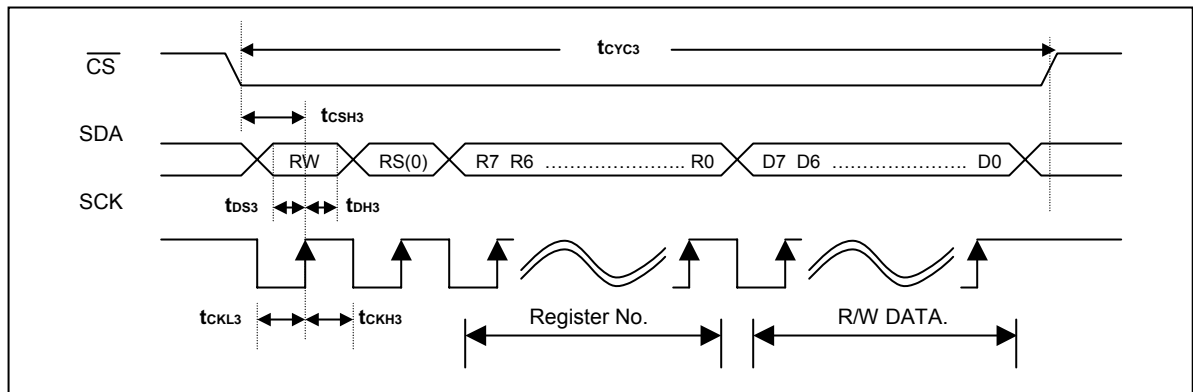


Figure 9-3 : 3-Wire Timing

3-Wire Serial Interface

Table 9-5

| Item | Signal | Symbol | Condition | Rating | | Unit |
|-----------------------------------|------------------------|-------------------|-----------|--------|------|---------------|
| | | | | Min. | Max. | |
| Access Time | $\overline{\text{CS}}$ | t_{CYC3} | | 3.6 | -- | μs |
| $\overline{\text{CS}}$ Setup Time | | t_{CSH3} | | 20 | -- | ns |
| Clock Low Pulse Width | SCK | t_{CKL3} | | 100 | -- | |
| Clock High Pulse Width | | t_{CKH3} | | 100 | -- | |
| Data Setup Time | SDA | t_{DS3} | | 20 | -- | |
| Data Hold Time | | t_{DH3} | | 10 | -- | |

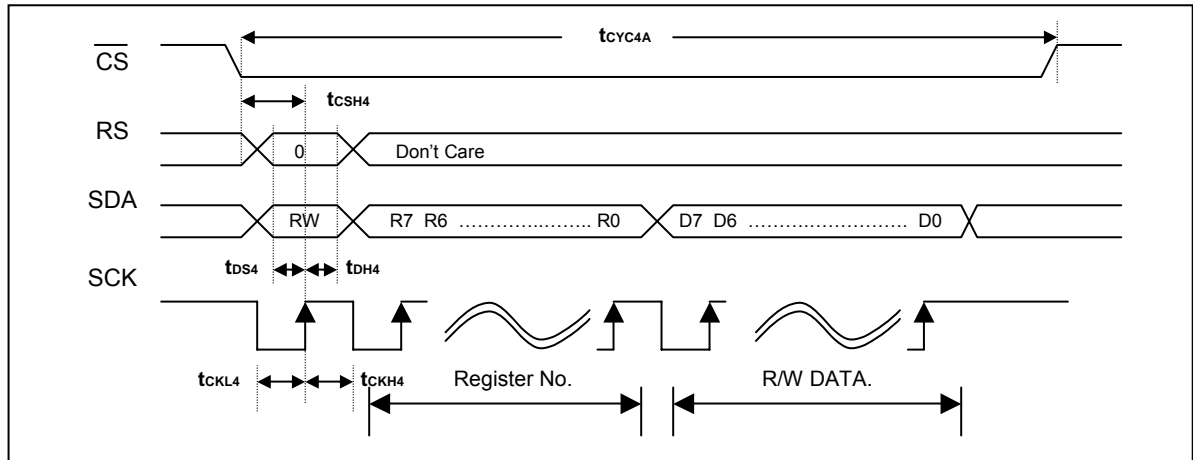


Figure 9-4 : 4-Wire(A-Type) Timing

4-Wire(A-Type) Serial Interface

Table 9-6

| Item | Signal | Symbol | Condition | Rating | | Unit |
|-----------------------------------|------------------------|--------------------|-----------|--------|------|---------------|
| | | | | Min. | Max. | |
| Access Time | $\overline{\text{CS}}$ | t_{CYC4A} | | 3.4 | -- | μs |
| $\overline{\text{CS}}$ Setup Time | | t_{CSH4} | | 20 | -- | ns |
| Clock Low Pulse Width | SCK | t_{CKL4} | | 100 | -- | |
| Clock High Pulse Width | | t_{CKH4} | | 100 | -- | |
| Data Setup Time | SDA, RS | t_{DS4} | | 20 | -- | |
| Data Hold Time | | t_{DH4} | | 10 | -- | |

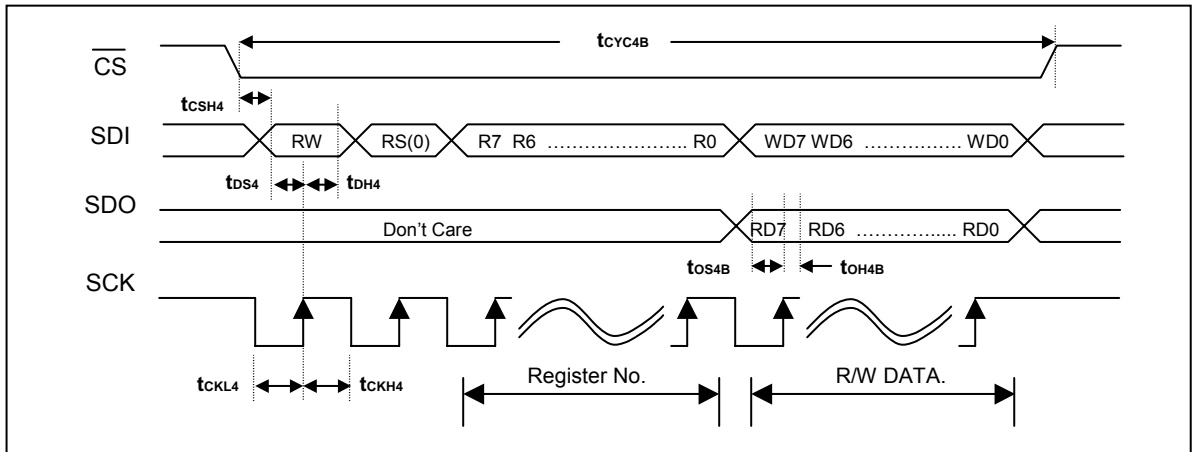


Figure 9-5A : 4-Wire(B Type) Timing

4-Wire(B-Type) Serial Interface

Table 9-7A

| Item | Signal | Symbol | Condition | Rating | | Unit |
|----------------------------|-----------------|-------------|-----------|--------|------|---------|
| | | | | Min. | Max. | |
| Access Time | \overline{CS} | t_{Cyc4A} | | 3.6 | -- | μs |
| \overline{CS} Setup Time | | t_{CSH4} | | 20 | -- | ns |
| Clock Low Pulse Width | SCK | t_{CKL4} | | 100 | -- | |
| Clock High Pulse Width | | t_{CKH4} | | 100 | -- | |
| Data Write Setup Time | SDI | t_{DS4} | | 20 | -- | |
| Data Write Hold Time | | t_{DH4} | | 10 | -- | |
| Data Read Setup Time | SDO | t_{OS4B} | | 20 | -- | |
| Data Read Hold Time | | t_{OH4B} | | 10 | -- | |

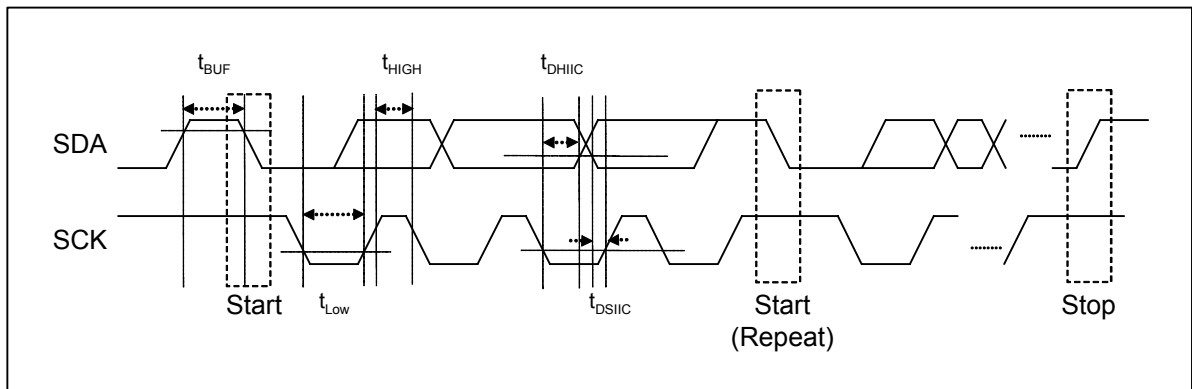


Figure 9-5B: IIC Timing

IIC Serial Interface

Table 9-7B

| Item | Signal | Symbol | Rating | | Unit |
|--------------------------------------|---------|-------------|--------|-----|------|
| | | | Min | Max | |
| SCK Clock Frequency | SCK | f_{SCL} | -- | 500 | KHz |
| Bus Free Time Between STOP and START | SCK/SDA | t_{BUF} | 1 | -- | us |
| LOW Period of SCK Clock | SCK | t_{Low} | 200 | -- | ns |
| HIGH Period of SCK Clock | SCK | t_{High} | 200 | -- | ns |
| Data Setup Time | SCK/SDA | t_{DSIIC} | 100 | | ns |
| Data Hold time | SCK/SDA | t_{DHIIC} | 100 | | ns |

9-3-3 Reset Interface

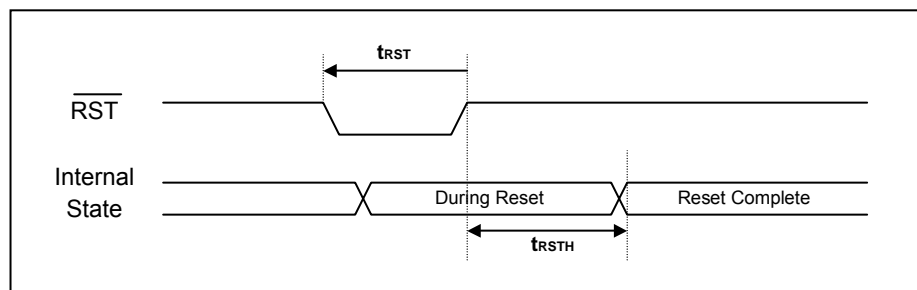


Figure 9-6: Reset Timing

Table 9-8

| Item | Signal | Symbol | Condition | Rating | | Unit |
|--------------------------|------------------|------------|--|--------|------|------|
| | | | | Min. | Max. | |
| Reset Pulse Width | \overline{RST} | t_{RST} | | 30 | -- | ms |
| Reset Complete Hold Time | \overline{RST} | t_{RSTH} | $F_{CL} = 100\text{KHz}$ (Internal RC Oscillator) | 150 | -- | ms |

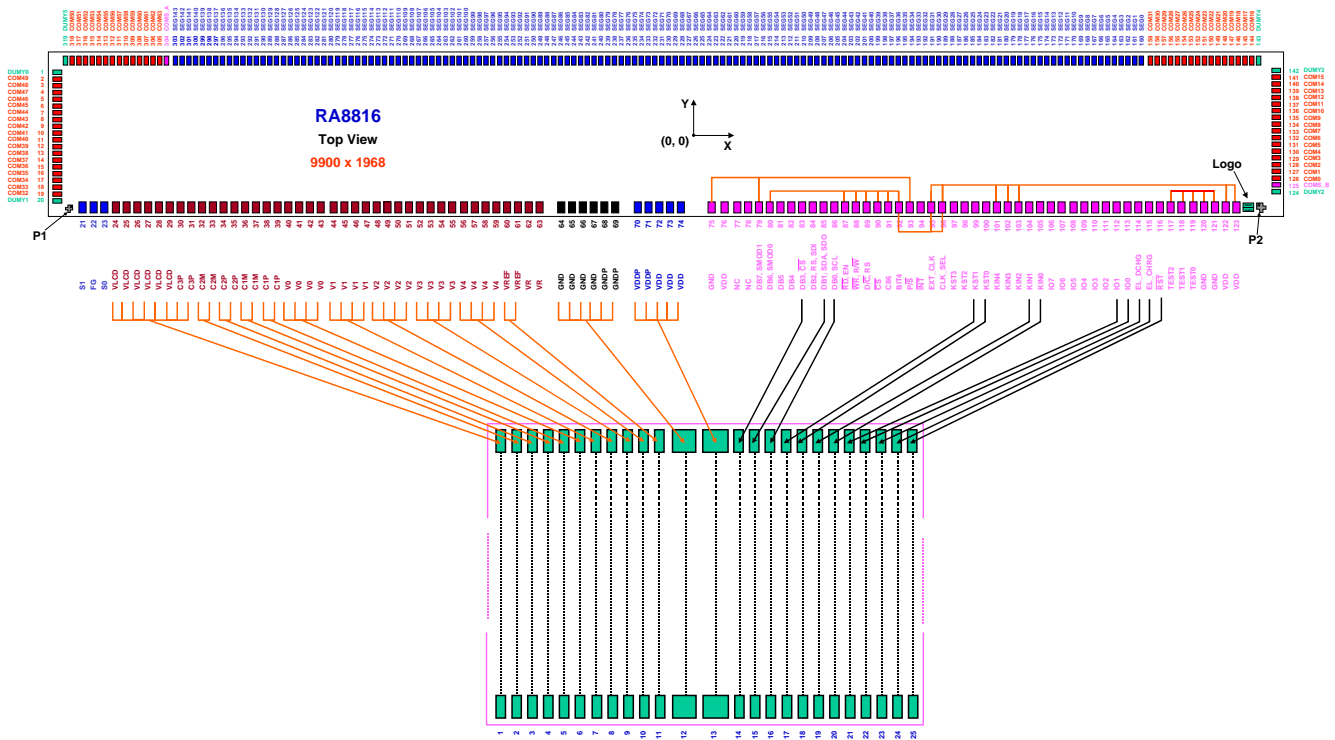


Figure A-4 : Example of COG Module

The Figure A-5 is an example for 144x65 LCD panel.

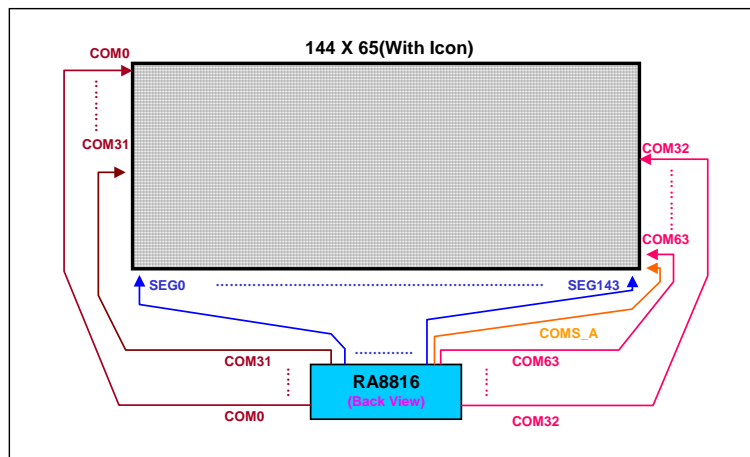


Figure A-5: The Connection of RA8816 with LCD Panel(144x65)

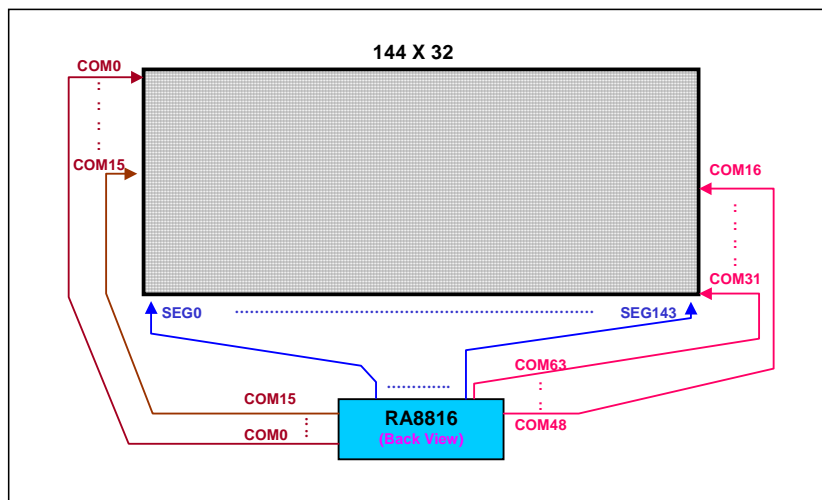


Figure A-6: The Connection of RA8816 with LCD Panel(144x32)

The Figure A-6 is an example of connection that use 144x32 panel. In this case, it supports two row for full size(16x16) or four rows for half-size(8x8) fonts. Please refer to Table5-3 for the Common signals connection

A-2 ITO

Table A-1: ITO Resistance of COG

| PAD Name | ITO(Ohm) | PAD Name | ITO(Ohm) | PAD Name | ITO(Ohm) |
|------------|----------|----------|----------|------------|----------|
| VDD , VDDP | 150 | C1M | 200 | BIT4 | 600 |
| GND , GNDP | 150 | C2P | 200 | P/S | 600 |
| VREF | 200 | C2M | 200 | CLK_SEL | 600 |
| VLCD | 200 | C3P | 200 | EXT_CLK | 600 |
| VR | 200 | DB[7..0] | 600 | KST[3..0] | 600 |
| V4 | 200 | RD , EN | 600 | KIN[4..0] | 600 |
| V3 | 200 | WR , R/W | 600 | IO[7..0] | 600 |
| V2 | 200 | D/C , RS | 600 | EL_CHRG | 600 |
| V1 | 200 | CS | 600 | EL_DCHG | 600 |
| V0 | 200 | INT | 600 | RST | 600 |
| C1P | 200 | C86 | 600 | TEST[2..0] | 600 |

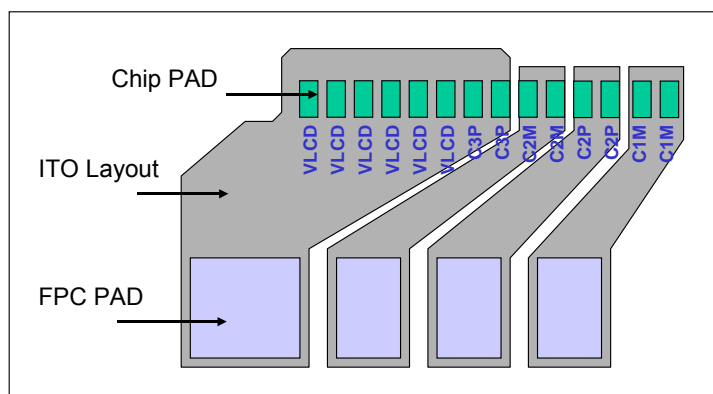


Figure A-7 : ITO Layout Example - VLCD

The RA8816 power signals (such as VDD, GND, VLCD, V[4..0], C1P, C1M, C2P, C2M) have to keep the smaller ITO resistance (less than 15 ohm is better) for panel layout. So the wires of layout need to keep as thick as possible to reduce the ITO resistance. The Figure A-7 is an example for VLCD layout of panel. Because the RA8816 provide six pads for VLCD, therefore the layout engineer has to connect all of these pads to FPC. In this case, the VLCD is three times of VDD, so the C3P have to connect to VLCD and do not forget keep the wire thicker.

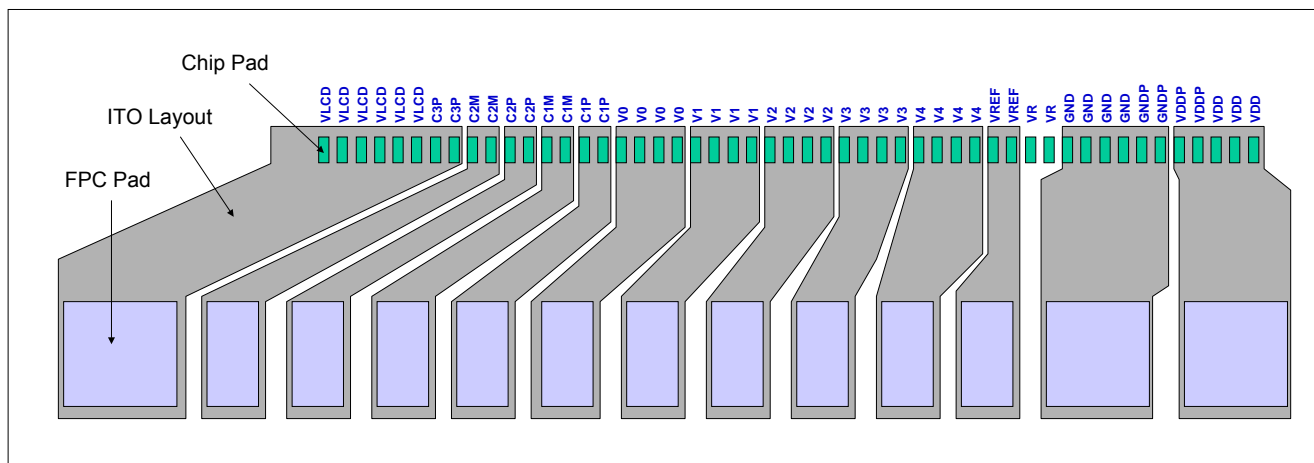


Figure A-8 : ITO Layout Example

The Figure A-8 is a layout example of RA8816 to FPC on COG module. The VDD and GND of RA8816 should be as close as possible to FPC. The RA8816 provides six GND pads, users have to connect these six pads to FPC with a thick wire. For the design of FPC, the related power signals (VDD, GND, VLCD) of layout need to keep as thick as possible to reduce the wire resistance. And the VDD, GND pad of FPC keep double width than other signals. For example, if panel resolution is 128x64 then use 4X VDD for booster and LCD voltage less than 9V is better.