TDA18271HD

Silicon Tuner IC

Rev. 03 — 11 September 2008 Product data sheet

1. General description

The TDA18271HD is a Silicon Tuner IC designed mainly for terrestrial analog and digital TV reception. The TDA18271HD integrates the overall tuning function, including selectivity.

The TDA18271HD is compatible with all analog and digital TV standards and delivers a low IF signal to a demodulator (for analog TV) and/or channel decoder (for digital TV).

This specification is based on software version 3.4.

2. Features

- Fully integrated RF tracking filters for unwanted signal suppression
- Fully integrated IF selectivity (no need for external SAW filters)
- Worldwide multistandard terrestrial (all analog and digital worldwide terrestrial standards supported)
- Integrated loop-through and slave tuner output for straightforward multi-silicon tuner application
- Fully integrated oscillators with no external components
- Alignment free
- Integrated wide-band gain control
- Single 3.3 V power supply
- Low power consumption
- Crystal oscillator output buffer (16 MHz) for single crystal applications
- I^2C-bus interface compatible with 3.3 V and 5 V microcontrollers
- Three Standby modes
- RoHS packaging

3. Applications

3.1 Target applications

- Hybrid (analog and digital TV) for PCTV, DVD-R and TV applications
- Application optimization is described in application notes *AN602*, *AN604* and *AN605*

3.2 Key benefits

- The TDA18271HD is a Silicon Tuner targeting digital and analog TV applications. The aim is to match the performance of conventional Can tuners while reducing the size of the tuner function. Additionally, the following benefits are provided:
  - Easy on-board integration
  - Easy dual tuner configuration
  - Drastic size reduction of the tuner function and power consumption

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{RF(STO)}$	RF frequency on pin STO	slave tuner output		45	-	864	MHz
NF_{tun}	tuner noise figure	maximum gain		-	5.5	-	dB
φ_n	phase noise	1 kHz and 10 kHz		-	–89	-	dBc/Hz
P	power dissipation			-	780	-	mW
$V_{i(max)}$	maximum input voltage	1 dB gain compression, one analog TV signal at RF input (–5 dBm)		-	103	-	dBµV
α_{image}	image rejection			-	65	-	dB
S_{dig}	digital sensitivity	DVB-T (64 QAM $^2/_3$); BER = 2.10^{-4}	[1]	-	–82	-	dBm
S_a	analog sensitivity	50 dB video SNR weighted 22 dBµV (color loss)	[2]	-	58	-	dBµV

[1] Measured with TDA10048HN channel decoder.

[2] Measured with TDA8295 IF modulator.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA18271HD/C2	HLQFN64R	plastic thermal enhanced low profile quad flat package; no leads; 64 terminals; resin based; body 9 × 9 × 1.6 mm	SOT903-1

6. Block diagram

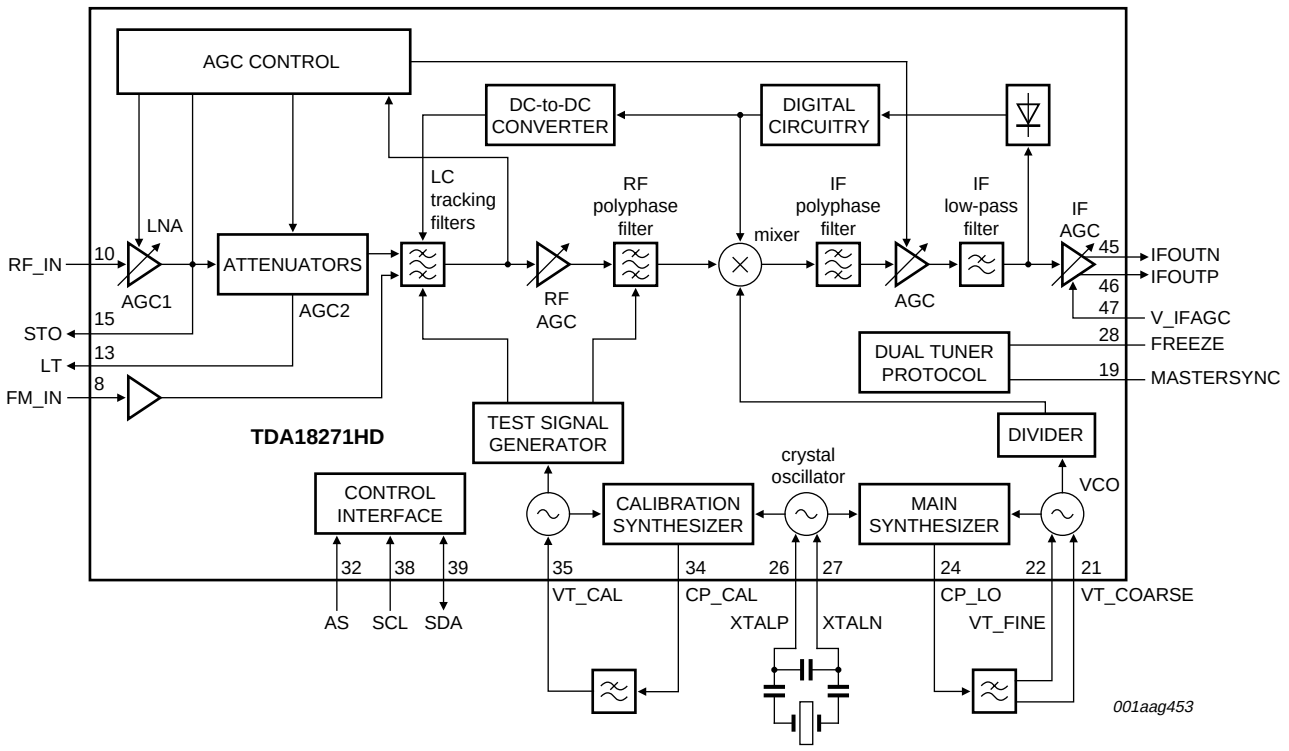


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

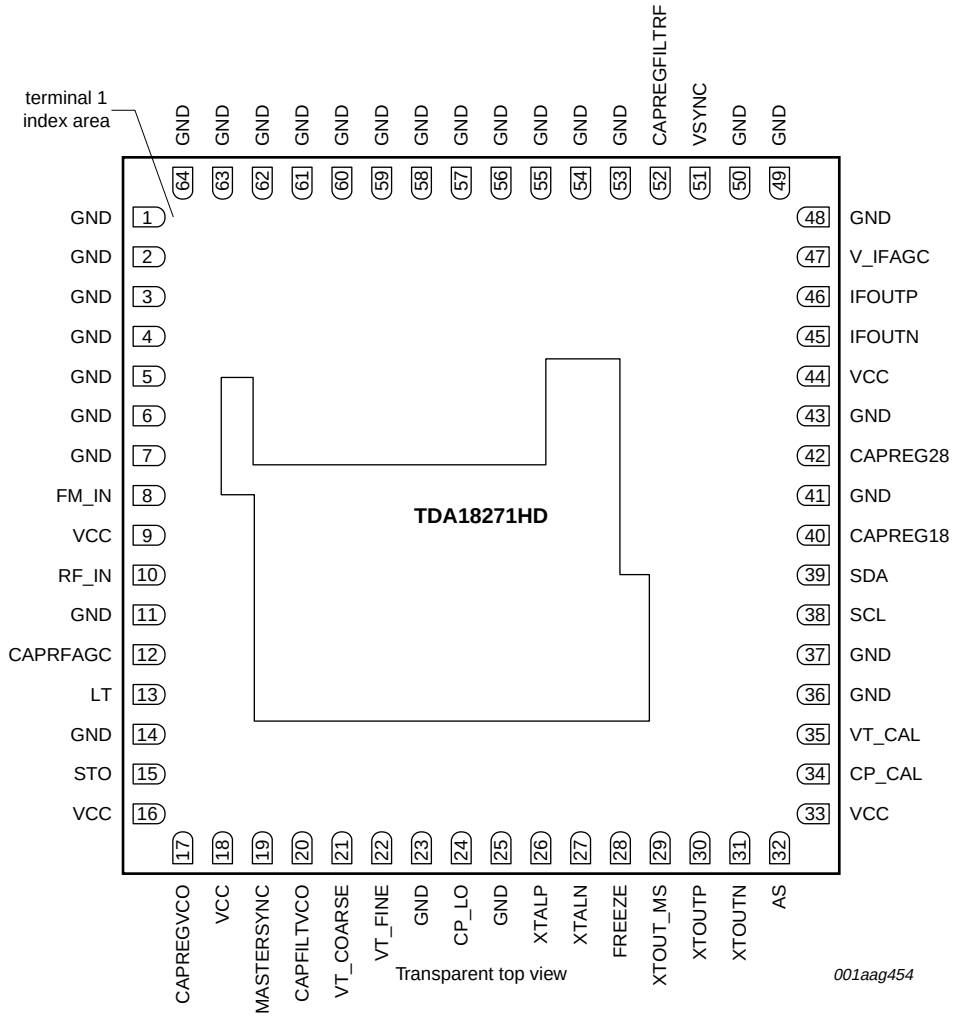


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	1 to 7	ground
FM_IN	8	unbalanced FM input
VCC	9	3.3 V supply voltage
RF_IN	10	unbalanced RF (TV) input
GND	11	ground
CAPRFAGC	12	RF AGC filtering

Table 3. Pin description *...continued*

Symbol	Pin	Description
LT	13	loop-through output
GND	14	ground
STO	15	slave tuner output
VCC	16	3.3 V supply voltage
CAPREGVCO	17	VCO supply decoupling
VCC	18	3.3 V supply voltage
MASTERSYNC	19	synchronization signal for dual tuner applications; leave open for single tuner applications
CAPFILTVCO	20	VCO reference decoupling
VT_COARSE	21	LO tuning voltage input
VT_FINE	22	LO tuning voltage input
GND	23	ground
CP_LO	24	charge pump of the local synthesizer
GND	25	ground
XTALP	26	crystal oscillator input
XTALN	27	crystal oscillator input
FREEZE	28	synchronization signal for multi tuner applications; leave open for single tuner applications
XTOUT_MS	29	XTOUT mode and master/slave selection
XTOUTP	30	crystal oscillator output buffer
XTOUTN	31	crystal oscillator output buffer
AS	32	I^2C-bus address selection input
VCC	33	3.3 V supply voltage
CP_CAL	34	charge pump of the calibration synthesizer
VT_CAL	35	tuning voltage of the calibration synthesizer
GND	36, 37	ground
SCL	38	I^2C-bus clock input
SDA	39	I^2C-bus data input/output
CAPREG18	40	internal regulator decoupling
GND	41	ground
CAPREG28	42	internal regulator decoupling
GND	43	ground
VCC	44	3.3 V supply voltage
IFOUTN	45	IF output
IFOUTP	46	IF output
V_IFAGC	47	IF gain control input
GND	48 to 50	ground
VSYNC	51	vertical synchronization input for analog applications; connect to ground for digital applications
CAPREGFILTRF	52	internal regulator decoupling
GND	53 to 64	ground
GND	exposed die	ground

8. Functional description

The RF input signal is driven to a low-noise amplifier. It is then band-pass filtered, amplified and fed to the image rejection mixer. The mixer downconverts the RF signal to a low IF depending on the channel bandwidth.

Standard IF filters are implemented for 1.5 MHz, 6 MHz, 7 MHz and 8 MHz channel bandwidths; see Table 43.

The Silicon Tuner can be used either as TV receiver or FM radio receiver.

The TDA18271HD requires a single 16 MHz crystal for clock generation. When bit XTOUT_ON = 1, a clock signal is available on pins XTOUTP and XTOUTN to drive a second tuner, a channel decoder or an IF demodulator (TDA8295) for analog TV reception and FM radio.

Remark: Most recent video decoders from NXP Semiconductors include a low IF demodulation function.

8.1 TV and FM reception

The Silicon Tuner can be used in two modes, selectable via the I^2C-bus:

- TV reception: the RF signal must be connected to pin RF_IN
- FM reception: the RF signal must be connected to pin FM_IN or RF_IN

The RF_IN input pin can also be used for FM reception at the cost of software modification. The FM_IN input pin can only receive signals in the FM frequency range.

8.2 Master and slave operation

The TDA18271HD allows easy dual-tuner configuration.

Each individual tuner has to be set either to Master mode or Slave mode by applying a specific DC voltage to the XTOUT_MS pin; see Table 4. This will decide whether the crystal oscillator part is used as negative impedance connected to the crystal part or as a current buffer.

Table 4. Master/slave selection

Voltage on pin XTOUT_MS	Tuner type	Crystal oscillator function
0 V to $0.1V_{CC}$	master	negative impedance presented to the crystal
$0.4V_{CC}$ to $0.6V_{CC}$	slave	current input buffer

In dual tuner applications:

- The first tuner is set to Master mode
- The second tuner has to be set to Slave mode

In single tuner applications:

- The tuner must be set to Master mode

8.3 Tuner outputs

The tuner provides a slave tuner output (pin STO) and a loop-through output (pin LT). These outputs are used to transmit the antenna signal to other tuners. Each output has its own characteristics (see Table 58 and Table 59).

8.3.1 Loop-through output

The gain between the antenna connector and the loop-through pin (pin LT) equals 0 dB. This pin can be connected to any consumer electronic equipment.

8.3.2 Slave tuner output

In dual tuner applications the slave tuner output (pin STO) must be connected to the RF input of the slave tuner TDA18271HD.

The gain between the antenna connector and the slave tuner output can change according to the input level. The slave tuner will automatically compensate for the gain change, using the MASTERSYNC and FREEZE signals.

8.4 Crystal input mode

The TDA18271HD requires a 16 MHz crystal reference. The chosen crystal must withstand at least 100 µW drive level and an additional shunt capacitor with a typical value of 5.6 pF as shown in Figure 1 is also needed. The quartz references for which the performances are guaranteed are:

- NDK NX5032
- Siward SX-5032
- TXC 9C series
- Chungho Elcom HC49S profile

Clock reference:

- In Master mode, the clock reference must be provided by a 16 MHz crystal connected between pins XTALP and XTALN of the master tuner
- In Slave mode, the clock reference must be provided by pins XTOUTP and XTOUTN of the tuner in Master mode to pins XTALP and XTALN of the tuner in Slave mode

8.5 Crystal output mode

Pins XTOUTP and XTOUTN deliver a symmetrical sine waveform to drive the channel decoder and/or IF demodulator. The load on these outputs should be made similar to ensure optimum performances. If only one crystal output is used, the unused output should be loaded by an equivalent capacitance.

9. Control interface

9.1 I²C-bus format, Write/Read mode

Remark: The I²C-bus read in the TDA18271HD must read the entire I²C-bus map, with required subaddress 00h. The number of bytes read is 16, or 39 in extended register mode; see Table 7. Reading write-only bits can return values that are different from the programmed values.

Table 5. I²C-bus format

Name	Byte name	Sub address	Bit							
			7	6	5	4	3	2	1	0
Address byte 1	-	-	1	1	0	0	0	MA[1:0]		R/W
Address byte 2	-	-	0	0	AD[5:0]					
ID byte	ID	00h	1	ID[6:0]						
Thermo byte	TM	01h	POR	LOCK	TM_RANGE	TM_ON	TM_D[3:0]			
Power level byte	PL	02h	POWER_LEVEL[7:0]							
Easy prog byte 1	EP1	03h	POWER_LEVEL[8]	DIS_POWER_LEVEL	0	RF_CAL_OK	IR_CAL_OK	BP_FILTER[2:0]		
Easy prog byte 2	EP2	04h	RF_BAND[2:0]			GAIN_TAPER[4:0]				
Easy prog byte 3	EP3	05h	SM	SM_LT	SM_XT	AGCK_MODE[1:0]		STD[2:0]		
Easy prog byte 4	EP4	06h	FM_RFN	XTOUT_ON	1	IF_LEVEL[2:0]			CAL_MODE[1:0]	
Easy prog byte 5	EP5	07h	EXTENDED_REG	IR_GSTEP[2:0]			0	IR_MEAS[2:0]		
Cal post-divider byte	CPD	08h	CAL_POST_DIV[7:0]							
Cal divider byte 1	CD1	09h	0	CAL_DIV[22:16]						
Cal divider byte 2	CD2	0Ah	CAL_DIV[15:8]							
Cal divider byte 3	CD3	0Bh	CAL_DIV[7:0]							
Main post-divider byte	MPD	0Ch	IF_NOTCH	MAIN_POST_DIV[6:0]						
Main divider byte 1	MD1	0Dh	0	MAIN_DIV[22:16]						
Main divider byte 2	MD2	0Eh	MAIN_DIV[15:8]							
Main divider byte 3	MD3	0Fh	MAIN_DIV[7:0]							
Extended byte 1	EB1	10h	EB1[7:3]					CALVCO_FORLON	AGC1_ALWAYS_MASTERN	AGC1_FIRSTN
Extended byte 2	EB2	11h	EB2[7:0]							
Extended byte 3	EB3	12h	EB3[7:0]							
Extended byte 4	EB4	13h	EB4[7:6]		LO_FORCE SRCE	EB4[4:0]				
Extended byte 5	EB5	14h	EB5[7:0]							
Extended byte 6	EB6	15h	EB6[7:0]							

Table 5. I²C-bus format *…continued*

Name	Byte name	Sub address	Bit							
			7	6	5	4	3	2	1	0
Extended byte 7	EB7	16h	EB7[7:6]		CAL_ FORCE SRCE	EB7[4:0]				
Extended byte 8	EB8	17h	CID_ALARM	EB8[6:4]			EB8[3]	EB8[2:0]		
Extended byte 9	EB9	18h	EB9[7:0]							
Extended byte 10	EB10	19h	EB10[7:6]		CID_GAIN[5:0]					
Extended byte 11	EB11	1Ah	EB11[7:0]							
Extended byte 12	EB12	1Bh	EB12[7:6]		PD_AGC1_ DET	PD_AGC2_ DET	EB12[3:0]			
Extended byte 13	EB13	1Ch	EB13[7]	RFC_K[2:0]			RFC_M[1:0]		EB13[1:0]	
Extended byte 14	EB14	1Dh	RFC_CPROG[7:0]							
Extended byte 15	EB15	1Eh	EB15[7:4]				EB15[3:0]			
Extended byte 16	EB16	1Fh	EB16[7:0]							
Extended byte 17	EB17	20h	EB17[7:0]							
Extended byte 18	EB18	21h	AGC1_ LOOP_OFF	EB18[6:2]					AGC1_GAIN[1:0]	
Extended byte 19	EB19	22h	EB19[7:0]							
Extended byte 20	EB20	23h	EB20[7:6]		FORCE_ LOCK	EB20[4:0]				
Extended byte 21	EB21	24h	AGC2_ LOOP_OFF	EB21[6:2]					AGC2_GAIN[1:0]	
Extended byte 22	EB22	25h	EB22[7]	RF_TOP[2:0]			IF_TOP[3:0]			
Extended byte 23	EB23	26h	EB23[7:3]					FORCELP_ FC2_EN	LP_FC	EB23[0]

9.2 I²C-bus at power-on reset

Table 6. I²C-bus at power-on reset

Name	Byte	Subaddress	7[1]	6[1]	5[1]	4[1]	3[1]	2[1]	1[1]	0[1]
Address byte 1	-	-	1	1	0	0	0	MA[1]	MA[0]	X
Address byte 2	-	-	X	X	AD[5]	AD[4]	AD[3]	AD[2]	AD[1]	AD[0]
ID byte	ID	00h	1	0	0	0	0	1	0	0
Thermo byte	TM	01h	1	0	0	0	X	X	X	X
Power level byte	PL	02h	X	X	X	X	X	X	X	X
Easy prog byte 1	EP1	03h	X	1	0	0	0	1	1	0
Easy prog byte 2	EP2	04h	1	1	0	1	1	1	1	1
Easy prog byte 3	EP3	05h	1	0	0	1	0	0	1	0
Easy prog byte 4	EP4	06h	0	1	1	0	0	0	0	0
Easy prog byte 5	EP5	07h	0	0	1	1	0	0	0	0
Cal post-divider byte	CPD	08h	0	0	0	0	0	0	0	0
Cal divider byte 1	CD1	09h	0	0	0	0	0	0	0	0
Cal divider byte 2	CD2	0Ah	0	0	0	0	0	0	0	0
Cal divider byte 3	CD3	0Bh	0	0	0	0	0	0	0	0
Main post-divider byte	MPD	0Ch	0	0	0	0	0	0	0	0
Main divider byte 1	MD1	0Dh	0	0	0	0	0	0	0	0
Main divider byte 2	MD2	0Eh	0	0	0	0	0	0	0	0
Main divider byte 3	MD3	0Fh	0	0	0	0	0	0	0	0
Extended byte 1	EB1	10h	1	1	1	1	1	1	1	1
Extended byte 2	EB2	11h	0	0	0	0	0	0	0	1
Extended byte 3	EB3	12h	1	0	0	0	0	1	0	0
Extended byte 4	EB4	13h	0	1	0	0	0	0	0	1
Extended byte 5	EB5	14h	0	0	0	0	0	0	0	1
Extended byte 6	EB6	15h	1	0	0	0	0	1	0	0
Extended byte 7	EB7	16h	0	1	0	0	1	0	0	0
Extended byte 8	EB8	17h	0	1	1	1	X	1	0	1
Extended byte 9	EB9	18h	0	0	0	0	0	0	0	0
Extended byte 10	EB10	19h	X	X	X	X	X	X	X	X
Extended byte 11	EB11	1Ah	1	0	0	0	0	1	1	0
Extended byte 12	EB12	1Bh	0	0	0	0	0	1	1	1
Extended byte 13	EB13	1Ch	1	1	0	0	0	0	1	0
Extended byte 14	EB14	1Dh	0	0	0	0	0	0	0	0
Extended byte 15	EB15	1Eh	1	0	0	0	X	X	X	X
Extended byte 16	EB16	1Fh	0	0	0	X	X	X	0	0
Extended byte 17	EB17	20h	0	0	0	X	X	X	X	X
Extended byte 18	EB18	21h	0	0	0	0	0	0	0	0
Extended byte 19	EB19	22h	0	0	0	X	X	X	0	0
Extended byte 20	EB20	23h	1	0	0	X	X	X	X	X

Table 6. I²C-bus at power-on reset *…continued*

Name	Byte	Subaddress	7[1]	6[1]	5[1]	4[1]	3[1]	2[1]	1[1]	0[1]
Extended byte 21	EB21	24h	0	0	1	1	0	0	1	1
Extended byte 22	EB22	25h	0	1	0	0	1	0	0	0
Extended byte 23	EB23	26h	1	0	1	1	0	0	0	0

[1] X indicates a bit not changed on reset.

9.3 Description of symbols used in I²C-bus format table

Table 7. I²C-bus register bits explanation

Address	Byte	Symbol	Description	Reference
		MA[1:0]	programmable address bits	Table 8
		AD[5:0]	programmable address bits of the first programming byte	Table 9
Data bytes				
00h	ID	ID[6:0]	chip identification number	Table 10
01h	TM	POR	Power-On Reset bit	Table 11
		LOCK	indicates that the main synthesizer is locked to the programmed frequency	
		TM_RANGE	range selection bit for the internal die sensor	
		TM_ON	enables die temperature measurement	
		TM_D[3:0]	data from die temperature measurement (read only)	
02h	PL	POWER_LEVEL[7:0]	Power level indicator value (read only)	Table 12
03h	EP1	POWER_LEVEL[8]		
		DIS_POWER_LEVEL	disables the power-on level function	Table 13
		RF_CAL_OK	indicates that the RF tracking filter calibration procedure has been successful	
		IR_CAL_OK	indicates that the complete image rejection calibration procedure has been successful	
		BP_FILTER[2:0]	RF band-pass filter selection	
04h	EP2	RF_BAND[2:0]	RF tracking filter band selection	Table 14
		GAIN_TAPER[4:0]	gain taper value	
05h	EP3	SM	Sleep mode, Standby modes	Table 15
		SM_LT		
		SM_XT		
		AGCK_MODE[1:0]	defines the standard	
		STD[2:0]	defines the standard	
06h	EP4	FM_RFN	selects which input is fed to RF filter	Table 18
		XTOUT_ON	provides the 16 MHz crystal reference on the XTOUTP and XTOUTN pins	
		IF_LEVEL[2:0]	IF output level selection	
		CAL_MODE[1:0]	calibration mode selection	
07h	EP5	EXTENDED_REG	enables the extended register addressing	Table 19
		IR_GSTEP[2:0]	gain step for image rejection calibration	
		IR_MEAS[2:0]	image rejection measurement frequency range	

Table 7. I²C-bus register bits explanation *…continued*

Address	Byte	Symbol	Description	Reference
08h	CPD	CAL_POST_DIV[7:0]	calibration synthesizer post-divider	Table 20
09h	CD1	CAL_DIV[22:16]	calibration synthesizer main divider bits	Table 21
0Ah	CD2	CAL_DIV[15:8]		
0Bh	CD3	CAL_DIV[7:0]		
0Ch	MPD	IF_NOTCH	adds a DC notch in IF for a better adjacent channels rejection; depends on standards	Table 22
		MAIN_POST_DIV[6:0]	LO synthesizer post-divider bits	
0Dh	MD1	MAIN_DIV[22:16]	LO synthesizer main divider bits	Table 23
0Eh	MD2	MAIN_DIV[15:8]		
0Fh	MD3	MAIN_DIV[7:0]		
Extended bytes				
10h	EB1	CALVCO_FORLON	determines which VCO is used during Normal mode operations	Table 24
		AGC1_ALWAYS_MASTERN	enables AGC1 normal operation whatever the tuner type (master or slave)	
		AGC1_FIRSTN	determines which AGC (1 or 2) will be detected when detectors 1 and 2 are up	
13h	EB4	LO_FORCESRCE	forces the main PLL charge pump to source current to the main PLL loop filter	
16h	EB7	CAL_FORCESRCE	forces the calibration PLL charge pump to source current to the calibration PLL loop filter	
17h	EB8	CID_ALARM	indicates that signal sensed by the power detector used during calibrations is out of range	
19h	EB10	CID_GAIN[5:0]	calibration power detector output	
1Bh	EB12	PD_AGC1_DET	power-down of AGC1 detector	
		PD_AGC2_DET	power-down of AGC2 detector	
1Ch	EB13	RFC_K[2:0]	parameter used during the RF tracking filter calibration	
		RFC_M[1:0]	parameter used during the RF tracking filter calibration	
1Dh	EB14	RFC_CPROG[7:0]	tuning word of the RF tracking filters	
21h	EB18	AGC1_LOOP_OFF	turns off the AGC1 loop	
		AGC1_GAIN[1:0]	AGC1 gain	
23h	EB20	FORCE_LOCK	forces the internal PLLs lock indicator to logic 1	
24h	EB21	AGC2_LOOP_OFF	turns off the AGC2 loop	
		AGC2_GAIN[1:0]	AGC2 gain	
25h	EB22	RF_TOP[2:0]	Take-Over Point (TOP) of the RF AGC, detection in RF	
		IF_TOP[3:0]	TOP of the RF AGC, detection in IF	
26h	EB23	FORCELP_FC2_EN	FM filter selection	
		LP_FC		

9.3.1 I²C-bus address selection

The programmable module address bits MA[1:0] allow up to four tuners to be addressed in one system. Bits MA1 and MA0 are programmed by a specific voltage (V_{AS}) applied to pin AS. The relationship between the status of bits MA[1:0] and the voltage applied to pin AS is shown in Table 8.

Table 8. Address byte 1 bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7 to 3	-	R/W	1 1000*	must be set to 1 1000
2 to 1	MA[1:0]	R/W		programmable address bits
			00	V_{AS} = 0 V to 0.1 × V_{CC}
			01	V_{AS} = 0.2 × V_{CC} to 0.3 × V_{CC}
			10	V_{AS} = 0.4 × V_{CC} to 0.6 × V_{CC}
			11	V_{AS} = 0.9 × V_{CC} to V_{CC}
0	R/W	R/W	0	write mode
			1	read mode

Table 9. Address byte 2 bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7 to 6	-	R/W	00	must be set to 00
5 to 0	AD[5:0]	R/W	-	programmable address bits of the first programming byte

9.3.2 Description of chip ID byte

Table 10. ID - identification byte (subaddress 00h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7	-	R	1*	must be 1
6 to 0	ID[6:0]	R	000 0100*	TDA18271HD/C2 identification number

9.3.3 Description of temperature sensor byte

The temperature sensor is not available in Device-off mode, as it requires a 16 MHz clock to operate.

Table 11. TM - Thermo byte (subaddress 01h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7	POR	R	1*	power supply falls below the power-on reset level and is reset after a read operation ending with a stop condition
			0	power supply is above the power-on reset level
6	LOCK	R	1	main synthesizer is locked to the programmed frequency
			0*	main synthesizer is not locked to the programmed frequency
5	TM_RANGE	R/W		temperature range selection for the internal die sensor (see Table 52)
			1	92 °C to 122 °C
			0*	60 °C to 90 °C
4	TM_ON	R/W	1	enables die temperature measurement (see Table 52)
			0*	disables die temperature measurement (see Table 52)
3 to 0	TM_D[3:0]	R	XXXX	data from die temperature measurement (see Table 52)

9.3.4 Description of power level byte (read mode)

There are 9 power level bits sent in power level bytes 2 and 3. They indicate the composite voltage gain of the LNA, the loaded attenuator voltage gains, and the level at the input of the RF AGC.

Table 12. PL - Power level (address 02h and 03h) bit description

*Legend: * power-on reset value.*

Address	Register	Bit	Symbol	Access	Value	Description
03h	EP1	7	POWER_LEVEL[8]	R		AGC2 gain, attenuator voltage gain including load, the attenuator load is 50 Ω (allows the maximum gain of −6 dB)
02h	PL	7	POWER_LEVEL[7]			
					00	−15 dB
					01	−12 dB
					10	−9 dB
					11	−6 dB
		6 to 5	POWER_LEVEL[6:5]	R		AGC1 gain, LNA voltage gain, the LNA voltage gain assumes a 75 Ω source impedance and a low output impedance
					00	6 dB
					01	9 dB
					10	12 dB
					11	15 dB
		4 to 0	POWER_LEVEL[4:0]	R		sensed level at the input of the RF AGC, detector slope is −1 dB/step
					0 0000	103 dBµV (RMS value)
					0 0001	102 dBµV (RMS value)
					...	...
					1 1110	73 dBµV (RMS value)
					1 1111	72 dBµV (RMS value)

9.3.5 Description of Easy prog byte 1

Table 13. EP1 - Easy prog byte 1 (subaddress 03h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7	POWER_LEVEL[8]	R		see Table 12
6	DIS_POWER_LEVEL	R/W	1*	power level disabled
			0	power level enabled
5	-	R/W	0*	must be set to 0
4	RF_CAL_OK	R/W		RF tracking filter calibration procedure (see Section 9.4.9); updated each time the procedure is started
			1	successful
			0*	not successful

Table 13. EP1 - Easy prog byte 1 (subaddress 03h) bit description *...continued*

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
3	IR_CAL_OK	R/W		complete image rejection calibration procedure (see Section 9.4.4); can only be reset with POR
			1	successful
			0*	not successful
2 to 0	BP_FILTER[2:0]	R/W	110*	RF band-pass filter selection (see Table 44)

9.3.6 Description of Easy prog byte 2

Table 14. EP2 - Easy prog byte 2 (subaddress 04h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7 to 5	RF_BAND[2:0]	R/W	110*	RF tracking filter band selection (see Table 45)
4 to 0	GAIN_TAPER[4:0]	R/W		gain taper value (see Table 49)
			1 1111*	minimum attenuation
			0 0000	maximum attenuation

9.3.7 Description of Easy prog byte 3

The TDA18271HD has three different Standby modes. Two Standby modes are dedicated to special application demands; the third Standby mode is called ‘device-off’. It represents the smallest achievable power consumption.

Table 15. EP3 - Easy prog byte 3 (subaddress 05h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7 to 5	SM, SM_LT, SM_XT	R/W	100	Power modes Table 16
4 to 3	AGCK_MODE[1:0]	R/W	10010*	defines the standard
2 to 0	STD[2:0]	R/W		description of standards (see Table 43)

Table 16. Power modes

Bit			Circuit			Mode[1]
SM	SM_LT	SM_XT	Loop-through	Slave-tuner output	Crystal oscillator	
0	0	0	on	on	on	Normal mode
1	0	0	on	on	on	Standby mode with crystal oscillator, slave-tuner output and loop-through output on
1	1	0	off	off	on	Standby mode with only crystal oscillator and its output buffer on
1	1	1	off	off	off	Device-off mode

[1] In all modes, the I^2C-bus interface remains active. All other bit settings are invalid.

Table 17. AGC modes

Standard	AGC_MODE[1:0] EP3[4:3][1]		Reference signal
FM radio	1	1	internal
Analog TV standards	0	1	VSYNC
Digital TV standards	1	1	internal

[1] Depending on the programmed AGC_MODE, AGC1 can be synchronous with either VSYNC or an internal 16 MHz signal; for analog reception, when no synchronization signal is available for VSYNC pin, the internal reference may be used.

9.3.8 Description of Easy prog byte 4

Table 18. EP4 - Easy prog byte 4 (subaddress 06h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7	FM_RFN	R/W		selection which input is fed to RF filter
			1	FM input (RF LNA on; FM LNA on)
			0*	RF input (RF LNA on; FM LNA off)
6	XTOUT_ON	R/W	1*	16 MHz on pins XTOUT
			0	not 16 MHz on pins XTOUT
5	-	R/W	1*	must be set to logic 1
4 to 2	IF_LEVEL[2:0]	R/W		IF output level selection and attenuation with regard to 2 V (p-p)
			000*	2 V (p-p); 0 dB
			001	1.25 V (p-p); 4 dB
			010	1 V (p-p); 6 dB
			011	0.8 V (p-p); 8 dB
			100	not used
			101	not used
			110	0.6 V (p-p); 10.4 dB
			111	0.5 V (p-p); 12 dB
1 to 0	CAL_MODE[1:0]	R/W		calibration mode selection
			00*	no calibration (Normal mode)
			01	Power detection mode
			10	image rejection calibration (IRCAL) mode
			11	RF tracking filter calibration (RFCAL) mode

All calibrations require a precise set of sequential operations, therefore it is mandatory to follow the flowcharts described in Section 9.4.

The TDA18271HD has two calibration modes: one for the image rejection calibration and one for the RF tracking filter calibration.

The image rejection calibration optimizes tunable parameters inside the mixer using a set of internal measurements to ensure a 65 dB typical value of image rejection. The internal signal used during this phase is generated by the PLL calibration (CAL PLL).

The RF tracking filters central frequency can be adjusted with the tuning word RFC_CPROG. The RF tracking filter calibration (RFCAL) uses an internal tone at the input of the tracking filters (generated by CAL PLL) and finds the RFC_CPROG that corresponds to the maximum transmitted power. The RFCAL is just a small part of a more complex algorithm fully described in the flowcharts in Section 9.4.

The Power detection mode is a Normal mode in which the detector used for the calibrations is switched ON. This special mode enables power sensing at the input of the TDA18271HD and makes the power scan algorithm possible (see Section 9.4.8 "Flowchart TDA18271PowerScan").

9.3.9 Description of Easy prog byte 5

Table 19. EP5 - Easy prog byte 5 (subaddress 07h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7	EXTENDED_REG	R/W		enables extended register addressing
			1	extended register (10h to 26h)
			0*	limited register (00h to 0Fh); only 1 byte can be programmed after address 0Fh within 1 transmission
6 to 4	IR_GSTEP[2:0]	R/W	011*	gain step for image rejection calibration
3	-	R/W	0*	must be set to logic 0
2 to 0	IR_MEAS[2:0]	R/W	000*	image rejection measurement frequency range (see Table 53)

9.3.10 Description of Cal post-divider byte

Table 20. CPD - Cal post-divider byte (subaddress 08h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7 to 0	CAL_POST_DIV[7:0]	R/W	00h*	calibration synthesizer post-divider (see Table 48)

9.3.11 Description of Cal divider bytes 1, 2 and 3

Table 21. CD1, CD2 and CD3 - Cal divider bytes 1, 2 and 3 (address 09h, 0Ah and 0Bh) bit description

*Legend: * power-on reset value.*

Address	Register	Bit	Symbol	Access	Value	Description
09h	CD1	7	-	R/W	0*	must be set to 0
		6 to 0	CAL_DIV[22:16]	R/W	00h*	calibration synthesizer main divider bits
0Ah	CD2	7 to 0	CAL_DIV[15:8]	R/W	00h*	
0Bh	CD3	7 to 0	CAL_DIV[7:0]	R/W	00h*	

9.3.12 Description of Main post-divider byte

Table 22. MPD - Main post-divider byte (subaddress 0Ch) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7	IF_NOTCH	R/W	0*	adds a DC notch in IF for better adjacent channels rejection; depends on standards; see Table 43
6 to 0	MAIN_POST_DIV[6:0]	R/W	000	LO synthesizer post-divider; see Table 47

9.3.13 Description of Main divider bytes 1, 2 and 3

Table 23. MD1, MD2 and MD3 - Main divider bytes 1, 2 and 3 (address 0Dh, 0Eh and 0Fh) bit description

*Legend: * power-on reset value.*

Address	Register	Bit	Symbol	Access	Value	Description
0Dh	MD1	7	-	R/W	0*	must be set to 0
		6 to 0	MAIN_DIV[22:16]	R/W	00h*	LO synthesizer main divider bits
0Eh	MD2	7 to 0	MAIN_DIV[15:8]	R/W	00h*	
0Fh	MD3	7 to 0	MAIN_DIV[7:0]	R/W	00h*	

9.3.14 Description of Extended bytes 1 to 23

Table 24. EB1 to EB23 - Extended bytes 1 to 23 (address 10h to 26h) bit description

*Legend: * power-on reset value.*

Address	Register	Bit	Symbol	Access	Value	Description
10h	EB1	7 to 3	EB1[7:3]	R	1 1111*	extended byte 1
		2	CALVCO_FORLON	R		determines VCO used during Normal mode operations
					1*	LO VCO is used
					0	CAL VCO is used
		1	AGC1_ALWAYS_MASTERN	R		enables AGC1 normal operation whatever the tuner type (master or slave)
					1*	normal operation for the master; 6 dB fixed for the slave
					0	normal operation for both the master and the slave
		0	AGC1_FIRSTN	R		determines which AGC will be updated when detectors 1 and 2 are active
					1*	AGC1 and AGC2 both updated
					0	AGC1 has priority on AGC2
11h	EB2	7 to 0	EB2[7:0]	R/W	0000 0001*	extended byte 2
12h	EB3	7 to 0	EB3[7:0]	R/W	1000 0100*	extended byte 3

Table 24. EB1 to EB23 - Extended bytes 1 to 23 (address 10h to 26h) bit description *…continued*

*Legend: * power-on reset value.*

Address	Register	Bit	Symbol	Access	Value	Description
13h	EB4	7 to 6	EB4[7:6]	R/W	01*	extended byte 4
		5	LO_FORCESRCE	R/W	1	forces the main PLL charge pump to source current to the main PLL loop filter
					0*	no force
		4 to 0	EB4[4:0]	R/W	0 0001*	extended byte 4
14h	EB5	7 to 0	EB5[7:0]	R/W	0000 0001*	extended byte 5
15h	EB6	7 to 0	EB6[7:0]	R/W	1000 0100*	extended byte 6
16h	EB7	7 and 6	EB7[7:6]	R/W	01*	extended byte 7
		5	CAL_FORCESRCE	R/W	1	forces the CAL PLL charge pump to source current to the CAL PLL loop filter
					0*	no force
		4 to 0	EB7[4:0]	R/W	0 1000*	extended byte 7
17h	EB8	7	CID_ALARM	R		signal sensed by the power detector used during calibrations
					1	out of range
					0*	in range
		6 to 4	EB8[6:4]	R/W	111 0101*	extended byte 8
		3	EB8[3]	R		
		2 to 0	EB8[2:0]	R/W		
18h	EB9	7 to 0	EB9[7:0]	W	0000 0000*	extended byte 9
19h	EB10	7 and 6	EB10[7:6]	R	00*	extended byte 10
		5 to 0	CID_GAIN[5:0]	R	-	calibration power detector output
1Ah	EB11	7 to 0	EB11[7:0]	R/W	1000 0110*	extended byte 11
1Bh	EB12	7 and 6	EB12[7:6]	R	00*	extended byte 12
		5	PD_AGC1_DET	R/W		AGC1 detector
					1	power down
					0*	no power down
		4	PD_AGC2_DET	R/W		AGC2 detector
					1	power down
					0*	no power down
		3 to 0	EB12[3:0]	R/W	0111*	extended byte 12
1Ch	EB13	7	EB13[7]	R/W	1*	extended byte 13
		6 to 4	RFC_K[2:0]	R/W	100*	parameters used during the RF tracking filter calibration (see Table 46)
		3 and 2	RFC_M[1:0]	R/W	00*	
		1 to 0	EB13[1:0]	R/W	10*	extended byte 13
1Dh	EB14	7 to 0	RFC_CPROG[7:0]	R/W	0000 0000*	tuning word of the RF tracking filters
1Eh	EB15	7 to 4	EB15[7:4]	R/W	1000 XXXX*	extended byte 15
		3 to 0	EB15[3:0]	R		
1Fh	EB16	7 to 0	EB16[7:0]	W	000X XX00*	extended byte 16

Table 24. EB1 to EB23 - Extended bytes 1 to 23 (address 10h to 26h) bit description *…continued*

*Legend: * power-on reset value.*

Address	Register	Bit	Symbol	Access	Value	Description
20h	EB17	7 to 0	EB17[7:0]	W	000X XXXX*	extended byte 17
21h	EB18	7	AGC1_LOOP_OFF	R/W		turns the AGC1 loop
					1	off
					0*	on
		6 to 2	EB18[6:2]	R/W	00000*	extended byte 18
		1 and 0	AGC1_GAIN[1:0]	R/W		AGC1 gain
					00*	6 dB
					01	9 dB
					10	12 dB
					11	15 dB
22h	EB19	7 to 0	EB19[7:0]	W	000X XX00*	extended byte 19
23h	EB20	7 and 6	EB20[7:6]	W	10*	extended byte 20
		5	FORCE_LOCK	W		forces the internal lock indicator
					1	forced to logic 1
					0*	not forced
		4 to 0	EB20[4:0]	W	X XXXX*	extended byte 20
24h	EB21	7	AGC2_LOOP_OFF	R/W		turns the AGC2 loop
					1	off
					0*	on
		6 to 2	EB21[6:2]	R/W	00000*	extended byte 21
		1 and 0	AGC2_GAIN[1:0]	R/W		AGC2 gain
					00*	−15 dB
					01	−12 dB
					10	−9 dB
					11	−6 dB
25h	EB22	7	EB22[7]	R	0*	extended byte 22
		6 to 4	RF_TOP[2:0]	R/W	100*	Take-Over Point of the RF AGC, detection in RF
		3 to 0	IF_TOP[3:0]	R/W	1000*	Take-Over Point of the RF AGC, detection in IF
26h	EB23	7 to 3	EB23[7:3]	R/W	1 0110*	extended byte 23
		2	FORCELP_FC2_EN	R/W	0*	FM filter selection; see Table 25 and Table 26
		1	LP_FC	R/W	0*	
		0	EB23[0]	R/W	0*	extended byte 23

Table 25. Low-pass cut-off frequency when using RF_IN input

RF input	FORCELP_FC2_EN	LP_FC	STD[1:0]	Cut-off frequency (MHz)
RF_IN	1	1	XX	1.5
	0	X	00	6
	0	X	01	7
	0	X	10	8
	0	X	11	9

Table 26. Low-pass cut-off frequency when using FM_IN input

RF input	FORCELP_FC2_EN	LP_FC	STD[1:0]	Cut-off frequency (MHz)
FM_IN	1	0	00	6
	1	0	01	7
	1	0	10	8
	1	0	11	9
	1	1	XX	1.5

9.4 I²C-bus programming flowcharts

The following flowcharts describe how to:

- Initialize the TDA18271HD
- Launch the calibrations
- Go to Normal mode

The image rejection calibration and RF tracking filter calibration must be launched exactly as described in the flowchart, otherwise bad calibration or even blocking of the TDA18211HD can result making it impossible to communicate via the I²C-bus.

Proper internal initialization requires switching to Normal mode using a single I²C-bus sequence from subaddresses 03h to 0Fh.

9.4.1 Flowchart explanation

This section provides instructions for reading the flowcharts.

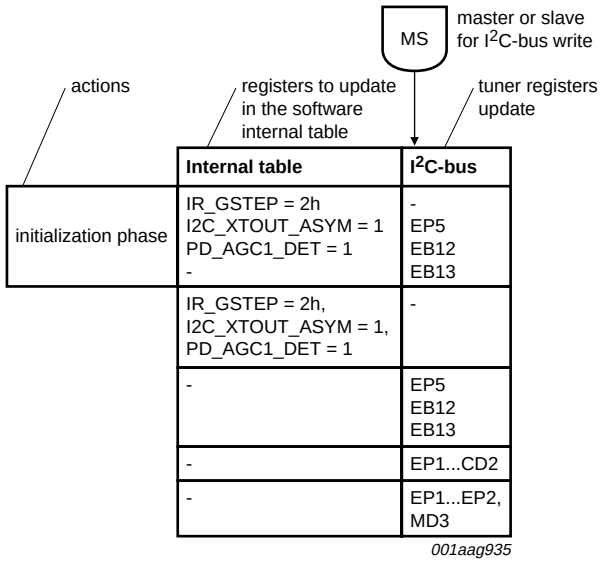


Fig 3. Programming sequence

1. I²C-bus write:
   - IR_GSTEP is updated, no immediate I²C-bus write
   - I2C_XTOUT_ASYM is updated followed by an I²C-bus write of byte EP5
   - PD_AGC1_DET is updated followed by an I²C-bus write of byte EB12
   - I²C-bus write of byte EB13 with current value of the software internal register of byte EB13

   I²C-bus read:
   - Subaddressing is not supported in read mode
   - The mandatory I²C-bus read access procedures to the TDA18271HD are described in Section 9.4.16 “Flowchart TDA18271Read” and Section 9.4.17 “Flowchart TDA18271ReadExtended”
2. Update at the same time is indicated by separation with commas:

   IR_GSTEP, I2C_XTOUT_ASYM and PD_AGC1_DET are updated, no I²C-bus registers updated
3. I²C-bus registers update bytes EP5, EB12 and EB13
4. Bytes EP1 to CD2 are written in a single I²C-bus sequence

   Example:

   Start C0 03 EP1 EP2 EP3 EP4 EP5 CPD CD1 CD2 Stop
5. Bytes EP1, EP2 and MD3 are written in as many I²C-bus sequences as needed

   Example:

   Start C0 03 EP1 EP2 Stop

   Start C0 0F MD3 Stop

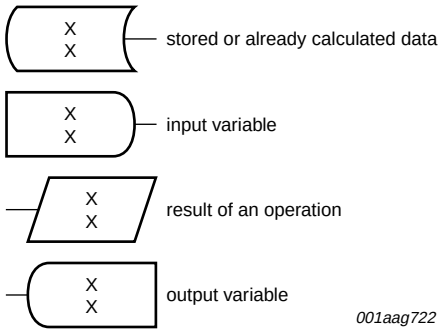
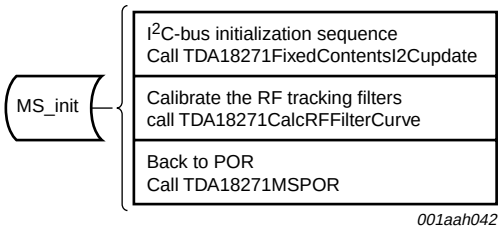
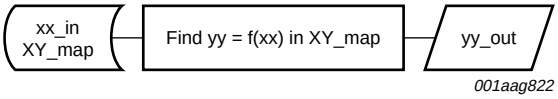


Fig 4. Blocks used in the flowcharts



Master/slave variable MS_init is input for each of the three procedures.

Fig 5. Variable used in multiple procedures

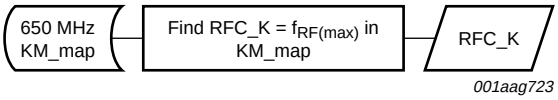


xx is a list of values stored in the first column of the map XY_map.

yy is a list of values stored in column in XY_map

yy_out is the particular value of yy to find row n. $xx(n-1) < xx\_in \leq xx(n)$

a. General description to find a value in a table



Finding the row of RFC_K: 350000 < 650000 ≤ 720000. Result n = 1. The value of RFC_K is then 3; see Table 46

b. Example to find the value RFC_K corresponding to f_{RF} = 650 MHz in the KM_map

Fig 6. Finding a value in a table

Units: In the flowcharts, hexadecimal values end with “h”, decimal values with “d”.

9.4.2 Flowchart TDA18271SetRf_dual

The initialization phase has to be launched before any SetRf.

Table 27. TDA18271SetRf_dual

Function	Description	Reference
Description	protocol top view for a dual tuner application	
Input	RF_freq, Standard (from microcontroller), MS (from microcontroller)[1]	
Table	-	
Output	-	

[1] MS = 1: master is selected for the channel configuration; MS = 0: slave is selected for the channel configuration.

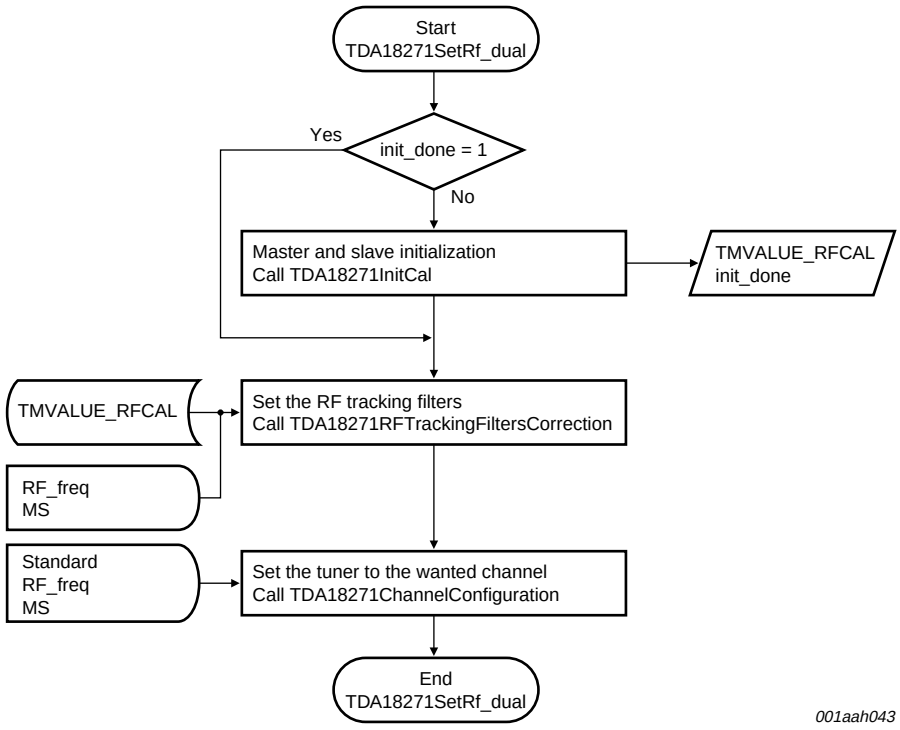


Fig 7. Flowchart TDA18271SetRf_dual

9.4.3 Flowchart TDA18271InitCal

Table 28. TDA18271InitCal

Function	Description	Reference
Description	systematic initializations for master and slave tuners	
Input	MS_init	
Table	-	
Output	TMVALUE_RFCAL, init_done	

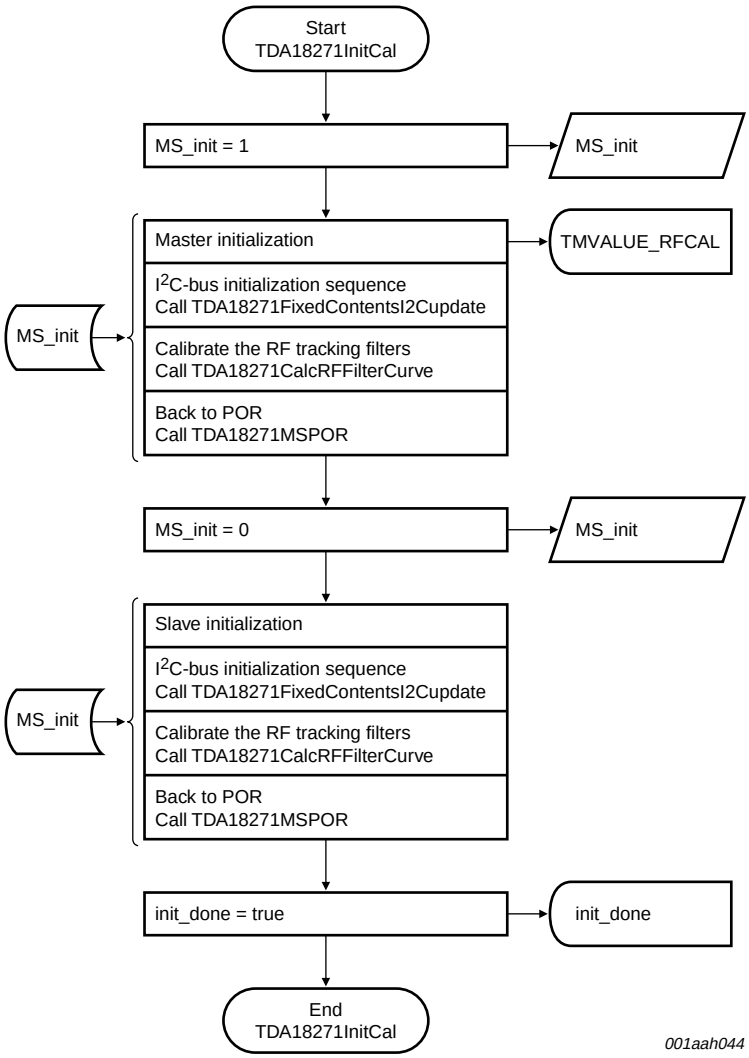


Fig 8. Flowchart TDA18271InitCal

9.4.4 Flowchart TDA18271FixedContentsI2Cupdate

Table 29. TDA18271FixedContentsI2Cupdate

Function	Description	Reference
Description	update and write the TDA18271HD registers sequential update of AGC1 and AGC2 image calibration algorithm	
Input	MS	
Table	-	
Output	-	

The register contents are not described in detail as this procedure is not to be modified.

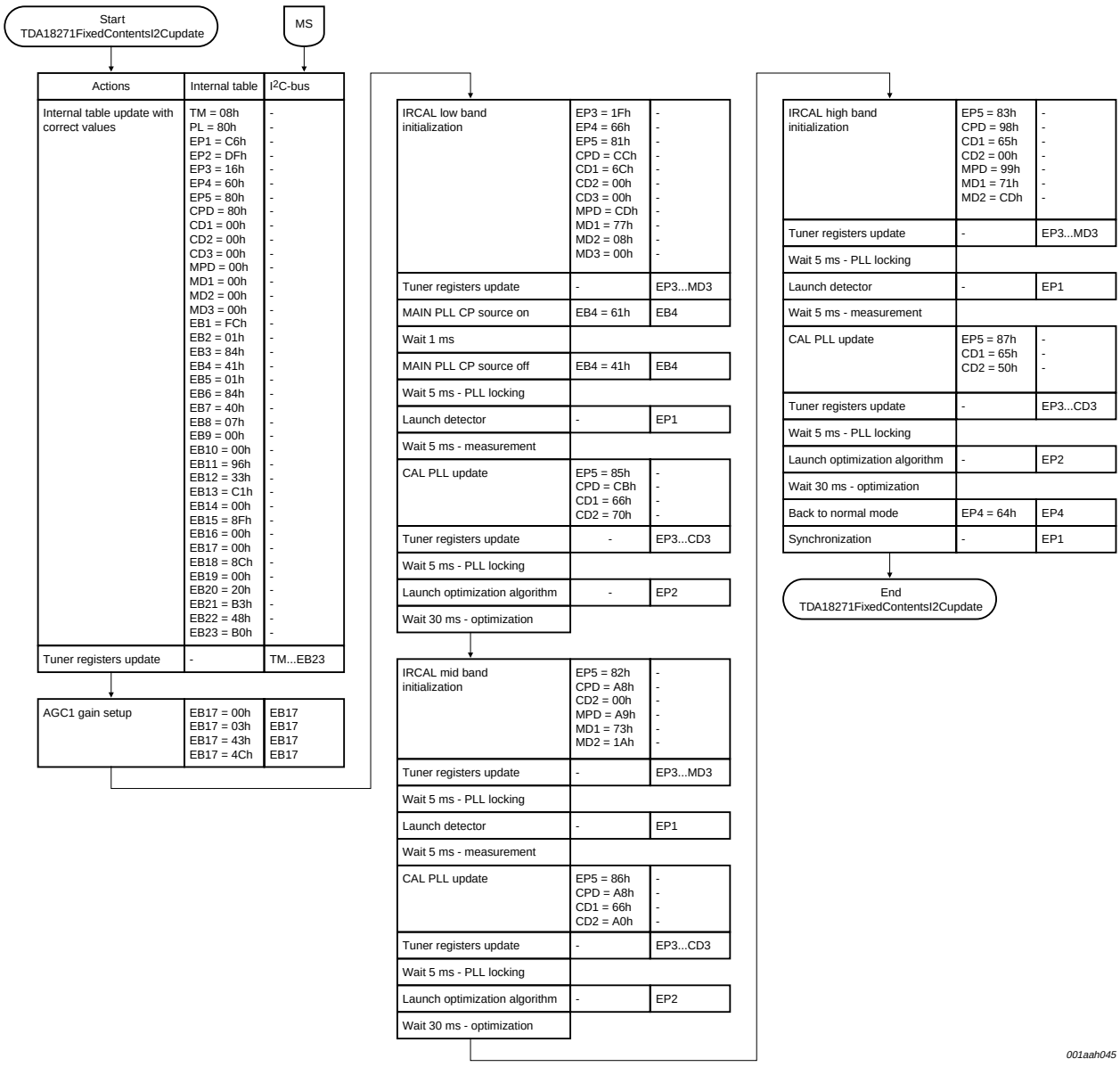
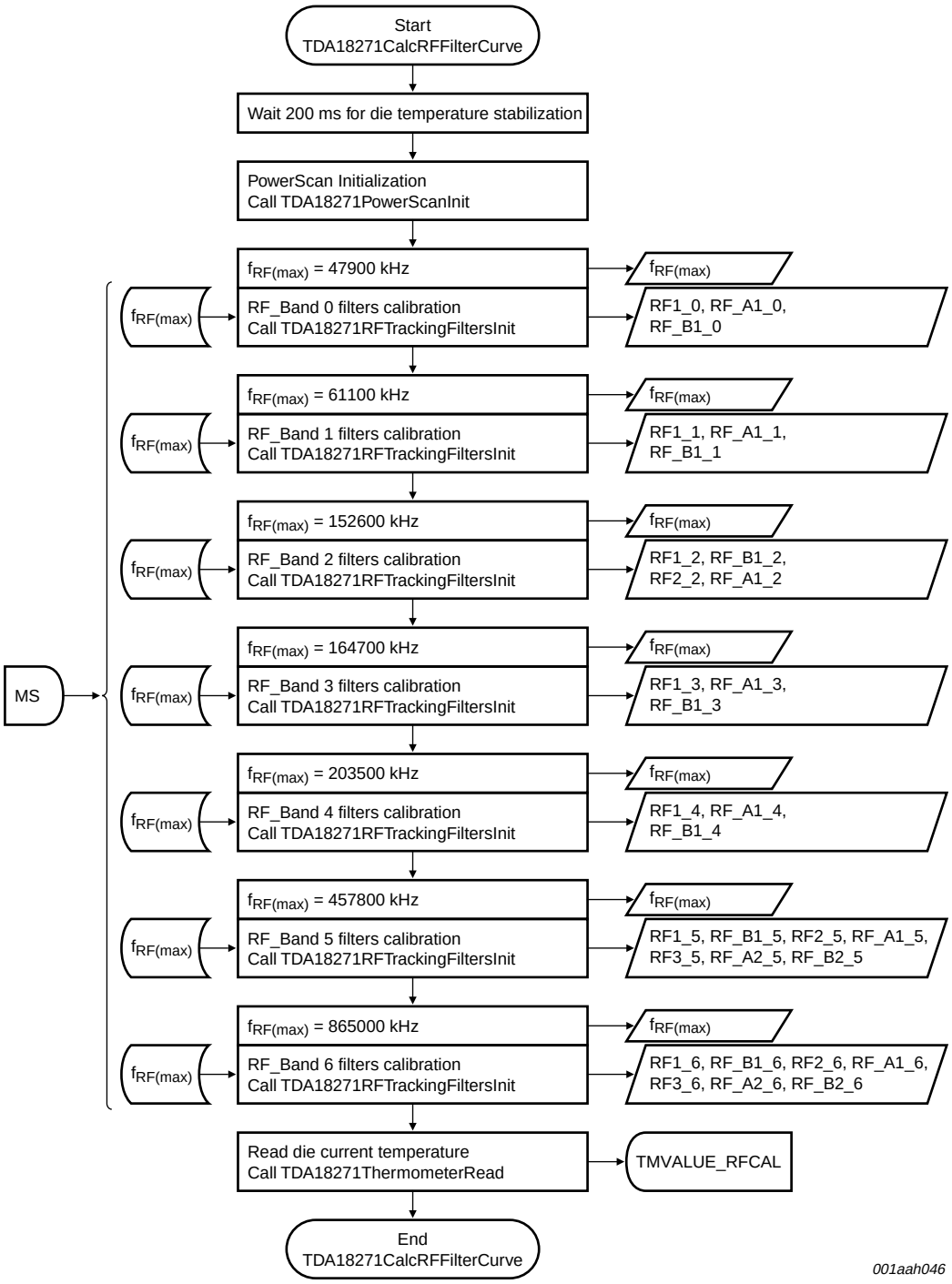


Fig 9. Flowchart TDA18271FixedContentsI2Cupdate

9.4.5 Flowchart TDA18271CalcRFFilterCurve

Table 30. TDA18271CalcRFFilterCurve

Function	Description	Reference
Description	calculate the RF filter curve coefficients	
Input	RF1_default, RF2_default, RF3_default, MS	
Table	RF_BAND_map	Table 45 “RF_BAND_map”
Output	TMVALUE_RFCAL	



Variable RF_max is used for frequency $f_{RF(max)}$.

Fig 10. Flowchart TDA18271CalcRFFilterCurve

9.4.6 Flowchart TDA18271RFTrackingFiltersInit

Table 31. TDA18271RFTrackingFiltersInit

Function	Description	Reference
Description	calculate the RF filter curve coefficients used for their approximation	
Input	$f_{RF(max)}$, MS	
Table	RF_CAL_map (Cprog_table = f (frequency))	Table 51 “RF_CAL_map”
Output	RF1, RF2, RF3, RF_A1, RF_B1, RF_A2, RF_B2	

bcal is a boolean output from TDA18271PowerScan:

bcal = 1 (true): enables the calibration of the RF tracking filters

bcal = 0 (false): no calibration is performed, default values for RFC_CPROG are used

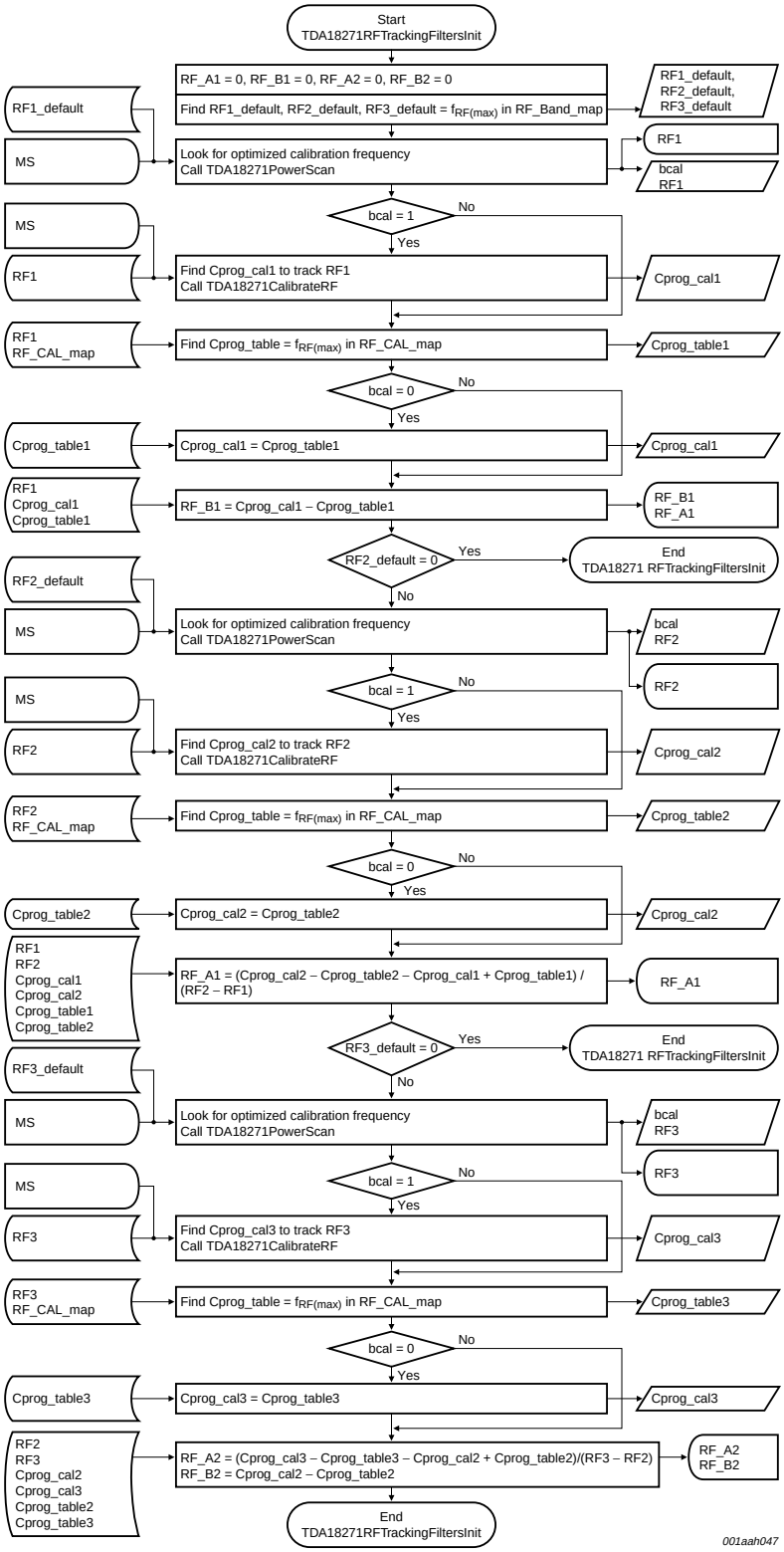


Fig 11. Flowchart TDA18271RFTrackingFiltersInit

9.4.7 Flowchart TDA18271PowerScanInit

Table 32. TDA18271PowerScanInit

Function	Description	Reference
Description	fixed settings of the TDA18271PowerScan	
Input	MS	
Table	-	
Output	-	

Frequency unit during the algorithm in kHz.

Variable count homogeneous to kHz.

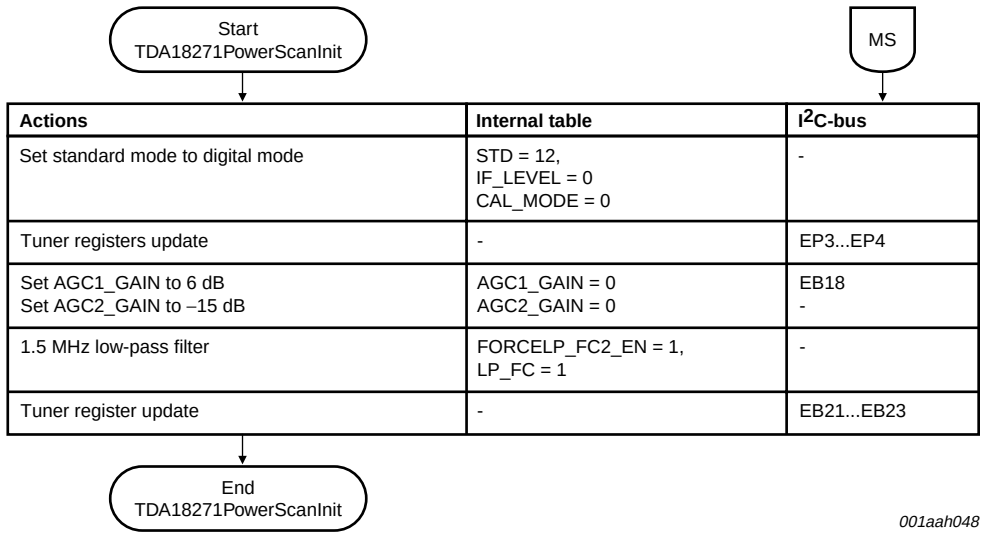


Fig 12. Flowchart TDA18271PowerScanInit

9.4.8 Flowchart TDA18271PowerScan

Table 33. TDA18271PowerScan

Function	Description	Reference
Description	find an interference-free calibration frequency	
Input	freq_input, MS	
Table	RF_BAND_map, RF_CAL_map, CID_Target_map	Table 45 “RF_BAND_map” Table 51 “RF_CAL_map” Table 54 “CID_Target_map”
Output	bcal, freq_output	

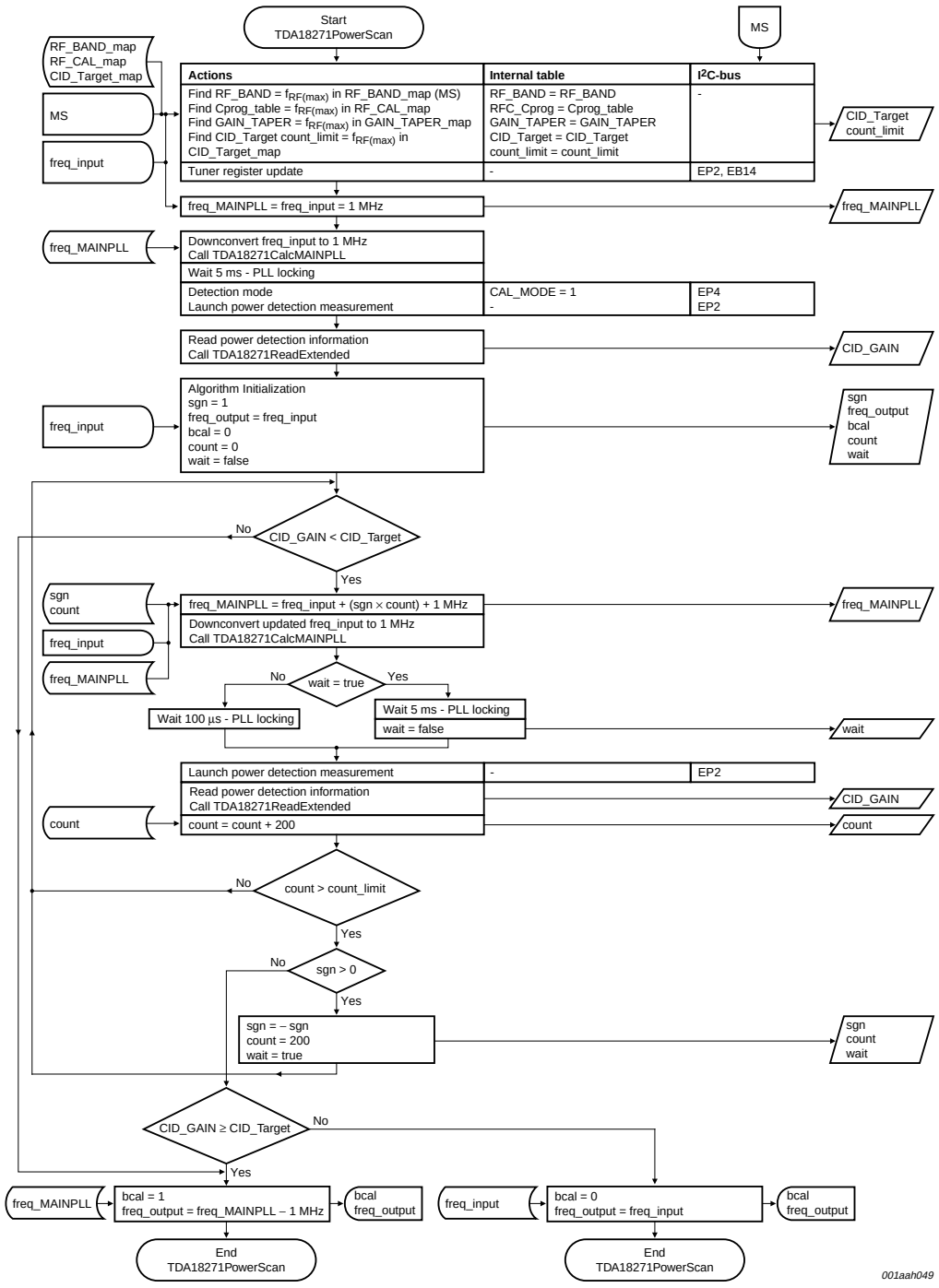


Fig 13. Flowchart TDA18271PowerScan

9.4.9 Flowchart TDA18271CalibrateRF

Table 34. TDA18271RFCalibrateRF

Function	Description	Reference
Description	finds the Cprog for which freq_input is the central frequency of the RF tracking filters	
Input	freq_input, MS	
Table	BP_FILTER_map, KM_map and GAIN_TAPER_map	Table 44 “BP_FILTER_map” Table 46 “KM_map” Table 49 “GAIN_TAPER_map”
Output	RFC_CPROG	

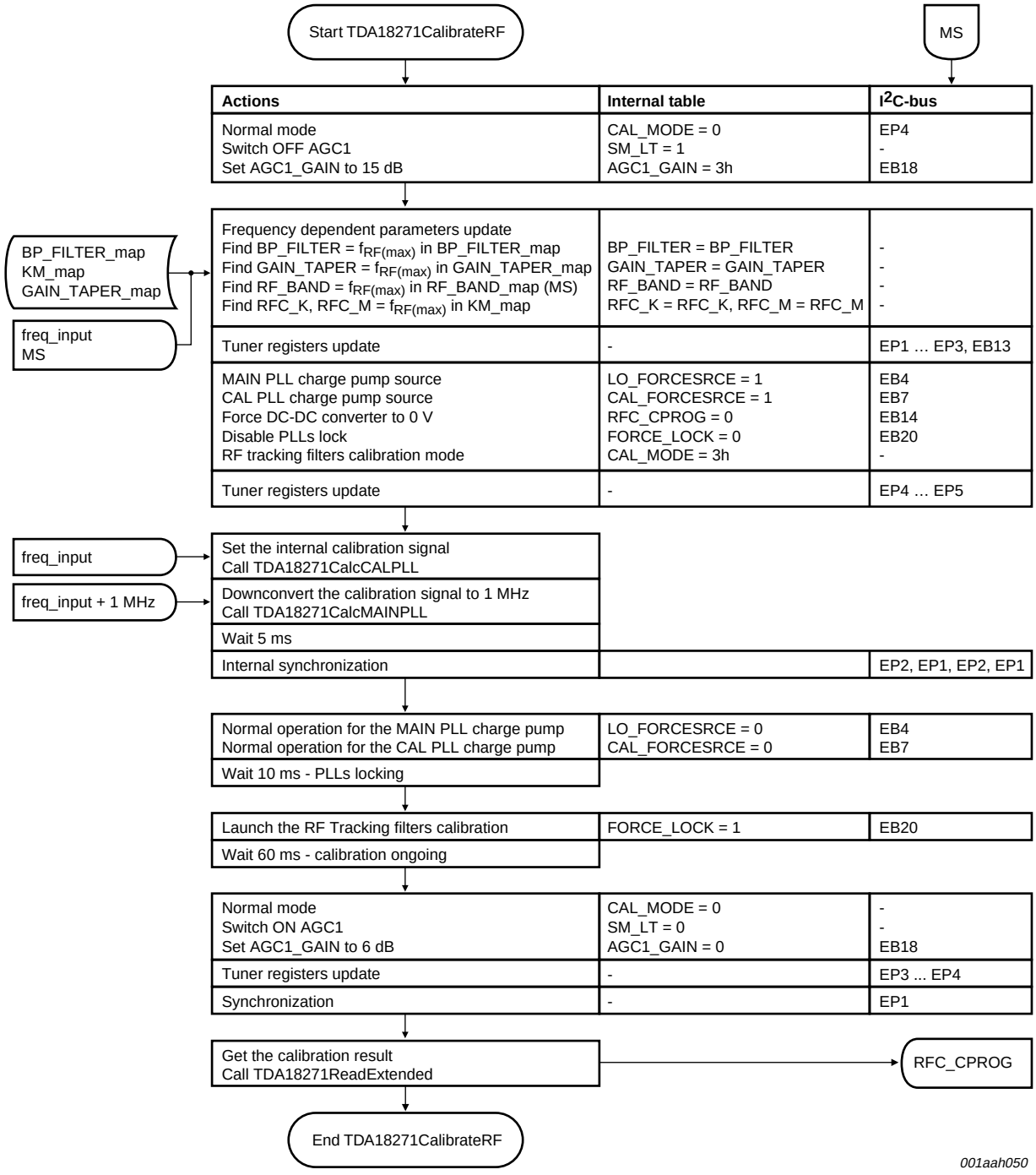


Fig 14. Flowchart TDA18271CalibrateRF

9.4.10 Flowchart TDA18271MSPOR

Table 35. TDA18271MSPOR

Function	Description	Reference
Description	master or slave tuner goes to Power-On Reset (POR) mode	
Input	MS	
Table	-	
Output	-	

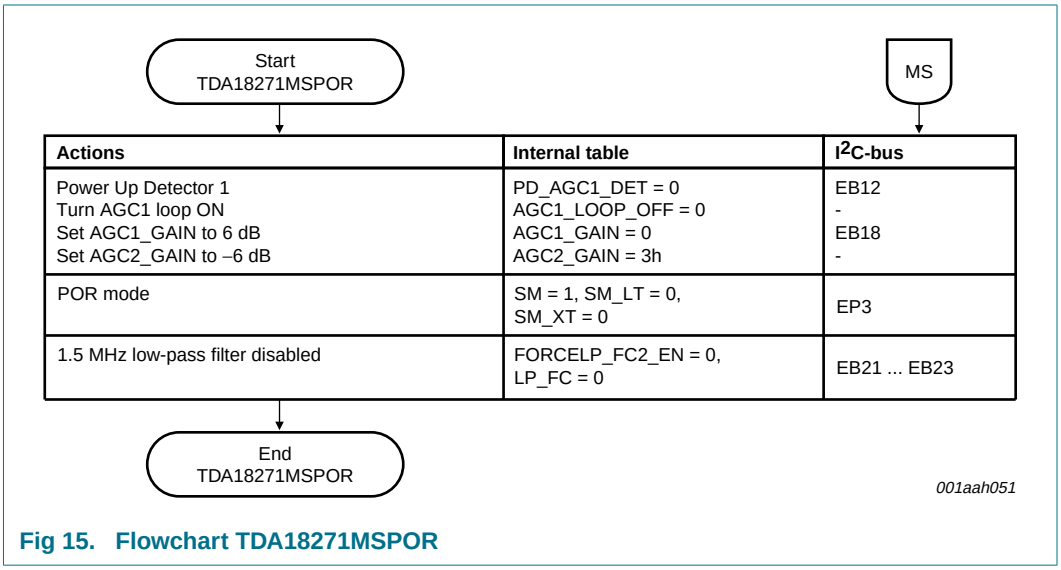


Fig 15. Flowchart TDA18271MSPOR

9.4.11 Flowchart TDA18271RFTrackingFiltersCorrection

Table 36. TDA18271RFTrackingFiltersCorrection

Function	Description	Reference
Description	find the Cprog corresponding to the programmed central frequency freq_input	
Input	freq_input, TMVALUE_RFCAL, MS	
Table	RF_BAND_map, RF_CAL_DC_OVER_DT_map, RF_CAL_map	Table 45 “RF_BAND_map” Table 50 “RF_CAL_DC_OVER_DT_map” Table 51 “RF_CAL_map”
Output	-	

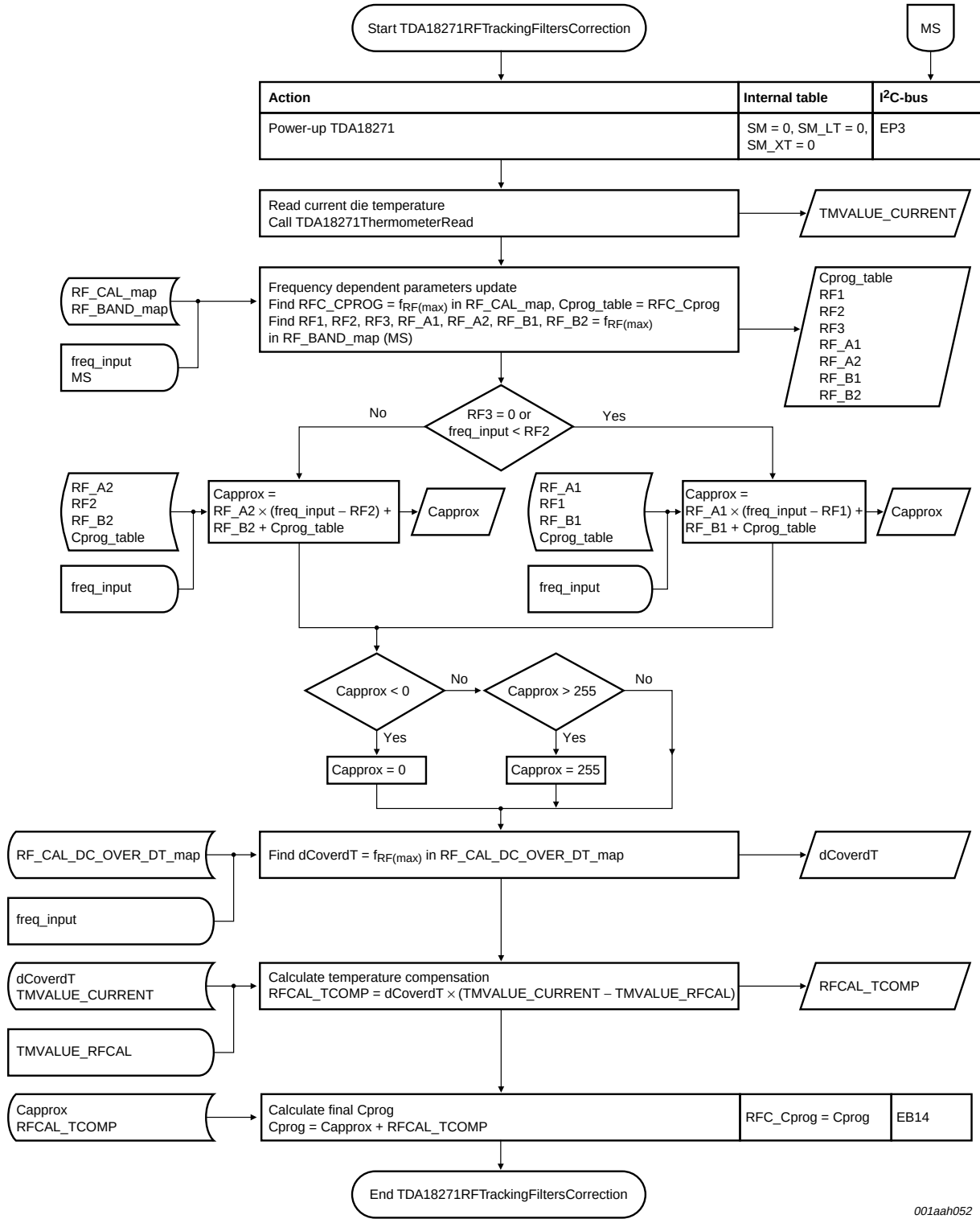


Fig 16. Flowchart TDA18271RFtrackingFiltersCorrection

9.4.12 Flowchart TDA18271ChannelConfiguration

Table 37. TDA18271ChannelConfiguration

Function	Description	Reference
Description	tunes the tuner according to the channel and broadcast configuration	
Input	freq_input, MS, Standard	
Table	STANDARD_DESCRIPTION_map, BP_FILTER_map, RF_BAND_map, CAL_PLL_map, GAIN_TAPER_map, IR_MEAS_map	Table 43 “STANDARD_DESCRIPTION_map” Table 44 “BP_FILTER_map” Table 45 “RF_BAND_map” Table 48 “CAL_PLL_map” Table 49 “GAIN_TAPER_map” Table 53 “IR_MEAS_map”
Output	-	

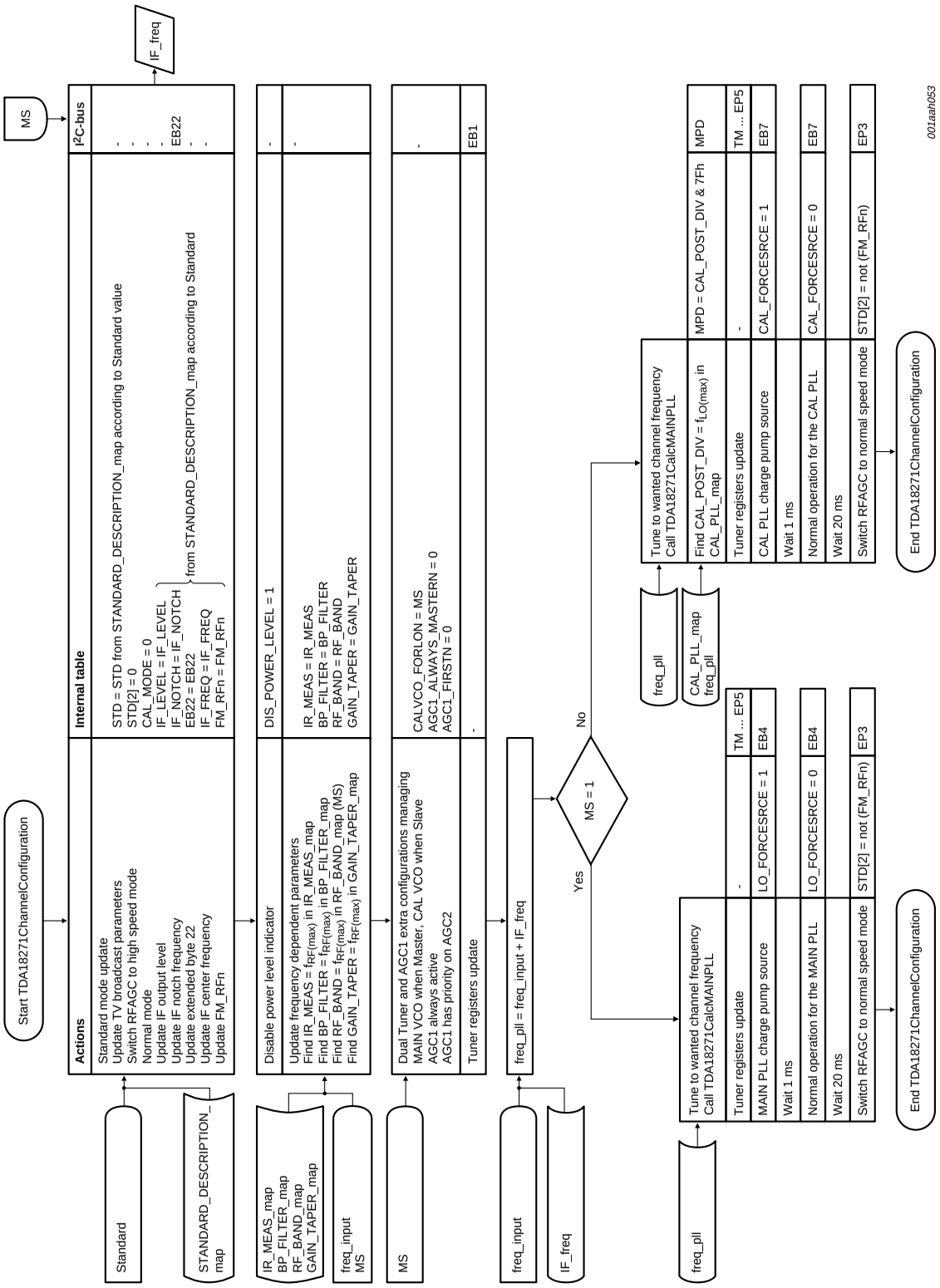


Fig 17. Flowchart TDA18271ChannelConfiguration

9.4.13 Flowchart TDA18271CalcMAINPLL

MPD, MD1, MD2 and MD3 are 8-bit registers. Arithmetical and logical operations performed on these registers are handled as binary operations. Dividing is right shifting and multiplying is left shifting.

Table 38. TDA18271CalcMAINPLL

Function	Description	Reference
Description	finds the correct values for the bytes MPD, MD1, MD2, MD3 and update the tuner registers	
Input	freq_input, MS	
Table	MAIN_PLL_map	Table 47 “MAIN_PLL_map”
Output	-	

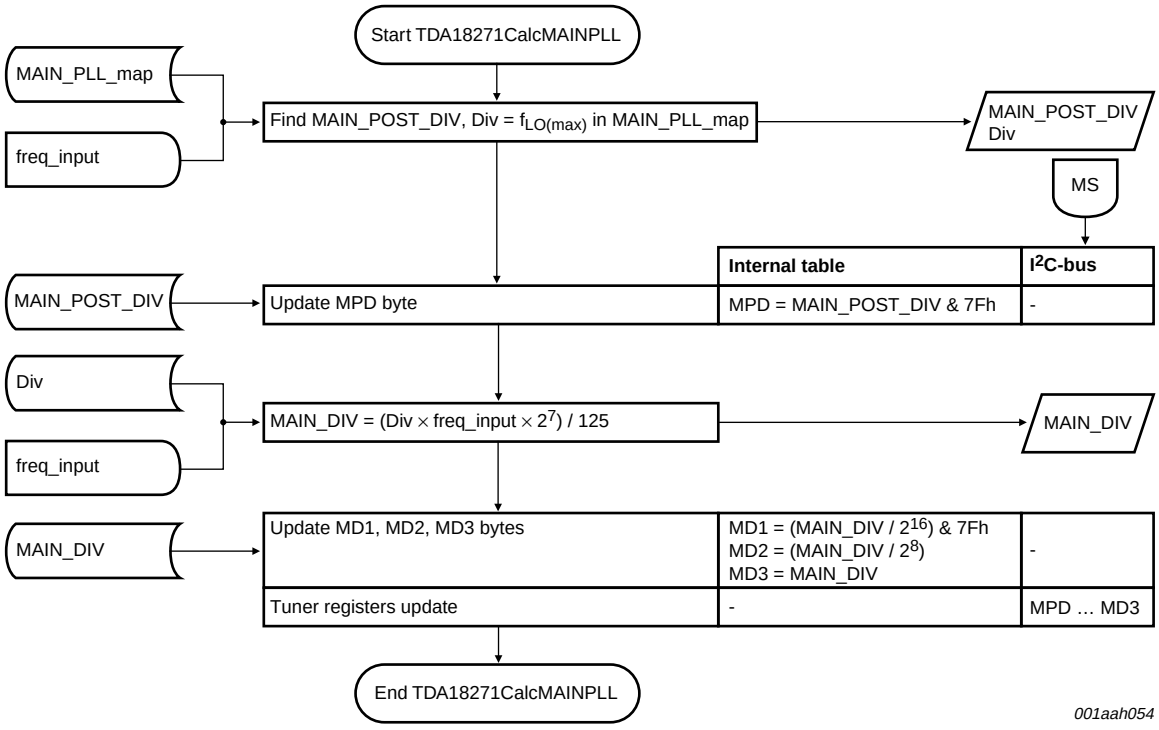


Fig 18. Flowchart TDA18271CalcMAINPLL

9.4.14 Flowchart TDA18271CalcCALPLL

CPD, CD1, CD2 and CD3 are 8-bit registers. Arithmetical and logical operations performed on these registers are handled as binary operations. Dividing is right shifting and multiplying is left shifting.

Table 39. TDA18271CalcCALPLL

Function	Description	Reference
Description	finds the correct values for the bytes CPD, CD1, CD2, CD3 and update the tuner registers	
Input	freq_input, MS	
Table	CAL_PLL_map	Table 48 “CAL_PLL_map”
Output	-	

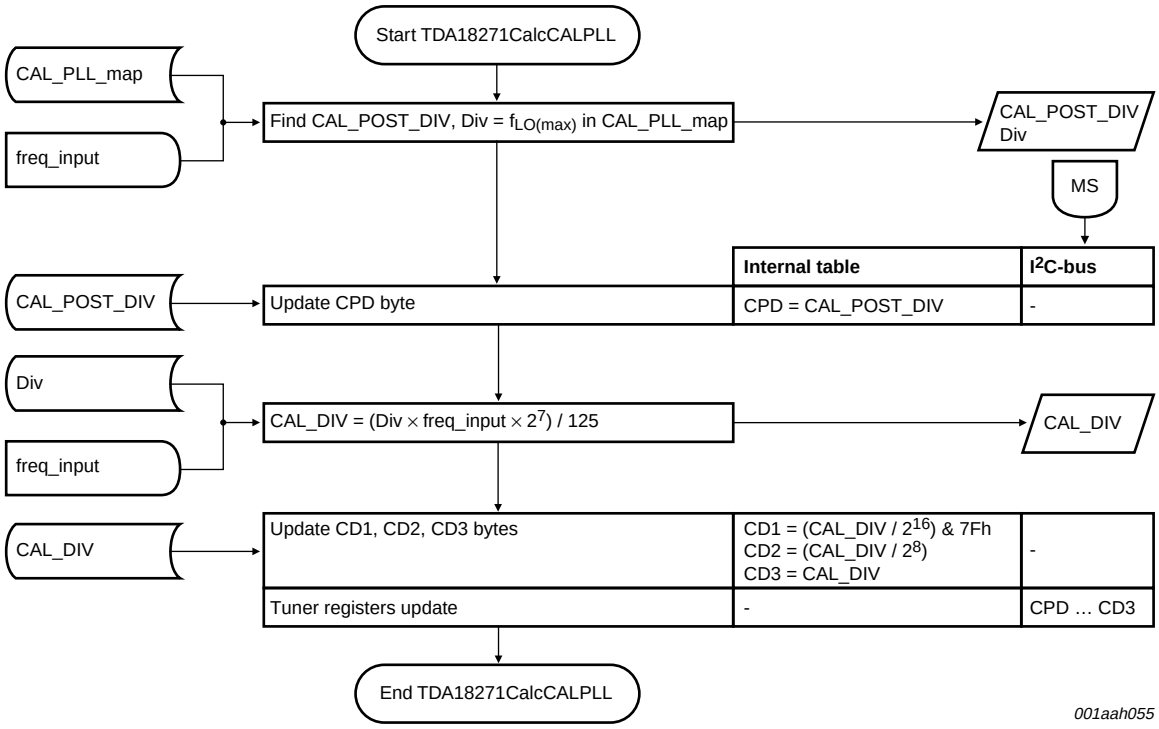


Fig 19. Flowchart TDA18271CalcCALPLL

9.4.15 Flowchart TDA18271ThermometerRead

Table 40. TDA18271ThermometerRead

Function	Description	Reference
Description	turns the on-chip temperature sensor ON, reads the current temperature on the die and then turns the temperature sensor OFF	
Input	MS	
Table	THERMOMETER_map	Table 52 “THERMOMETER_map”
Output	TMVALUE (temperature in °C)	

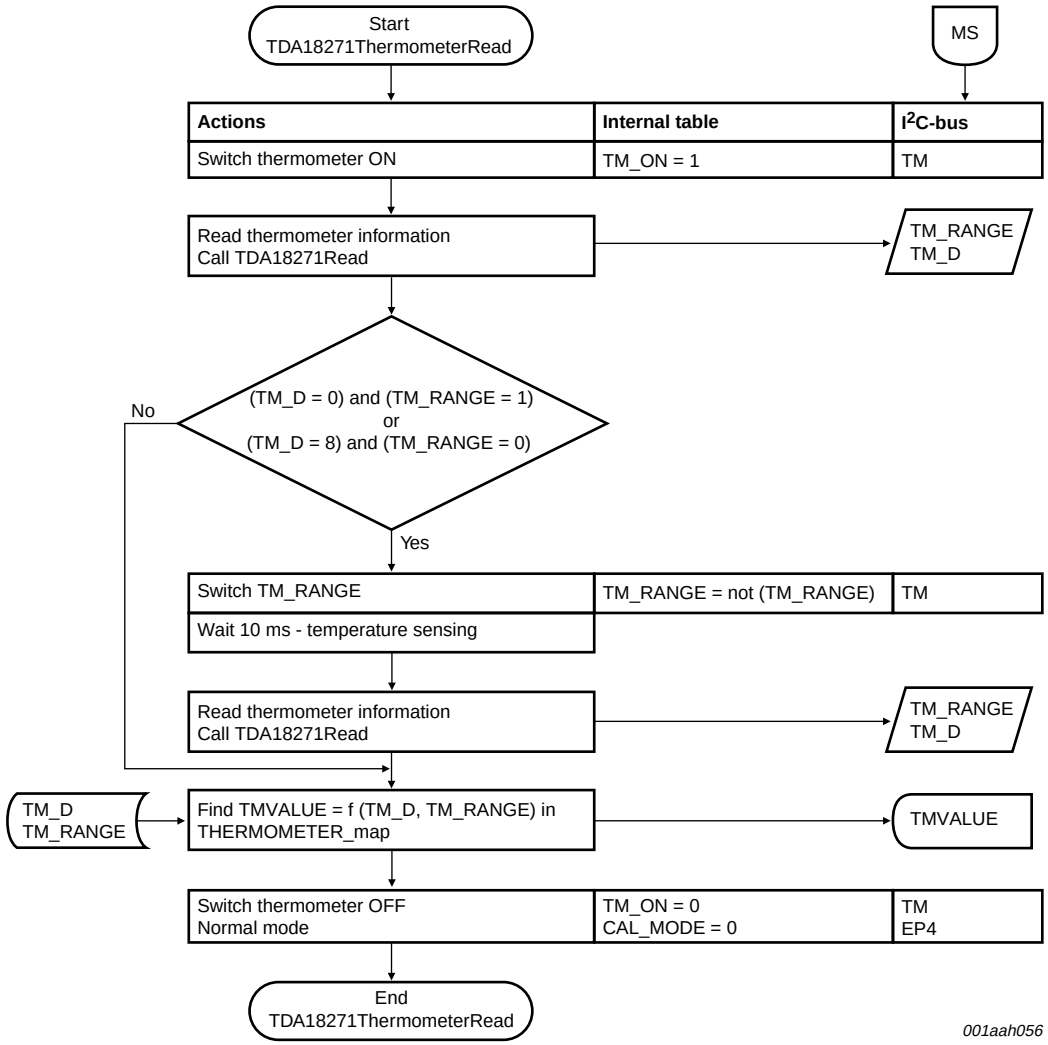


Fig 20. Flowchart TDA18271ThermometerRead

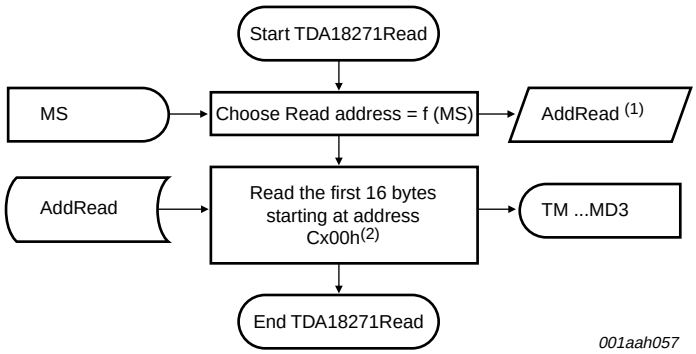
9.4.16 Flowchart TDA18271Read

Table 41. TDA18271Read

Function	Description	Reference
Description	reads the first 16 bytes of the TDA18271HD	
Input	MS	
Table	-	
Output	an image of the tuner registers from TM to MD3	

The internal software registers are never updated at any time during the read procedure but are updated when the TDA18271Read is called.

The I^{2}C-bus read in the TDA18271HD does not support subaddressing or variable length sequences. The chip can only be read by performing read sequences TDA18271Read (16 bytes) or TDA18271ReadExtended (39 bytes).



(1) AddRead = C1h, C3h, C5h or C7h.

(2) x = 1, 3, 5 or 7.

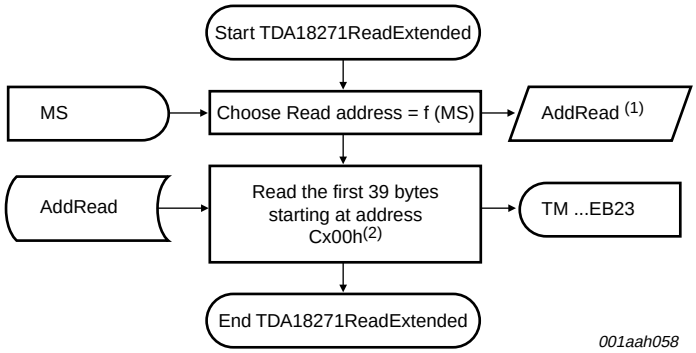
Fig 21. Flowchart TDA18271Read

9.4.17 Flowchart TDA18271ReadExtended

Table 42. TDA18271ReadExtended

Function	Description	Reference
Description	read the first 39 bytes of the TDA18271HD	
Input	MS	
Table	-	
Output	an image of the tuner registers from TM to EB23	

The internal software registers are not updated throughout a read procedure. The update is performed at the level of the call TDA18271ReadExtended.



(1) AddRead = C1h, C3h, C5h or C7h.

(2) x = 1, 3, 5 or 7.

Fig 22. Flowchart TDA18271ReadExtended

9.5 Maps

Table 43. STANDARD_DESCRIPTION_map

Standard	Selection		Recommended values[1]			
	STD[2:0]	FM_RFN	IF_LEVEL[2:0]	IF_NOTCH	EB22[7:0][2]	f_{IF} (MHz)
Radio						
FM radio	000	1	000	0	2Ch	1.25
Analog TV						
Analog TV std B	101	0	000	0	2Ch	6
Analog TV std D/K	110					6.9
Analog TV std G/H						7.1
Analog TV std I						7.25
Analog TV std L						6.9
Analog TV std L'						1.25
Analog TV std M/N	100					5.4
Digital TV[3]						
ATSC 6 MHz	100	0	001	1	37h	3.25
DVB-T 6 MHz						3.30
DVB-T 7 MHz						3.50
DVB-T 8 MHz	101					4
QAM 6 MHz						4
QAM 8 MHz	111					5

[1] Recommended values for analog and digital reception with a TDA8295 IF demodulator and a TDA10048HN channel decoder respectively.

[2] EB22[7:0] is the byte of the Take-Over Points of the RF_AGC (bits RF_TOP[2:0] and bits IF_TOP[3:0]).
The RF performances (see Section 13 "Characteristics") relate to these standard dependent arrangements. Any other combination of RF_TOP and IF_TOP fields is not recommended.

[3] Digital standard settings may vary, depending on channel decoder used.

Table 44. BP_FILTER_map

$f_{RF(max)}$ (kHz)	BP_FILTER[2:0]
62000	000
84000	001
100000	010
140000	011
170000	100
180000	101
865000	110

Table 45. RF_BAND_map

$f_{RF(max)}$ (kHz)	RF_BAND [2:0]	Used in flowchart							RF1_ default (kHz)	RF2_ default (kHz)	RF3_ default (kHz)
		RF_A1	RF_B1	RF_A2	RF_B2	RF1	RF2	RF3			
47900	000	RF_A1_0	RF_B1_0	RF_A2_0	RF_B2_0	RF1_0	0	0	46000	0	0
61100	001	RF_A1_1	RF_B1_1	RF_A2_1	RF_B2_1	RF1_1	0	0	52200	0	0
152600	010	RF_A1_2	RF_B1_2	RF_A2_2	RF_B2_2	RF1_2	RF2_2	0	70100	136800	0
164700	011	RF_A1_3	RF_B1_3	RF_A2_3	RF_B2_3	RF1_3	0	0	156700	0	0
203500	100	RF_A1_4	RF_B1_4	RF_A2_4	RF_B2_4	RF1_4	0	0	186250	0	0
457800	101	RF_A1_5	RF_B1_5	RF_A2_5	RF_B2_5	RF1_5	RF2_5	RF3_5	230000	345000	426000
865000	110	RF_A1_6	RF_B1_6	RF_A2_6	RF_B2_6	RF1_6	RF2_6	RF3_6	489500	697500	842000

Table 46. KM_map

$f_{RF(max)}$ (kHz)	RFC_K[2:0]	RFC_M[1:0]
47900	011	10
61100	100	01
350000	011	00
720000	010	01
865000	011	11

The KM_map refers to parameters used during the RF tracking filter calibration. These parameters are frequency dependent.

Table 47. MAIN_PLL_map

$f_{LO(max)}$ (kHz)	MAIN_POST_DIV[6:0]	Div[1]
33125	57h	F0h
35500	56h	E0h
38188	55h	D0h
41375	54h	C0h
45125	53h	B0h
49688	52h	A0h
55188	51h	90h
62125	50h	80h
66250	47h	78h
71000	46h	70h
76375	45h	68h
82750	44h	60h
90250	43h	58h
99375	42h	50h
110375	41h	48h
124250	40h	40h
132500	37h	3Ch
142000	36h	38h
152750	35h	34h
165500	34h	30h

Table 47. MAIN_PLL_map *…continued*

$f_{LO(max)}$ (kHz)	MAIN_POST_DIV[6:0]	Div[1]
180500	33h	2Ch
198750	32h	28h
220750	31h	24h
248500	30h	20h
265000	27h	1Eh
284000	26h	1Ch
305500	25h	1Ah
331000	24h	18h
361000	23h	16h
397500	22h	14h
441500	21h	12h
497000	20h	10h
530000	17h	0Fh
568000	16h	0Eh
611000	15h	0Dh
662000	14h	0Ch
722000	13h	0Bh
795000	12h	0Ah
883000	11h	09h
994000	10h	08h

[1] Used in Section 9.4.13 “Flowchart TDA18271CalcMAINPLL”.

Table 48. CAL_PLL_map

$f_{LO(max)}$ (kHz)	CAL_POST_DIV[7:0]	Div[1]
33813	DDh	D0h
36625	DCh	C0h
39938	DBh	B0h
43938	DAh	A0h
48813	D9h	90h
54938	D8h	80h
62813	D3h	70h
67625	CDh	68h
73250	CCh	60h
79875	CBh	58h
87875	CAh	50h
97625	C9h	48h
109875	C8h	40h
125625	C3h	38h
135250	BDh	34h
146500	BCh	30h
159750	BBh	2Ch

Table 48. CAL_PLL_map *…continued*

$f_{LO(max)}$ (kHz)	CAL_POST_DIV[7:0]	Div[1]
175750	BAh	28h
195250	B9h	24h
219750	B8h	20h
251250	B3h	1Ch
270500	ADh	1Ah
293000	ACh	18h
319500	ABh	16h
351500	AAh	14h
390500	A9h	12h
439500	A8h	10h
502500	A3h	0Eh
541000	9Dh	0Dh
586000	9Ch	0Ch
639000	9Bh	0Bh
703000	9Ah	0Ah
781000	99h	09h
879000	98h	08h

[1] Used in Section 9.4.14 “Flowchart TDA18271CalcCALPLL”.

Table 49. GAIN_TAPER_map

GAIN_TAPER[4:0][1]	$f_{RF(max)}$ (kHz)			
	1	2	3	4
1Fh	45400	154300	-	-
1Eh	45800	156100	-	-
1Dh	46200	157800	-	-
1Ch	46700	159500	-	-
1Bh	47100	161200	-	-
1Ah	47500	163000	-	-
19h	47900	164700	-	476300
18h	-	-	-	494800
17h	49600	170200	-	513300
16h	51200	175800	-	531800
15h	52900	181300	-	550300
14h	54500	186900	216200	568900
13h	56200	192400	228900	587400
12h	57800	198000	241600	605900
11h	59500	203500	254400	624400
10h	61100	-	267100	642900
0Fh	-	-	279800	661400
0Eh	-	-	292500	679900
0Dh	67600	-	305200	698400

Table 49. GAIN_TAPER_map *...continued*

GAIN_TAPER[4:0][1]	$f_{RF(max)}$ (kHz)			
	1	2	3	4
0Ch	74200	-	317900	716900
0Bh	80700	-	330700	735400
0Ah	87200	-	343400	753900
09h	93800	-	356100	772500
08h	100300	-	368800	791000
07h	106900	-	381500	809500
06h	113400	-	394200	828000
05h	119900	-	406900	846500
04h	126500	-	419700	865000
03h	133000	-	432400	-
02h	139500	-	445100	-
01h	146100	-	457800	-
00h	152600	-	-	-

[1] The gain taper function compensates for any systematic RF gain ripple, giving a flat RF gain with frequency.

Table 50. RF_CAL_DC_OVER_DT_map

$f_{RF(max)}$ (kHz)	dCoverdT[1]	$f_{RF(max)}$ (kHz)	dCoverdT[1]	$f_{RF(max)}$ (kHz)	dCoverdT[1]	$f_{RF(max)}$ (kHz)	dCoverdT[1]
47900	0h	383000	22h	457800	3Ch	754000	3Ch
55000	0h	386000	23h	465000	0Fh	759000	3Dh
61100	0Ah	389000	24h	477000	12h	764000	3Eh
64000	0Ah	393000	25h	483000	14h	769000	3Fh
82000	14h	396000	26h	502000	19h	774000	40h
84000	19h	399000	27h	508000	1Bh	779000	41h
119000	1Ch	402000	28h	519000	1Ch	784000	43h
124000	20h	404000	29h	522000	1Dh	789000	46h
129000	2Ah	407000	2Ah	524000	1Eh	794000	48h
134000	32h	409000	2Bh	534000	1Fh	799000	4Bh
139000	39h	412000	2Ch	549000	20h	804000	4Fh
144000	3Eh	414000	2Dh	554000	22h	809000	54h
149000	3Fh	417000	2Eh	584000	24h	814000	59h
152600	40h	419000	2Fh	589000	26h	819000	5Dh
154000	40h	422000	30h	658000	27h	824000	61h
164700	41h	424000	31h	664000	2Ch	829000	68h
203500	32h	427000	32h	669000	2Dh	834000	6Eh
353000	19h	429000	33h	699000	2Eh	839000	75h
356000	1Ah	432000	34h	704000	30h	844000	7Eh
359000	1Bh	434000	35h	709000	31h	849000	82h
363000	1Ch	437000	36h	714000	32h	854000	84h
366000	1Dh	439000	37h	724000	33h	859000	8Fh
369000	1Eh	442000	38h	729000	36h	865000	9Ah

Table 50. RF_CAL_DC_OVER_DT_map *...continued*

$f_{RF(max)}$ (kHz)	dCoverdT[1]	$f_{RF(max)}$ (kHz)	dCoverdT[1]	$f_{RF(max)}$ (kHz)	dCoverdT[1]	$f_{RF(max)}$ (kHz)	dCoverdT[1]
373000	1Fh	444000	39h	739000	38h	-	-
376000	20h	447000	3Ah	744000	39h	-	-
379000	21h	449000	3Bh	749000	3Bh	-	-

[1] Used in flowcharts.

Table 51. RF_CAL_map

$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table
41000	0Fh	127000	6Eh	208000	0Fh	370000	58h	521000	20h	740000	69h
43000	1Ch	128000	70h	212000	10h	372000	59h	525000	21h	741000	6Ah
45000	2Fh	129000	71h	216000	11h	375000	5Ah	529000	22h	742000	6Bh
46000	39h	130000	75h	217000	12h	376000	5Bh	533000	23h	743000	6Ch
47000	40h	131000	77h	218000	13h	377000	5Ch	539000	24h	745000	6Dh
47900	50h	132000	78h	220000	14h	379000	5Dh	541000	25h	747000	6Eh
49100	16h	133000	7Bh	222000	15h	382000	5Eh	547000	26h	748000	6Fh
50000	18h	134000	7Eh	225000	16h	384000	5Fh	549000	27h	750000	70h
51000	20h	135000	81h	228000	17h	385000	60h	551000	28h	752000	71h
53000	28h	136000	82h	231000	18h	386000	61h	556000	29h	754000	72h
55000	2Bh	137000	87h	234000	19h	388000	62h	561000	2Ah	757000	73h
56000	32h	138000	88h	235000	1Ah	390000	63h	563000	2Bh	758000	74h
57000	35h	139000	8Dh	236000	1Bh	393000	64h	565000	2Ch	760000	75h
58000	3Eh	140000	8Eh	237000	1Ch	394000	65h	569000	2Dh	763000	76h
59000	43h	141000	91h	240000	1Dh	396000	66h	571000	2Eh	764000	77h
60000	4Eh	142000	95h	242000	1Eh	397000	67h	577000	2Fh	766000	78h
61100	55h	143000	9Ah	244000	1Fh	398000	68h	580000	30h	767000	79h
63000	0Fh	144000	9Dh	247000	20h	400000	69h	582000	31h	768000	7Ah
64000	11h	145000	A1h	249000	21h	402000	6Ah	584000	32h	773000	7Bh
65000	12h	146000	A2h	252000	22h	403000	6Bh	588000	33h	774000	7Ch
66000	15h	147000	A4h	253000	23h	407000	6Ch	591000	34h	776000	7Dh
67000	16h	148000	A9h	254000	24h	408000	6Dh	596000	35h	777000	7Eh
68000	17h	149000	AEh	256000	25h	409000	6Eh	598000	36h	778000	7Fh
70000	19h	150000	B0h	259000	26h	410000	6Fh	603000	37h	779000	80h
71000	1Ch	151000	B1h	262000	27h	411000	70h	604000	38h	781000	81h
72000	1Dh	152000	B7h	264000	28h	412000	71h	606000	39h	783000	82h
73000	1Fh	152600	BDh	267000	29h	413000	72h	612000	3Ah	784000	83h
74000	20h	154000	20h	269000	2Ah	414000	73h	615000	3Bh	785000	84h
75000	21h	155000	22h	271000	2Bh	417000	74h	617000	3Ch	786000	85h
76000	24h	156000	24h	273000	2Ch	418000	75h	621000	3Dh	793000	86h
77000	25h	157000	25h	275000	2Dh	420000	76h	622000	3Eh	794000	87h
78000	27h	158000	27h	277000	2Eh	422000	77h	625000	3Fh	795000	88h
80000	28h	159000	29h	279000	2Fh	423000	78h	632000	40h	797000	89h

Table 51. RF_CAL_map *…continued*

$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table
81000	29h	160000	2Ch	282000	30h	424000	79h	633000	41h	799000	8Ah
82000	2Dh	161000	2Dh	284000	31h	427000	7Ah	634000	42h	801000	8Bh
83000	2Eh	163000	2Eh	286000	32h	428000	7Bh	642000	43h	802000	8Ch
84000	2Fh	164000	2Fh	287000	33h	429000	7Dh	643000	44h	803000	8Dh
85000	31h	164700	30h	290000	34h	432000	7Fh	647000	45h	804000	8Eh
86000	33h	166000	11h	293000	35h	434000	80h	650000	46h	810000	90h
87000	34h	167000	12h	295000	36h	435000	81h	652000	47h	811000	91h
88000	35h	168000	13h	297000	37h	436000	83h	657000	48h	812000	92h
89000	37h	169000	14h	300000	38h	437000	84h	661000	49h	814000	93h
90000	38h	170000	15h	303000	39h	438000	85h	662000	4Ah	816000	94h
91000	39h	172000	16h	305000	3Ah	439000	86h	665000	4Bh	817000	96h
93000	3Ch	173000	17h	306000	3Bh	440000	87h	667000	4Ch	818000	97h
94000	3Eh	174000	18h	307000	3Ch	441000	88h	670000	4Dh	820000	98h
95000	3Fh	175000	1Ah	310000	3Dh	442000	89h	673000	4Eh	821000	99h
96000	40h	176000	1Bh	312000	3Eh	445000	8Ah	676000	4Fh	822000	9Ah
97000	42h	178000	1Dh	315000	3Fh	446000	8Bh	677000	50h	828000	9Bh
99000	45h	179000	1Eh	318000	40h	447000	8Ch	681000	51h	829000	9Dh
100000	46h	180000	1Fh	320000	41h	448000	8Eh	683000	52h	830000	9Fh
102000	48h	181000	20h	323000	42h	449000	8Fh	686000	53h	831000	A0h
103000	4Ah	182000	21h	324000	43h	450000	90h	688000	54h	833000	A1h
105000	4Dh	183000	22h	325000	44h	452000	91h	689000	55h	835000	A2h
106000	4Eh	184000	24h	327000	45h	453000	93h	691000	56h	836000	A3h
107000	50h	185000	25h	331000	46h	454000	94h	695000	57h	837000	A4h
108000	51h	186000	26h	334000	47h	456000	96h	698000	58h	838000	A6h
110000	54h	187000	27h	337000	48h	457800	98h	703000	59h	840000	A8h
111000	56h	188000	29h	339000	49h	461000	11h	704000	5Ah	842000	A9h
112000	57h	189000	2Ah	340000	4Ah	468000	12h	705000	5Bh	845000	AAh
113000	58h	190000	2Ch	341000	4Bh	472000	13h	707000	5Ch	846000	ABh
114000	59h	191000	2Dh	343000	4Ch	473000	14h	710000	5Dh	847000	ADh
115000	5Ch	192000	2Eh	345000	4Dh	474000	15h	712000	5Eh	848000	AEh
116000	5Dh	193000	2Fh	349000	4Eh	481000	16h	717000	5Fh	852000	AFh
117000	5Fh	194000	30h	352000	4Fh	486000	17h	718000	60h	853000	B0h
119000	60h	195000	33h	353000	50h	491000	18h	721000	61h	858000	B1h
120000	64h	196000	35h	355000	51h	498000	19h	722000	62h	860000	B2h
121000	65h	198000	36h	357000	52h	499000	1Ah	723000	63h	861000	B3h
122000	66h	200000	38h	359000	53h	501000	1Bh	725000	64h	862000	B4h
123000	68h	201000	3Ch	361000	54h	506000	1Ch	727000	65h	863000	B6h
124000	69h	202000	3Dh	362000	55h	511000	1Dh	730000	66h	864000	B8h
125000	6Ch	203500	3Eh	364000	56h	516000	1Eh	732000	67h	865000	B9h
126000	6Dh	206000	0Eh	368000	57h	520000	1Fh	735000	68h	-	-

Table 52. THERMOMETER_map

Bit TM_ON must be set to logic 1.

TM_D[3:0]	TMVALUE (die temperature)	
	TM_RANGE = 0	TM_RANGE = 1
0000	60 °C	92 °C
0001	62 °C	94 °C
0010	66 °C	98 °C
0011	64 °C	96 °C
0100	74 °C	106 °C
0101	72 °C	104 °C
0110	68 °C	100 °C
0111	70 °C	102 °C
1000	90 °C	122 °C
1001	88 °C	120 °C
1010	84 °C	116 °C
1011	86 °C	118 °C
1100	76 °C	108 °C
1101	78 °C	110 °C
1110	82 °C	114 °C
1111	80 °C	112 °C

Table 53. IR_MEAS_map

$f_{RF(max)}$ (kHz)	IR_MEAS[2:0]
200	101
600	110
865	111

Table 54. CID_Target_map

$f_{RF(max)}$	CID_Target	count_limit
46000	4	1800
52200	A	1500
70100	1	4000
136800	18	
156700	18	
186250	A	
230000	A	
345000	18	
426000	E	
489500	1E	
697500	32	
842000	3A	

10. Internal circuitry

Table 55. Internal circuits

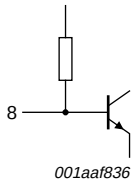
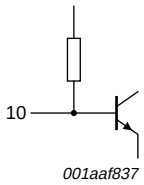
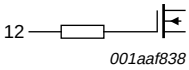
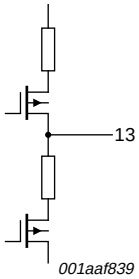
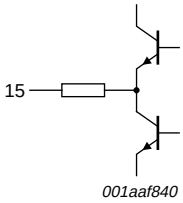
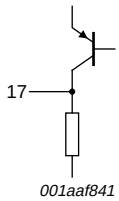
Symbol	Pin	Description[1]	Average DC voltage
FM_IN	8		0.8 V
RF_IN	10		0.8 V
CAPRFAGC	12		2.8 V
LT	13		0.85 V
STO	15		0.85 V
CAPREGVCO	17		2.8 V (Normal mode); 0 V (Standby mode)

Table 55. Internal circuits *…continued*

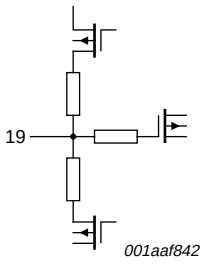
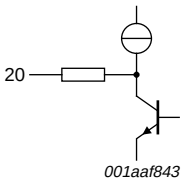
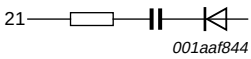
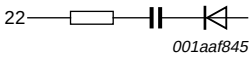
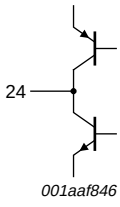
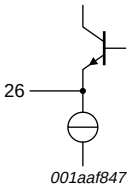
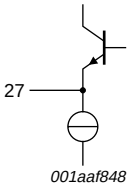
Symbol	Pin	Description[1]	Average DC voltage
MASTERSYNC	19		$0.5 \times V_{CC}$
CAPFILTVCO	20		1.6 V (Normal mode); 0 V (Standby mode)
VT_COARSE	21		$0.5 \times V_{CC}$
VT_FINE	22		$0.5 \times V_{CC}$
CP_LO	24		$0.5 \times V_{CC}$
XTALP	26		1.45 V
XTALN	27		1.45 V

Table 55. Internal circuits *…continued*

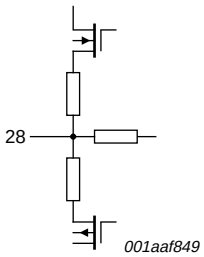
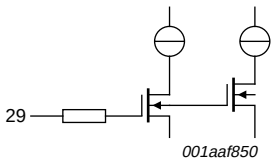
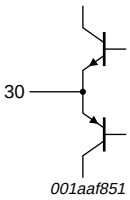
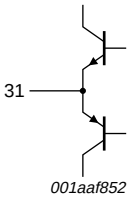
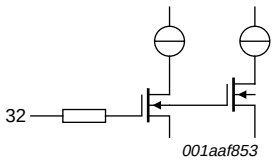
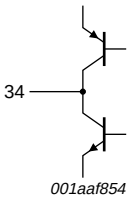
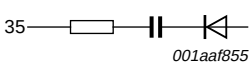
Symbol	Pin	Description[1]	Average DC voltage
FREEZE	28		3.3 V
XTOUT_MS	29		high-Z
XTOUTP	30		2.4 V
XTOUTN	31		2.4 V
AS	32		high-Z
CP_CAL	34		3.3 V (Normal mode); $0.5 \times V_{CC}$ (Calibration mode)
VT_CAL	35		3.3 V (Normal mode); $0.5 \times V_{CC}$ (Calibration mode)

Table 55. Internal circuits *…continued*

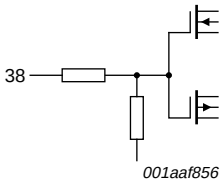
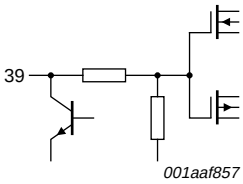
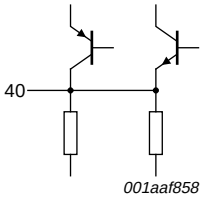
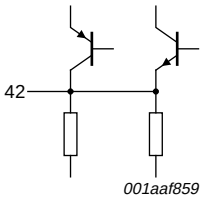
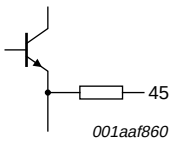
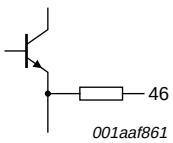
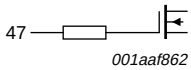
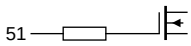
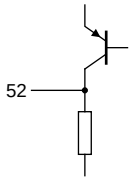
Symbol	Pin	Description[1]	Average DC voltage
SCL	38		high-Z
SDA	39		high-Z
CAPREG18	40		1.8 V (Normal mode); 2.0 V (Sleep mode)
CAPREG28	42		2.8 V (Normal mode); 2.4 V (Sleep mode)
IFOUTN	45		1.35 V
IFOUTP	46		1.35 V

Table 55. Internal circuits *...continued*

Symbol	Pin	Description[1]	Average DC voltage
V_IFAGC	47	 *001aaf862*	high-Z
VSYNC	51	 *001aaf863*	high-Z
CAPREGFILTRF	52	 *001aaf864*	2.8 V (Normal mode); 0 V (Sleep mode)

[1] ESD protection components are not shown.

11. Limiting values

Table 56. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+3.6	V
V_I	input voltage	pins SDA and SCL	–0.3	+5.5	V
		all other pins			
		V_{CC} < 3.3 V	–0.3	V_{CC} + 0.3	V
		V_{CC} > 3.3 V	–0.3	+3.6	V
T_{stg}	storage temperature		–40	+150	°C
T_j	junction temperature		-	110	°C
V_{esd}	electrostatic discharge voltage	HBM: EIA/JESD22-A114	±2000	-	V
		MM: EIA/JESD22-A115	±200	-	V

[1] The TDA18271HD withstands the latch-up specifications of JEDEC JESD78A, with the specific recommendation using coupling capacitors on pins RF_IN, LT, STO, XTOUTP and XTOUTN.

12. Thermal characteristics

Table 57. Thermal characteristics[1]

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	according to JEDEC specification	19.6	K/W

[1] The junction temperature can be obtained with the formula $T_j = T_{amb} + R_{th(j-a)} \times V_{CC} \times I_{CC}$, where $R_{th(j-a)}$ is the thermal resistance of the application. $R_{th(j-a)}$ must be such that the resulting T_j does not exceed the maximum value defined in Table 56.

13. Characteristics

All data in this section refers to Master mode operation

Table 58. Loop-through characteristics (RF input to loop-through output)

T_{amb} = 25 °C; V_{CC} = 3.3 V; for test circuit see Figure 27; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{RF(lt)}$	loop-through RF frequency	center of channel		45	-	864	MHz
VSWR	voltage standing wave ratio	loop-through output; 75 Ω nominal impedance		-	-	3	
$G_{v(lt)}$	loop-through voltage gain	75 Ω load		-	1.5	-	dB
ΔG_{lt}	loop-through gain variation	in the RF frequency range; 75 Ω load		-	3	-	dB
NF_{lt}	loop-through noise figure	Standby mode with LT, STO and crystal oscillator on		-	6.5	-	dB
CSO	composite second-order distortion		[1]	-	–60	-	dBc
CTB	composite triple beat		[1]	-	–63	-	dBc
$\alpha_{isol(bp)}$	bypass isolation	from loop-through output to RF input		-	24	-	dB
$V_{L(tun-lto)}$	leakage voltage between tuner and loop-through output	in RF TV band		-	5	-	dBµV

[1] Channel loading assumptions: 129 channels (NTSC 129 frequency plan) at 75 dBµV.

Table 59. Slave tuner output characteristics (pin STO)

T_{amb} = 25 °C; V_{CC} = 3.3 V; for test circuit see Figure 27; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{RF(STO)}$	RF frequency on pin STO		45	-	864	MHz
$Z_{o(STO)}$	output impedance on pin STO		30	35	40	Ω
$G_{v(STO)}$	voltage gain on pin STO	75 Ω source resistance on RF input; Z_i = 35 Ω (75 Ω, VSWR = 2)				
		POWER_LEVEL[6:5] = 00	-	6	-	dB
		POWER_LEVEL[6:5] = 01	-	9	-	dB
		POWER_LEVEL[6:5] = 10	-	12	-	dB
		POWER_LEVEL[6:5] = 11	-	15	-	dB

Table 60. General characteristics for TV reception (RF input to IF output)

T_{amb} = 25 °C; V_{CC} = 3.3 V; IF output level option 2 V (p-p); IF output load = 1 kΩ on each terminal; for test circuit see Figure 27; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{CC}	supply voltage		3.13	3.30	3.47	V
I_{CC}	supply current	Normal mode	180	235	290	mA
		Standby mode with LT, STO and crystal oscillator on (default at POR)	40	51	65	mA
		Standby mode with only crystal oscillator and its output on	10	15	20	mA
		Device off mode	1	2	5	mA
P	power dissipation		-	780	-	mW
T_{amb}	ambient temperature		0	-	70	°C
Input						
f_{RF}	RF frequency	center of channel	45	-	864	MHz
VSWR	voltage standing wave ratio	RF input; 75 Ω nominal impedance	-	2	-	-
NF_{tun}	tuner noise figure	maximum gain	-	5.5	-	dB
$G_{v(tun)max}$	maximum tuner voltage gain	2 V (p-p) IF output selection	-	83	-	dB
$\Delta G_{AGC(tun)}$	tuner AGC gain range		-	71	-	dB
$V_{i(max)}$	maximum input voltage	1 dB gain compression, one analog TV signal at RF input (–5 dBm)	-	103	-	dBµV
$V_{L(tun-RF)}$	leakage voltage between tuner and RF	at RF input; in RF band	-	0	-	dBµV
Output						
$V_{o(IF)dif(p-p)}$	peak-to-peak differential IF output voltage	IF_LEVEL[2:0] = 000	-	2	-	V
		IF_LEVEL[2:0] = 001	-	1.25	-	V
		IF_LEVEL[2:0] = 010	-	1	-	V
		IF_LEVEL[2:0] = 110	-	0.6	-	V
		IF_LEVEL[2:0] = 111	-	0.5	-	V
$Z_{o(IF)}$	IF output impedance	differential mode; magnitude value	-	100	-	Ω
$\Delta G_{AGC(IF)}$	IF AGC GAIN range	2 V (p-p) IF output voltage selection	-	30	-	dB
G_{tlt}	tilt gain	RF frequency range; 6/7/8 MHz channel	-	2	4	dB

Table 60. General characteristics for TV reception (RF input to IF output) *...continued*

T_{amb} = 25 °C; V_{CC} = 3.3 V; IF output level option 2 V (p-p); IF output load = 1 kΩ on each terminal; for test circuit see Figure 27; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{IF(stpb)lp}$	low-pass stop-band IF frequency	60 dB attenuation					
		6 MHz IF filter		-	14	-	MHz
		7 MHz IF filter		-	16	-	MHz
		8 MHz IF filter		-	18	-	MHz
α_{image}	image rejection			-	65	-	dB
$t_{d(grp)}$	group delay time	analog TV; difference between f1 and f2 in IF					
		Std B; f1 = 1.57 MHz; f2 = 6 MHz		-	130	-	ns
		Std G; f1 = 2.67 MHz; f2 = 7.1 MHz		-	36	-	ns
		Std M/N; f1 = 1.82 MHz; f2 = 5.4 MHz		-	92	-	ns
t_{ripple}	ripple time	digital TV; difference between f1 and f2 in digital channel					
		ATSC 6 MHz; f1 = 0.75 MHz; f2 = 5.75 MHz		-	395	-	ns
		DVB-T 6 MHz; f1 = 0.8 MHz and f2 = 5.8 MHz		-	365	-	ns
		DVB-T 7 MHz; f1 = 0.5 MHz and f2 = 6.5 MHz		-	478	-	ns
		DVB-T 8 MHz; f1 = 0.5 MHz and f2 = 7.5 MHz		-	515	-	ns
		QAM 6 MHz; f1 = 1.5 MHz and f2 = 6.5 MHz		-	155	-	ns
		QAM 8 MHz; f1 = 1.5 MHz and f2 = 8.5 MHz		-	180	-	ns
φ_n	phase noise	1 kHz and 10 kHz; see Figure 23		-	–89	-	dBc/Hz
Various							
$t_{startup(tun)}$	tuner start-up time	at power up		-	1.5	-	s
t_{set}	setting time	channel change		-	20	-	ms
S_{dig}	digital sensitivity	DVB-T (64 QAM 2/3); BER = 2.10^{-4}	[1]	-	–82	-	dBm
S_a	analog sensitivity	50 dB video SNR weighted 22 dBµV (color loss)	[2]	-	58	-	dBµV

[1] Measured with TDA10048HN channel decoder.

[2] Measured with TDA8295 IF modulator.

Table 61. General characteristics for FM radio reception (FM input to IF output)

V_{CC} = 3.3 V; T_{amb} = 25 °C; IF output load of 1 kΩ on each terminal; for test circuit see Figure 27; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{CC}	supply current	FM mode with loop-through, slave tuner output and crystal oscillator on (default at POR)	-	265	315	mA
Input						
f_{RF}	RF frequency		65	-	108	MHz
VSWR	voltage standing wave ratio	75 Ω nominal impedance	-	2	-	
Output						
f_o	output frequency	IF	-	1	-	MHz
$V_{o(p-p)}$	peak-to-peak output voltage	IF_LEVEL[2:0] = 000	-	2.0	-	V
		IF_LEVEL[2:0] = 001	-	1.25	-	V
		IF_LEVEL[2:0] = 010	-	1.0	-	V
		IF_LEVEL[2:0] = 111	-	0.5	-	V
$\alpha_{isol(bp)}$	bypass isolation	in FM band between pins RF_IN and pin FM_IN	-	32	-	dB

Table 62. Characteristics of terminals

T_{amb} = 25 °C; V_{CC} = 3.3 V; 2.2 nF on input pin V_IFAGC; for test circuit see Figure 27; unless otherwise specified.

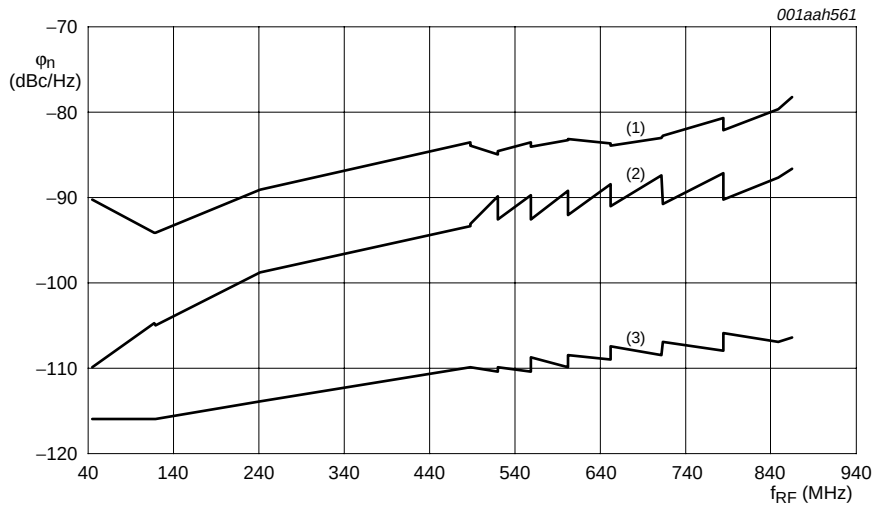
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IF AGC input: pin V_IFAGC						
V_{AGC}	AGC voltage		0	-	V_{CC}	V
Z_i	input impedance		-	high-Z	-	Ω
dG_{AGC}/dV	rate of change of AGC gain with voltage		-	30	55	dB/V
Crystal oscillator						
f_{xtal}	crystal frequency		15.99	16	16.01	MHz
Z_i	input impedance	magnitude value; master mode	-	500	-	Ω
Crystal oscillator output buffer; pins XTOUTP and XTOUTN						
R_o	output resistance	16 MHz output frequency	-	460	-	Ω
$V_{o(p-p)}$	peak-to-peak output voltage	10 kΩ//10 pF AC load	-	0.4	-	V
SR_r	slew rate of rising signal	10 kΩ//10 pF AC load	-	40	-	V/µs
SR_f	slew rate of falling signal	10 kΩ//10 pF AC load	-	40	-	V/µs

Table 62. Characteristics of terminals *...continued*

T_{amb} = 25 °C; V_{CC} = 3.3 V; 2.2 nF on input pin V_IFAGC; for test circuit see Figure 27; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C-bus[1]						
Pin SCL						
V_{IL}	LOW-level input voltage	fixed input levels	-	-	1.5	V
		V_{DD} related input levels	-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	fixed input levels	3	-	-	V
		V_{DD} related input levels	$0.7V_{DD}$	-	-	V
f_{SCL}	SCL clock frequency		-	-	400	kHz
pin SDA						
V_{OH}	HIGH-level output voltage	I_{SDA} = 3 mA (sink current)	-	-	0.4	V
V_{IL}	LOW-level input voltage	fixed input levels	-	-	1.5	V
		V_{DD} related input levels	-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	fixed input levels	3	-	-	V
		V_{DD} related input levels	$0.7V_{DD}$	-	-	V

[1] Devices that use non-standard supply voltages, which do not conform to the intended I²C-bus system levels, must relate their input levels to the supply voltage to which the pull-up resistors are connected.

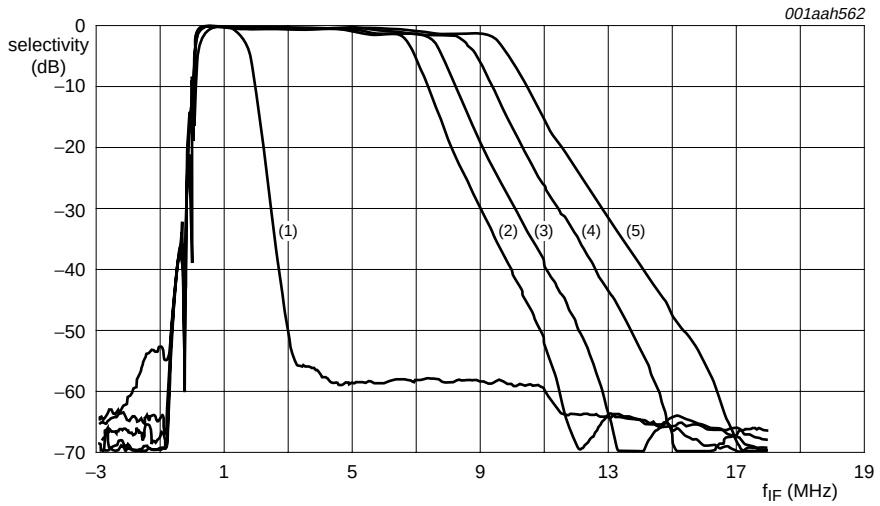


(1) Offset is 1 kHz

(2) Offset is 10 kHz

(3) Offset is 100 kHz

Fig 23. Typical phase noise curve



(1) 1.5 MHz bandwidth filter
(2) 6 MHz bandwidth filter
(3) 7 MHz bandwidth filter
(4) 8 MHz bandwidth filter
(5) 9 MHz bandwidth filter

Fig 24. Typical IF selectivity curves

14. Application information

14.1 Application examples

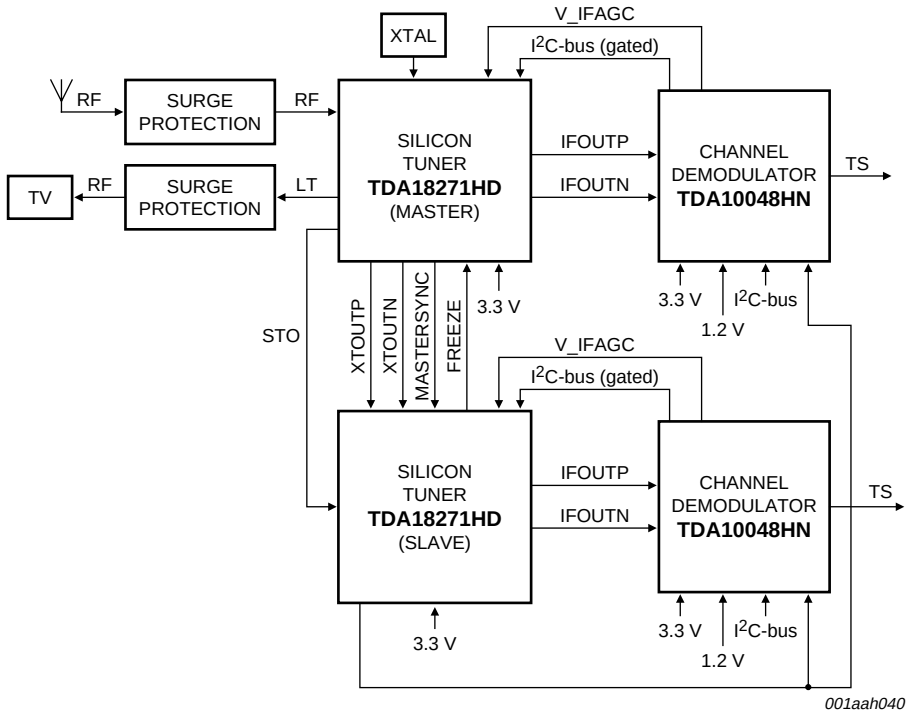


Fig 25. Example of DVB-T dual tuner reception for PCTV applications

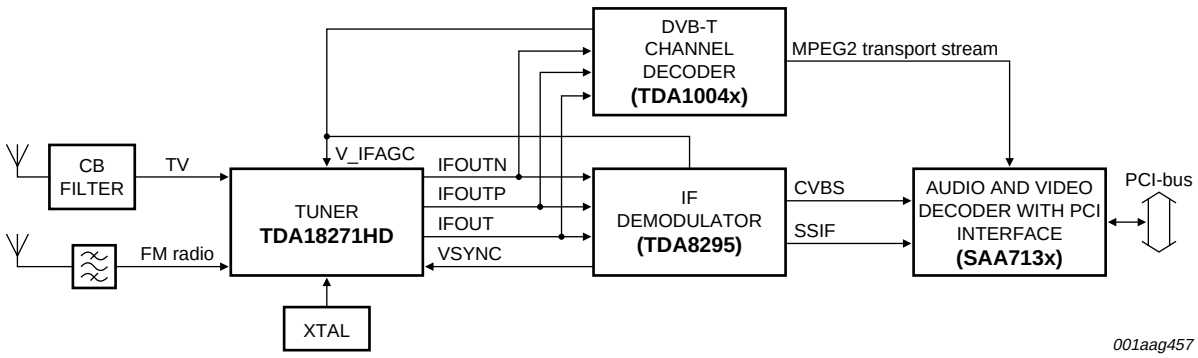


Fig 26. Example of hybrid reception for PCTV applications

14.2 Application notes

Application notes are available for the following:

- Analog and digital front end: see application note *AN605*
- Analog front end: see application note *AN602*
- Dual tuner application for PCTV: see application note *AN604*

15. Test information

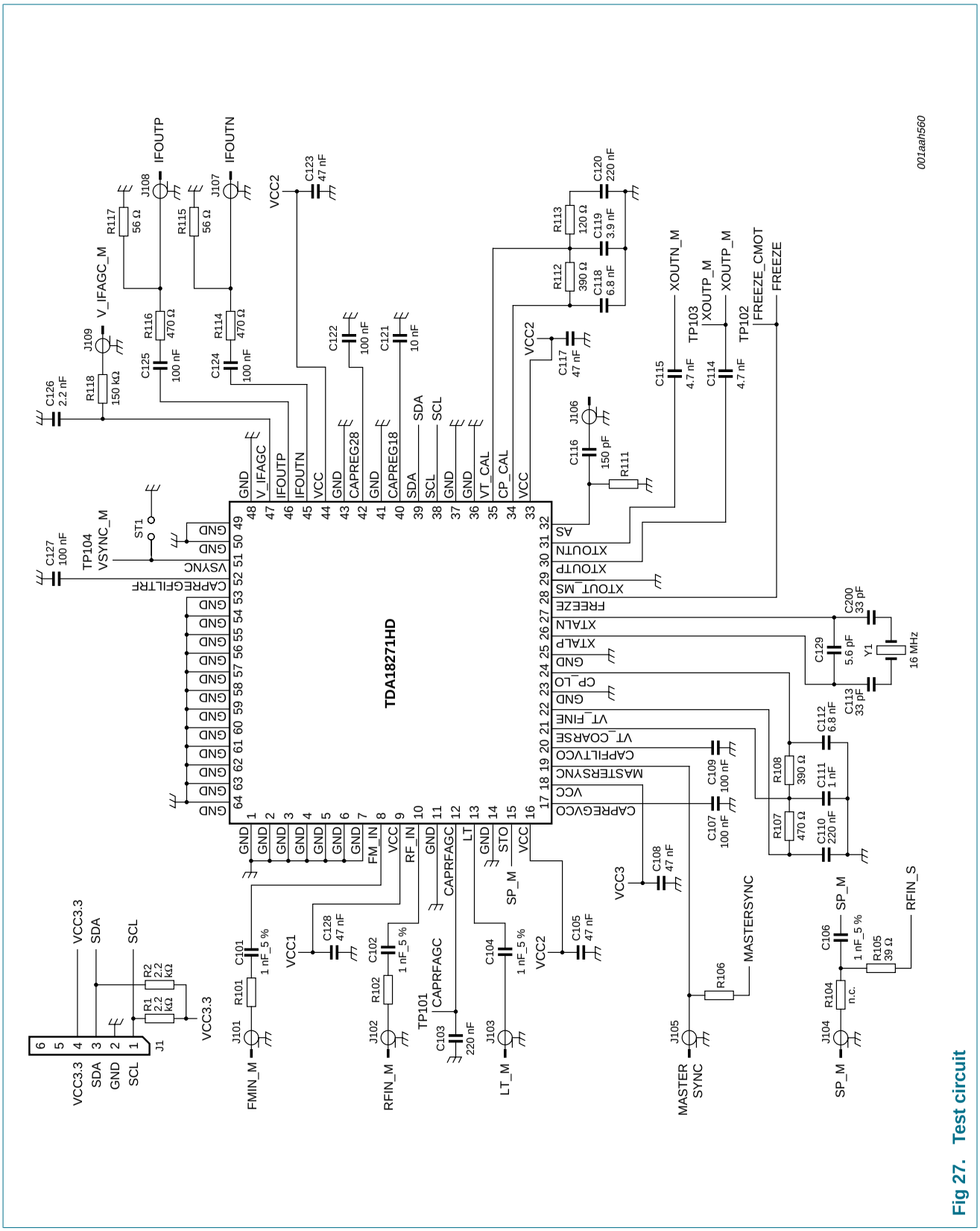
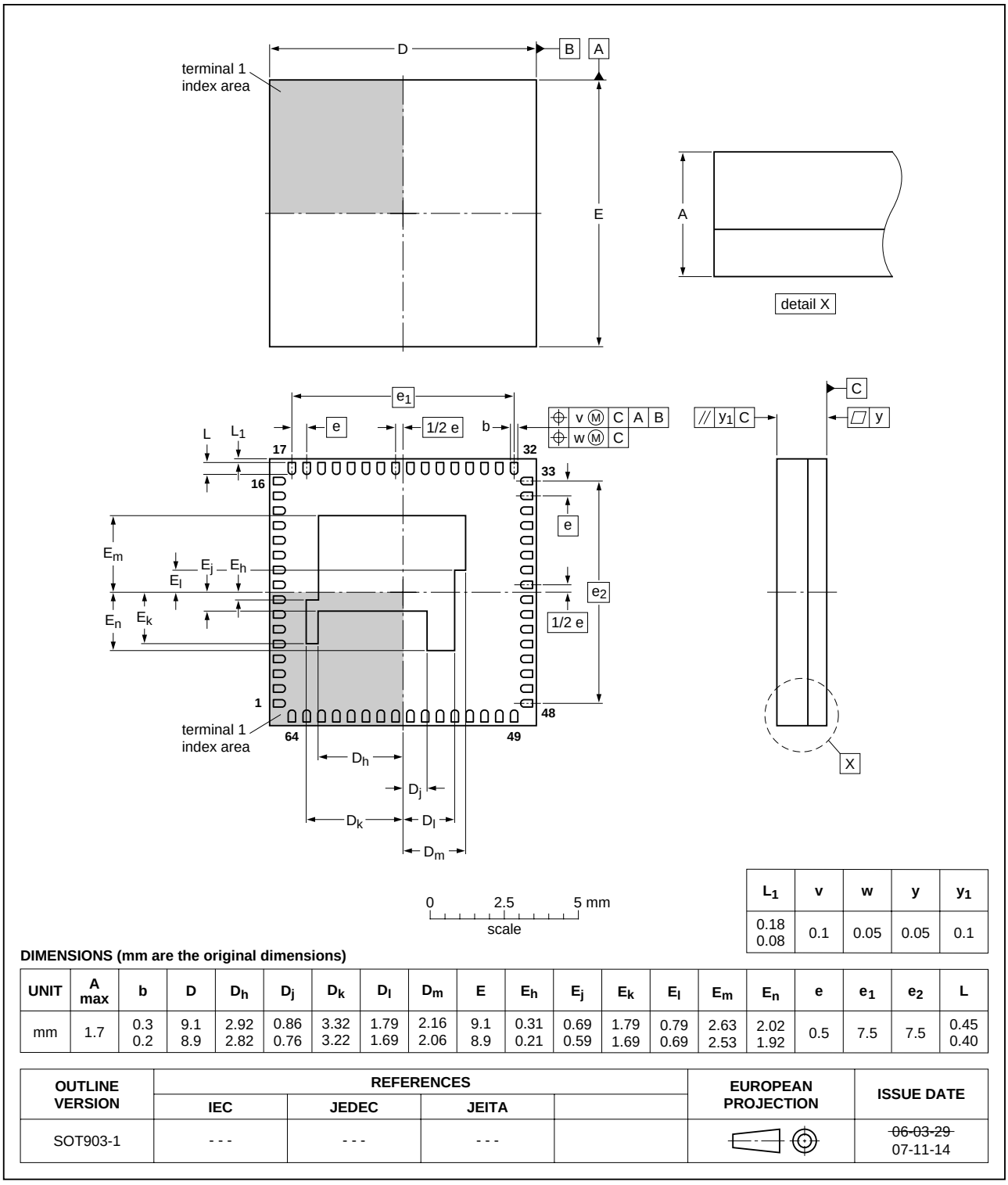


Fig 27. Test circuit

16. Package outline

HLQFN64R; plastic thermal enhanced low profile quad flat package; no leads; 64 terminals; resin based; body 9 × 9 × 1.6 mm **SOT903-1**



L_1	v	w	y	y_1
0.18 0.08	0.1	0.05	0.05	0.1

DIMENSIONS (mm are the original dimensions)

UNIT	A max	b	D	D_h	D_j	D_k	D_l	D_m	E	E_h	E_j	E_k	E_l	E_m	E_n	e	e_1	e_2	L
mm	1.7	0.3 0.2	9.1 8.9	2.92 2.82	0.86 0.76	3.32 3.22	1.79 1.69	2.16 2.06	9.1 8.9	0.31 0.21	0.69 0.59	1.79 1.69	0.79 0.69	2.63 2.53	2.02 1.92	0.5	7.5	7.5	0.45 0.40

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT903-1	- - -	- - -	- - -			~~06-03-29~~ 07-11-14

Fig 28. Package outline SOT903-1 (HLQFN64R)

17. Printed-circuit board

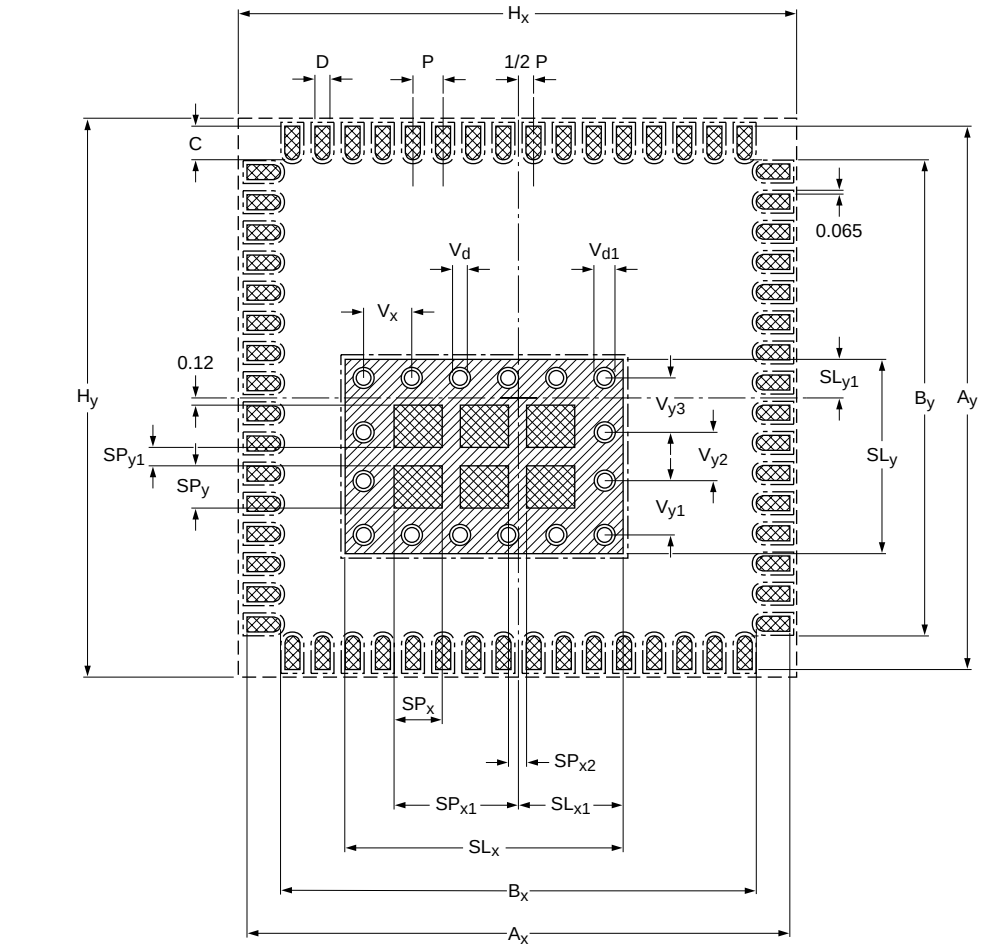
17.1 Reflow profile

See application note *AN10366*.

17.2 De-soldering recommendation

See application note *AN10366*.

17.3 Footprint layout



SP_{y1}	V_d	V_{d1}	V_x	V_{y1}	V_{y2}	V_{y3}
0.3	0.35	0.5	0.8	0.9	0.8	0.9

DIMENSIONS in mm

P	A_x	A_y	B_x	B_y	C	D	H_x	H_y	SL_x	SL_{x1}	SL_y	SL_{y1}	SP_x	SP_{x1}	SP_{x2}	SP_y
0.500	9.000	9.000	7.880	7.880	0.555	0.250	9.500	9.500	4.610	1.740	3.220	0.640	0.800	2.065	0.3	0.7

Fig 29. Footprint HLQFN64R (SOT903-1)

18. Abbreviations

Table 63. Abbreviations

Acronym	Description
AGC	Automatic Gain Control
BER	Bit Error Rate
CB	Citizens Band
CP	Charge Pump
DVB-T	Digital Video Broadcasting - Terrestrial
DVD-R	Digital Versatile Disk-Recordable
ESD	ElectroStatic Discharge
HBM	Human Body Model
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
LT	Loop-Through
MM	Machine Model
PCTV	Personal Computer TeleVision
PLL	Phase-Locked Loop
QAM	Quadrature Amplitude Modulation
RoHS	Restriction of Hazardous Substances
SAW	Surface Acoustic Wave
SNR	Signal-to-Noise Ratio
TS	Transport Stream
VCO	Voltage Controlled Oscillator

19. Revision history

Table 64. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA18271HD_3	20080911	Product data sheet	-	TDA18271HD_2
Modifications:	• Table 18: added row with value 110 • Table 60: added row with condition IF_LEVEL[2:0] = 110			
TDA18271HD_2	20080306	Product data sheet	-	TDA18271HD_1
Modifications:	• Section 9.4 “I²C-bus programming flowcharts”: updated for TDA18271HD/C2			
TDA18271HD_1	20070806	Product data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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