AGR09180EF
180 W, 865 MHz—895 MHz, N-Channel E-Mode, Lateral MOSFET

Introduction

The AGR09180EF is a high-voltage, gold-metalized, laterally diffused metal oxide semiconductor (LDMOS) RF power transistor suitable for cellular band, code-division multiple access (CDMA), global system for mobile communication (GSM), enhanced data for global evolution (EDGE), and time-division multiple access (TDMA) single and multicarrier class AB wireless base station amplifier applications. This device is manufactured on an advanced LDMOS technology, offering state-of-the-art performance, reliability, and thermal resistance. Packaged in an industry-standard CuW package capable of delivering a minimum output power of 180 W, it is ideally suited for today's RF power amplifier applications.

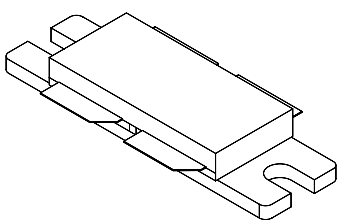


Figure 1. AGR09180EF (flanged) Package

Features

Typical performance ratings are for IS-95 CDMA, pilot, sync, paging, traffic codes 8—13:
- — Output power (P_{OUT}): 38 W.
- — Power gain: 18.25 dB.
- — Efficiency: 27%.
- — Adjacent channel power ratio (ACPR) for 30 kHz bandwidth (BW):
  - (750 kHz offset: –45 dBc)
  - (1.98 MHz offset: –60 dBc).
- — Input return loss: 10 dB.

High-reliability, gold-metalization process.

High gain, efficiency, and linearity.

Integrated ESD protection.

Si LDMOS.

Industry-standard packages.

180 W minimum output power.

Table 1. Thermal Characteristics

Parameter	Sym	Value	Unit
Thermal Resistance, Junction to Case	R_{JC}	0.35	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Sym	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, +15	Vdc
Total Dissipation at T_C = 25 °C	P_D	500	W
Derate Above 25 ˇC	—	2.86	W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, +150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating*

AGR09180EF	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1000	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

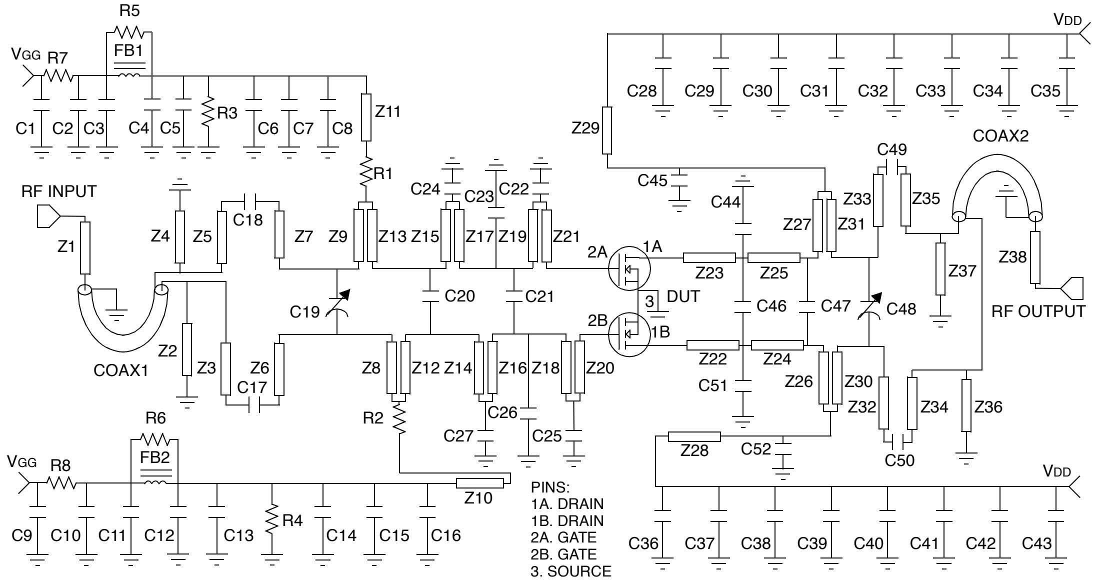
Table 4. dc Characteristics (Measurements made on ½ of device)

Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0, I_D = 400 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	6	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	200	μAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 1.0 A)	G_{FS}	—	12	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 600 μA)	$V_{GS(TH)}$	—	—	4.8	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_{DQ} = 2 x 850 mA)	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 1.0 A)	$V_{DS(ON)}$	—	0.06	—	Vdc

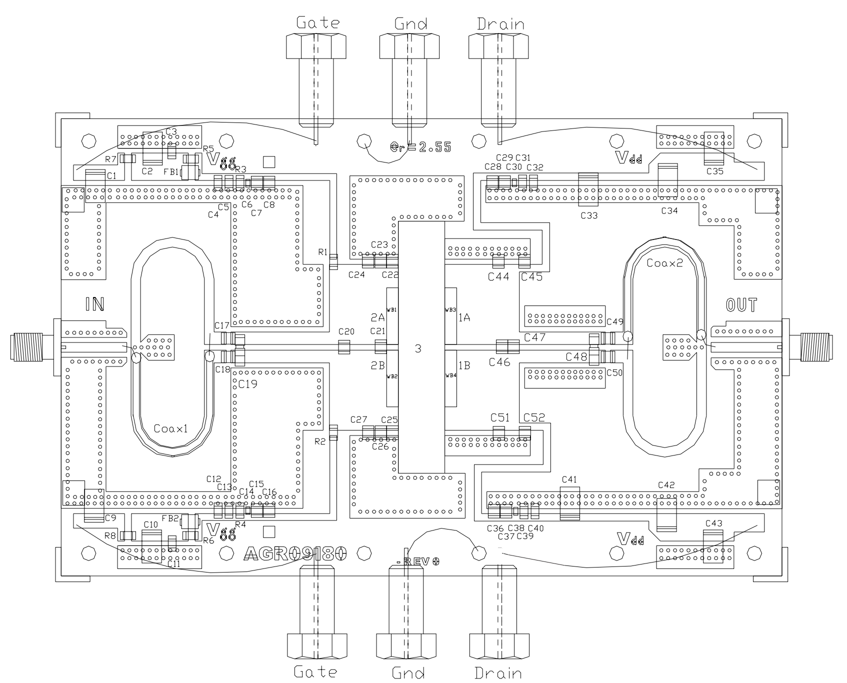
Table 5. RF Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics (Measurements made on ½ of device)					
Output Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{OSS}	—	46	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{RSS}	—	2.4	—	pF
Functional Tests (in Supplied Test Fixture) (Test frequencies (f) = 865 MHz, 880 MHz, 895 MHz)					
Linear Power Gain (V_{DS} = 28 V, P_{OUT} = 38 W, I_{DQ} = 2 x 850 mA)	G_L	17.5	18.25	—	dB
Output Power (V_{DS} = 28 V, 1 dB compression, I_{DQ} = 2 x 850 mA)	P_{1dB}	180	210	—	W
Drain Efficiency (V_{DS} = 28 V, P_{OUT} = P_{1dB}, I_{DQ} = 2 x 850 mA)		—	58	—	%
Third-order Intermodulation Distortion (100 kHz spacing, V_{DS} = 28 V, P_{OUT} = 180 WPEP, I_{DQ} = 2 x 850 mA)	IMD	—	–30	—	dBc
Input VSWR	$VSWR_I$	—	2:1	—	—
Ruggedness (V_{DS} = 28 V, P_{OUT} = 180 W, I_{DQ} = 2 x 850 mA, f = 880 MHz, VSWR = 10:1, all angles)	—	No degradation in output power.			

Test Circuit Illustrations



A. Schematic



Parts List:

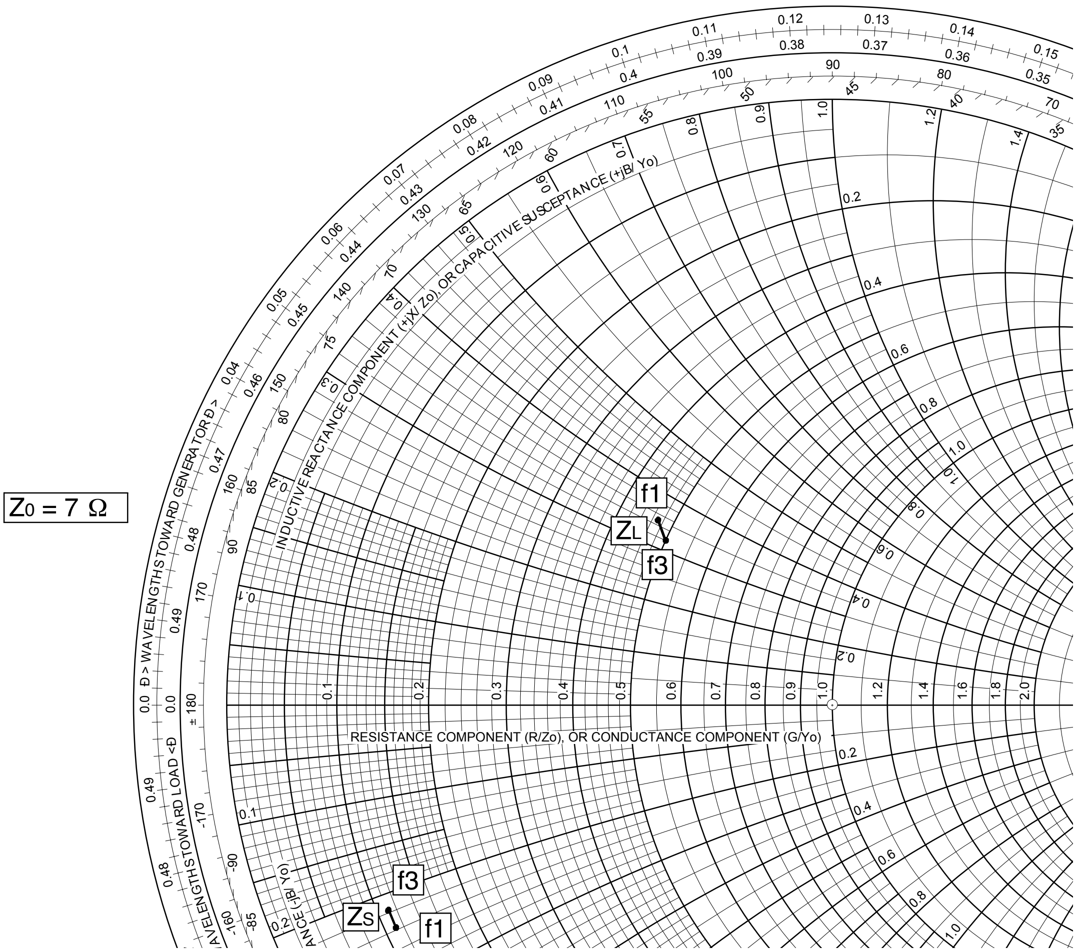
Kemet® 1206 size chip capacitor: C3, C4, C11, C12, C32, C40: 0.1 μF, C1206C104KRAC7800.
Murata® 0805: C5, C13, C31, C39: 0.01 μF, GRM40X7R103K100AL.
Sprague® tantalum chip capacitor, 35 V: C1, C2, C9, C10, C33, C34, C41, C42: 10 μF; C35, C43: 22 μF.
Johanson Giga-Trim® variable capacitors, 27291SL: C19, C48:0.8 pF—8.0 pF.
ATC® chip capacitor: C7, C15, C20, C22, C25, C29, C37, C47: 10 pF, 100B100JW; C8, C16, C17, C18, C28, C36, C49, C50: 47 pF, 100B470JW;
C21: 3.9 pF, 100B3R9BW;
C23, C26: 6.8 pF, 100B6R8BW;
C24, C27: 4.7 pF, 100B4R7BW;
C44, C51: 12 pF 100B120JW;
C45, C52: 2.0 pF, 100B2R0BW;
C46: 5.6 pF 100B5R6BW.
0603 size chip capacitors:
C6, C14, C30, C38: 220 pF.
UT-141A: Coax1, Coax2: 50 , semi-rigid coaxial cable.
Kreger® ferrite bead: FB1, FB2: 2743D19447.
Taconic® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, r = 2.55.

Microstrip line: Z1, Z38 0.572 in. x 0.084 in.; Z2, Z4, Z36, Z37 1.834 in. x 0.084 in.; Z3, Z5, Z34, Z35 0.106 in. x 0.110 in.; Z6, Z7 0.0785 in. x 0.110 in.; Z8, Z9 0.782 in. x 0.110 in.; Z10, Z11 1.182 in. x 0.060 in.; Z12, Z13 0.128 in. x 0.700 in.; Z14, Z15 0.209 in. x 0.700 in.; Z16, Z17, Z18, Z19, Z24, Z25 0.100 in. x 0.700 in.; Z20, Z21, Z26, Z27 0.050 in. x 0.700 in.; Z22, Z23 0.498 in. x 0.700 in.; Z28, Z29 1.715 in. x 0.065 in.; Z30, Z31 0.651 in. x 0.110 in.; Z32, Z33 0.100 in. x 0.110 in.
1206 size chip resistor, 0.25 W: R1, R2: 51 , RM73B2B510J; R3, R4: 56 k , RM73B2B563J; R5, R6: 12 , RM73B2B120J; R7, R8: 1.2 k , RM73B2B122J.

B. Component Layout

Figure 2. Test Circuit

Typical Performance Characteristics



MHz (f)	ZS Ω (Complex Source Impedance)	ZL Ω (Complex Optimum Load Impedance)
(f1)	0.7 – j1.46	3.32 + j2.44
(f2)	0.7 – j1.54	3.34 + j2.36
(f3)	0.7 – j1.64	3.38 + j2.28

Note: Measured drain to drain and gate to gate, respectively.

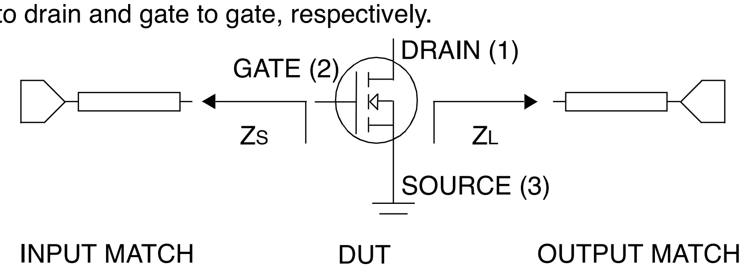
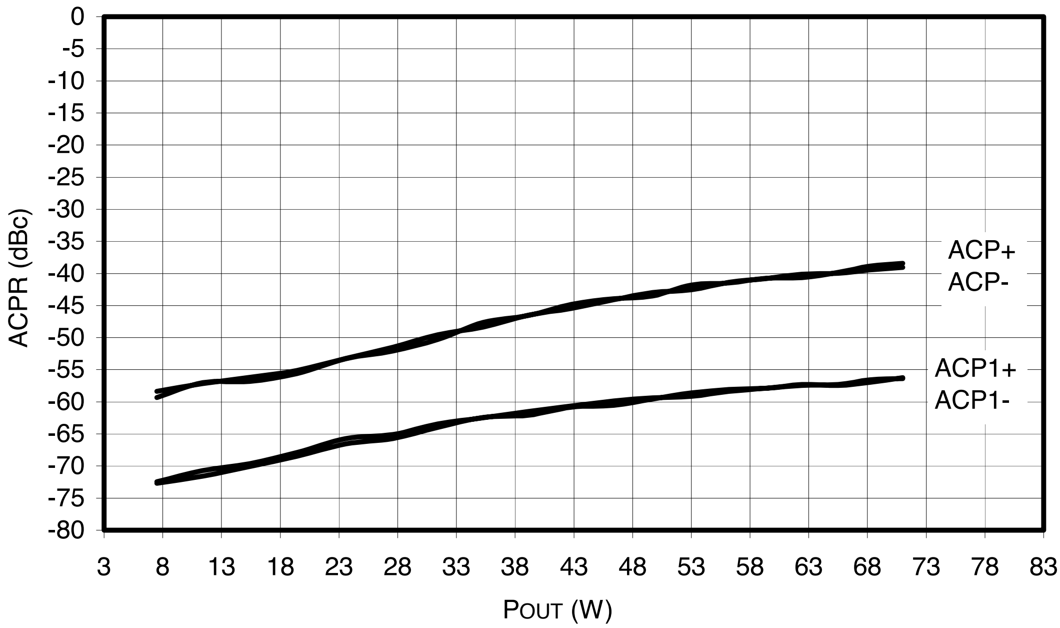


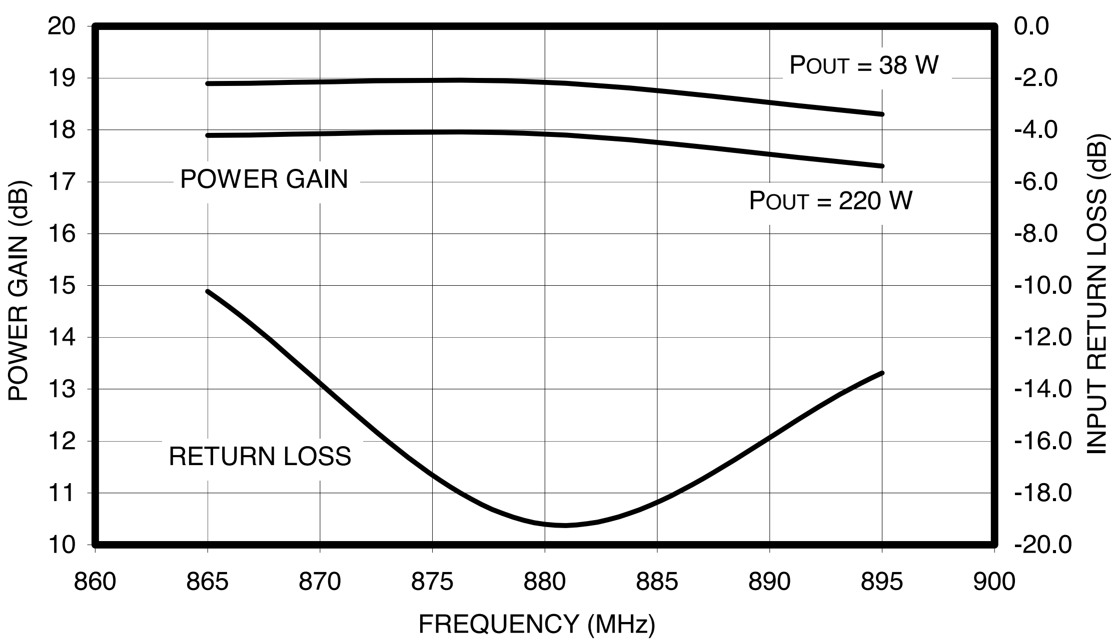
Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)



Test Conditions:
VDD = 28 Vdc, IDQ = 1700 mA, TC = 30 °C, IS-95 CDMA PILOT, PAGING, SYNC, TRAFFIC CODES 8—13,
FREQUENCY = 880 MHz, OFFSET 1 = 750 kHz, 30 kHz BW, OFFSET 2 = 1.98 MHz, 30 kHz BW.

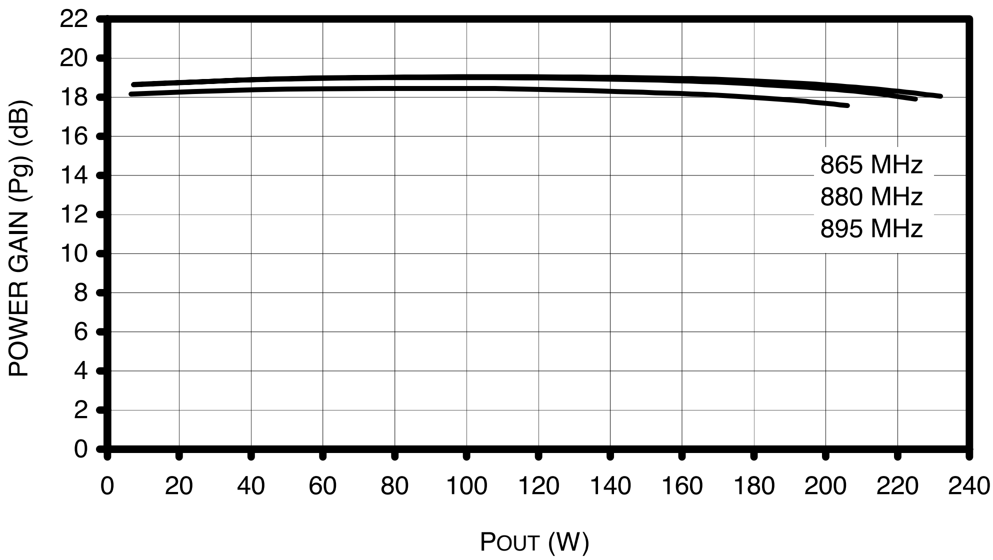
Figure 4. ACPR vs. POUT



Test Conditions:
VDD = 28 Vdc, IDQ = 1700 mA, TC = 30 °C, WAVEFORM = CW.

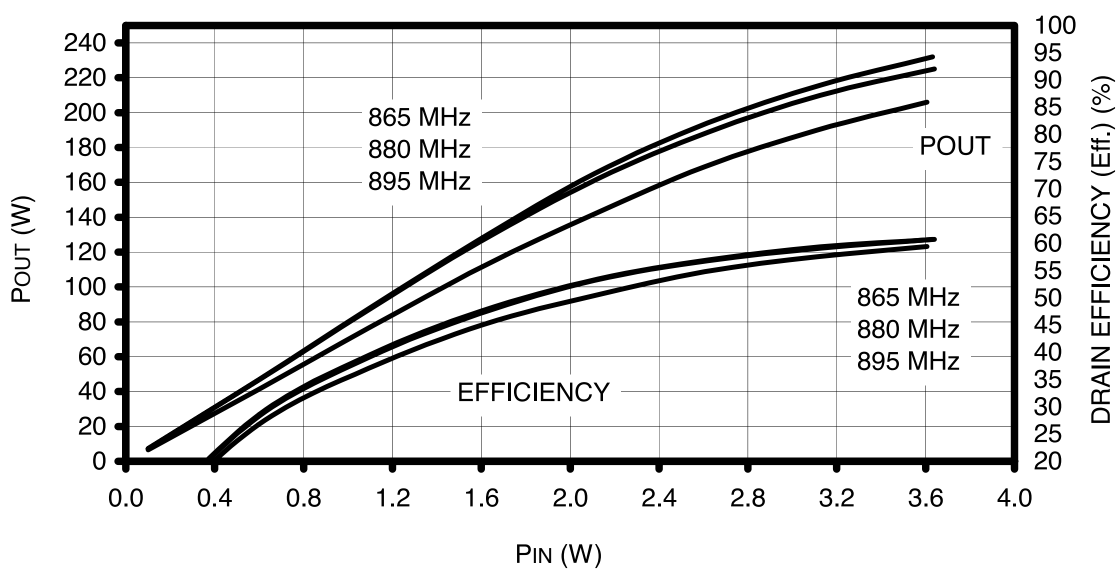
Figure 5. Power Gain and Return Loss vs. Frequency

Typical Performance Characteristics (continued)



Test Conditions:
V_{DD} = 28 Vdc, I_{DQ} = 1700 mA, T_C = 30 °C, WAVEFORM = CW.

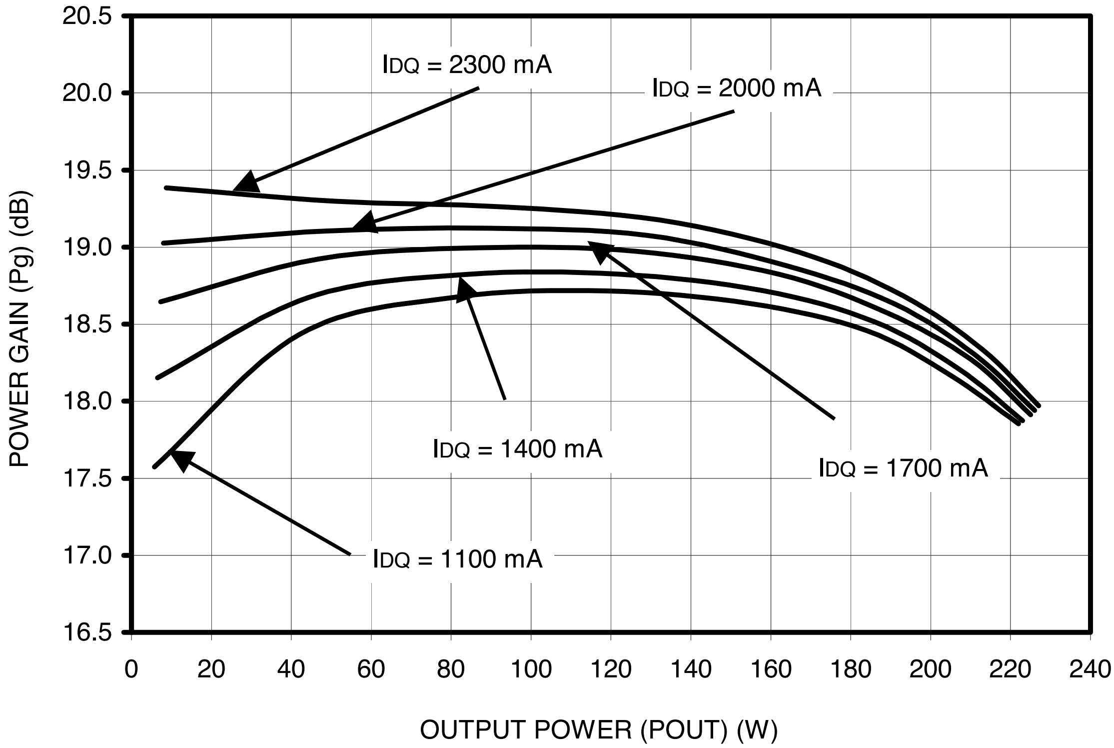
Figure 6. Power Gain vs. Power Out



Test Conditions:
V_{DD} = 28 Vdc, I_{DQ} = 1700 mA, T_C = 30 °C, WAVEFORM = CW.

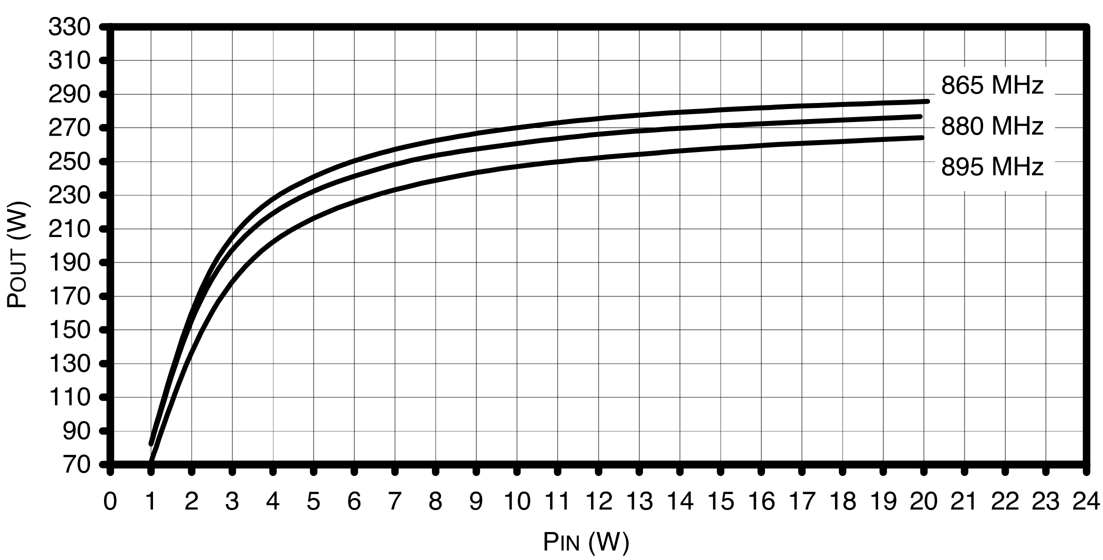
Figure 7. Power Out and Drain Efficiency vs. Input Power

Typical Performance Characteristics (continued)



Test Conditions:
V_{DD} = 28 V, FREQUENCY = 880 MHz.

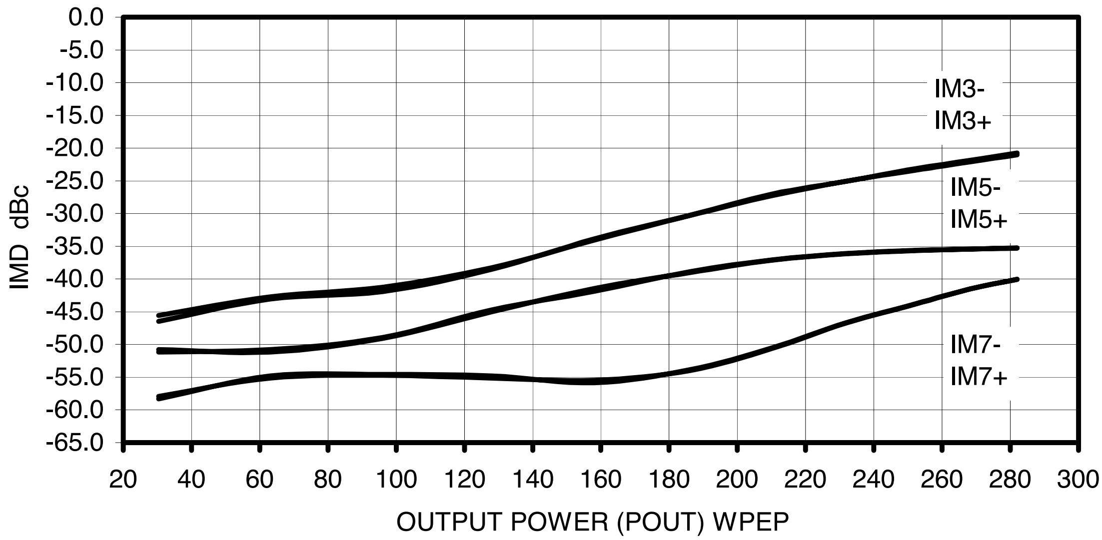
Figure 8. Power Gain vs. Power Out



Test Conditions:
V_{DD} = 28 V, I_{DQ} = 1700 mA, T_C = 30 °C.
PULSE WIDTH = 8 μs, DUTY FACTOR = 10%.

Figure 9. Power Out vs. Input Power

Typical Performance Characteristics (continued)

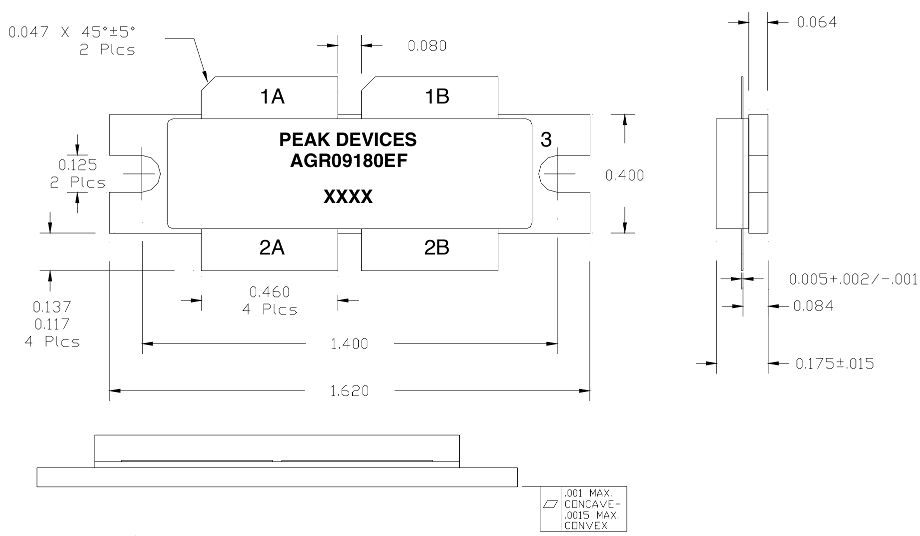


Test Conditions:
V_{DD} = 28 V, I_{DQ} = 1700 mA, T_C = 30 °C.
F1 = 880 MHz and F2 = 880.1 MHz.

Figure 10. Third-order Intermodulation Distortion vs. Power Out

Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified.



PINS:
1A. DRAIN
1B. DRAIN
2A. GATE
2B. GATE
3. SOURCE

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