

## RAD-HARD OCTAL D-TYPE FLIP FLOP WITH 3 STATE OUTPUT NON INVERTING

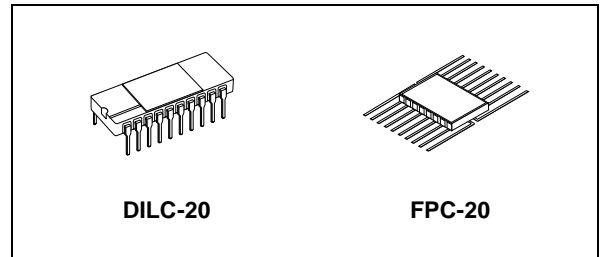
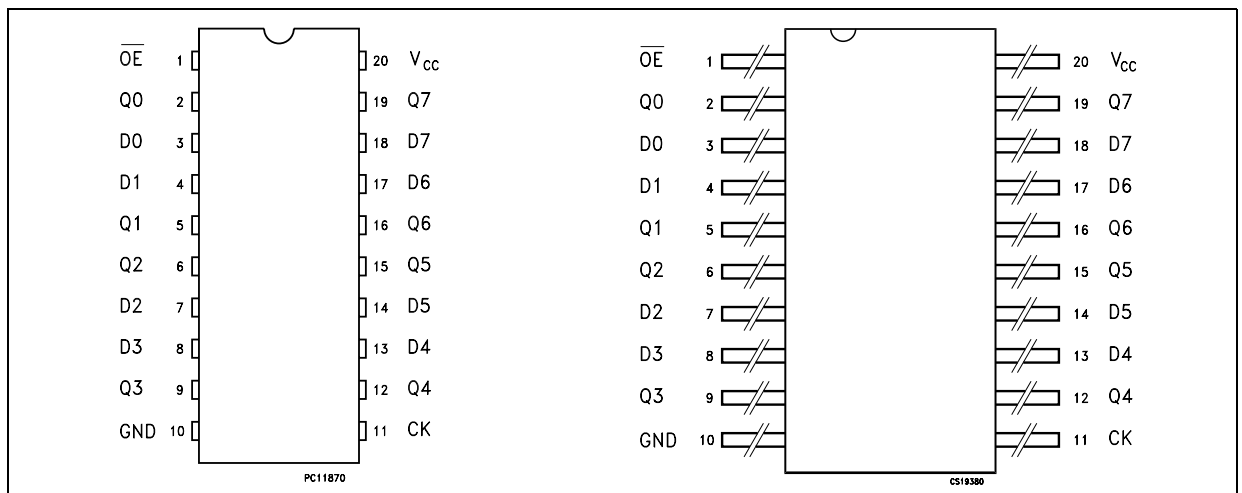
- HIGH SPEED:  
 $f_{MAX} = 90\text{MHz}$  (TYP.) at  $V_{CC} = 6\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4\mu\text{A}$ (MAX.) at  $T_A=25^\circ\text{C}$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 6\text{mA}$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:  
 $V_{CC}$  (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 374
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9203-060

### DESCRIPTION

The M54HC374 is an high speed CMOS OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate C<sup>2</sup>MOS technology.

This 8 bit D-TYPE FLIP FLOP is controlled by a clock input (CK) and an output enable input ( $\overline{OE}$ ).

### PIN CONNECTION



### ORDER CODES

PACKAGE	FM	EM
DILC	M54HC374D	M54HC374D1
FPC	M54HC374K	M54HC374K1

On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs.

While the  $\overline{OE}$  input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while  $\overline{OE}$  is high the outputs will be in a high impedance state.

The output control does not affect the internal operation of flip-flops; that is, the old data can be retained or the new data can be entered even while the outputs are off.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Figure 1: IEC Logic Symbols

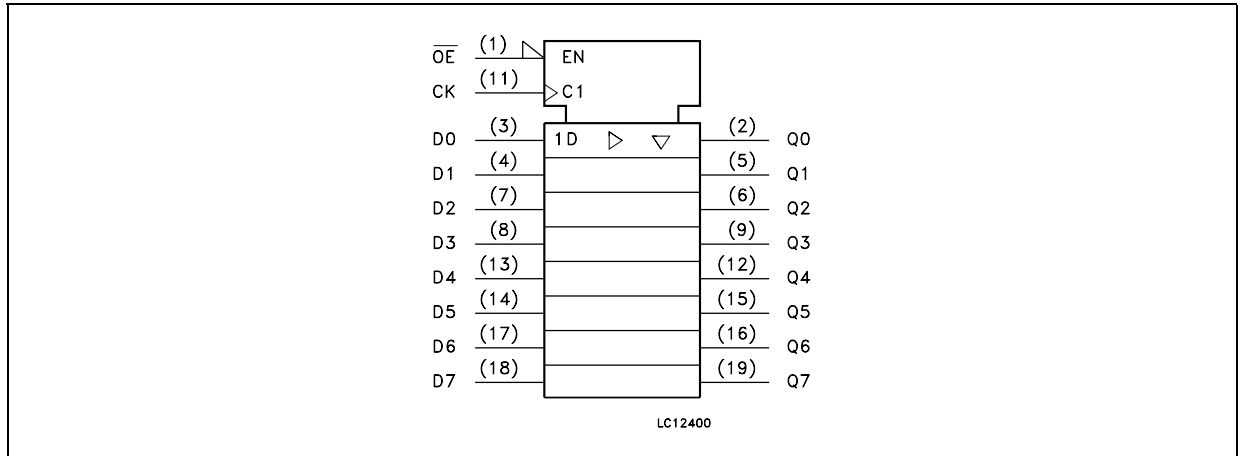


Figure 2: Input And Output Equivalent Circuit

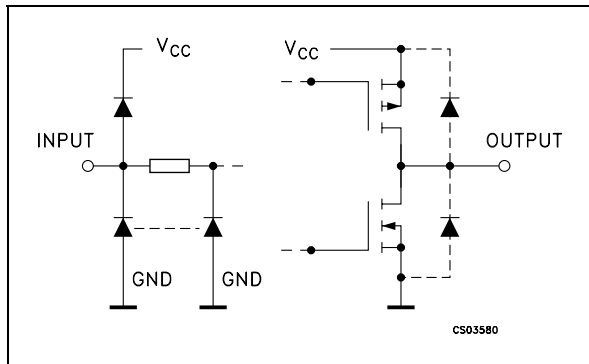


Table 1: Pin Description

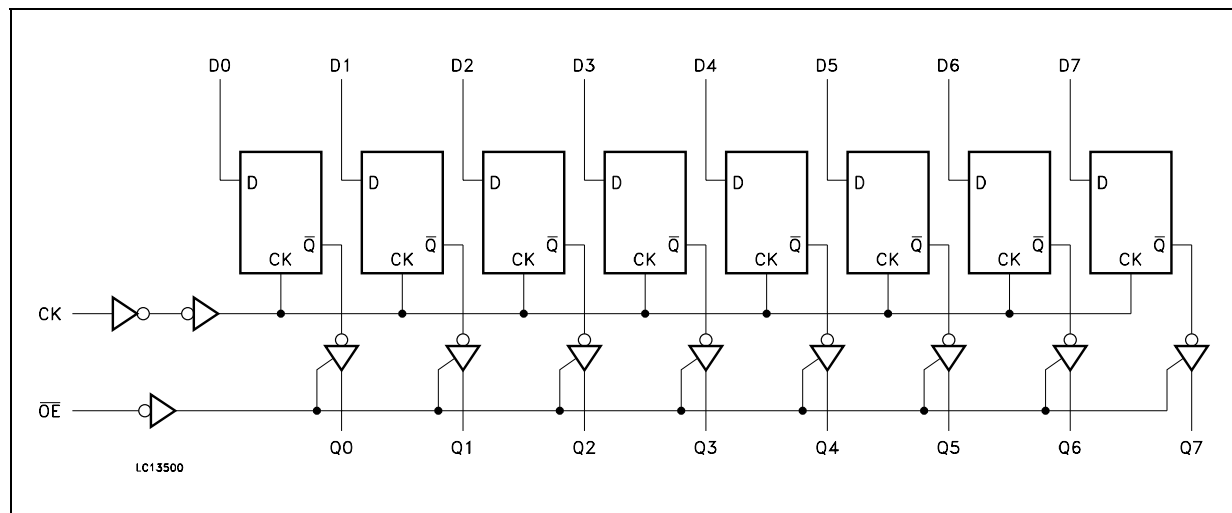
PIN N°	SYMBOL	NAME AND FUNCTION
1	OE	3 State Output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3 State Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive Supply Voltage

Table 2: Truth Table

INPUTS			OUTPUT
OE	CK	D	Q
H	X	X	Z
L		X	NO CHANGE
L		L	L
L		H	H

X: Don't Care  
Z: High Impedance

Figure 3: Logic Diagram



This logic diagram has not been used to estimate propagation delays

Table 3: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 35$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 70$	mA
$P_D$	Power Dissipation	420	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	265	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 4: Recommended Operating Conditions

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply Voltage	2 to 6	V	
$V_I$	Input Voltage	0 to $V_{CC}$	V	
$V_O$	Output Voltage	0 to $V_{CC}$	V	
$T_{op}$	Operating Temperature	-55 to 125	°C	
$t_r, t_f$	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

Table 5: DC Specifications

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V <sub>IL</sub>	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V <sub>OH</sub>	High Level Output Voltage	2.0	I <sub>O</sub> =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I <sub>O</sub> =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I <sub>O</sub> =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I <sub>O</sub> =-6.0 mA	4.18	4.31		4.13		4.10		
		6.0	I <sub>O</sub> =-7.8 mA	5.68	5.8		5.63		5.60		
V <sub>OL</sub>	Low Level Output Voltage	2.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		6.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		4.5	I <sub>O</sub> =6.0 mA		0.17	0.26		0.33		0.40	
		6.0	I <sub>O</sub> =7.8 mA		0.18	0.26		0.33		0.40	
I <sub>I</sub>	Input Leakage Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			± 0.1		± 1		± 1	μA
I <sub>OZ</sub>	High Impedance Output Leakage Current	6.0	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND			± 0.5		± 5		± 10	μA
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		80	μA

Table 6: AC Electrical Characteristics ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

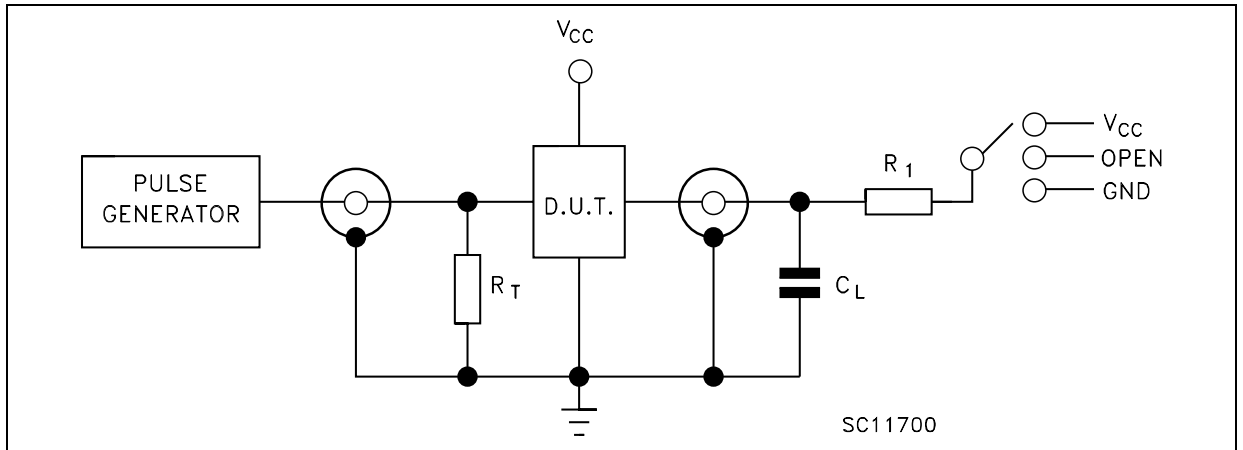
Symbol	Parameter	Test Condition			Value						Unit	
		$V_{CC}$ (V)	$C_L$ (pF)		$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{TLH}$ $t_{THL}$	Output Transition Time	2.0	50		25	60		75		90	ns	
		4.5		7	12		15		18			
		6.0		6	10		13		15			
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CLOCK - Q)	2.0	50		45	140		175		210	ns	
		4.5		15	28		35		42			
		6.0		13	24		30		36			
		2.0	150		60	190		240		285	ns	
		4.5		20	38		48		57			
		6.0		17	32		41		48			
$t_{PZL}$ $t_{PZH}$	High Impedance Output Enable Time	2.0	50	$R_L = 1\text{ K}\Omega$		39	135		170		205	ns
		4.5			13	27		34		41		
		6.0			11	23		29		35		
		2.0	150	$R_L = 1\text{ K}\Omega$		54	185		230		280	ns
		4.5			18	37		46		56		
		6.0			15	31		39		48		
$t_{PLZ}$ $t_{PHZ}$	High Impedance Output Disable Time	2.0	50	$R_L = 1\text{ K}\Omega$		30	125		155		190	ns
		4.5			14	25		31		38		
		6.0			13	21		26		32		
$f_{MAX}$	Maximum Clock Frequency	2.0	50		6.2	18		5		4.2	MHz	
		4.5		31	75		25		21			
		6.0		37	90		30		25			
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0	50		15	75		95		110	ns	
		4.5		6	15		19		22			
		6.0		6	13		16		19			
$t_s$	Minimum Set-up Time	2.0	50		25	75		95		110	ns	
		4.5		6	15		19		22			
		6.0		4	13		16		19			
$t_h$	Minimum Hold Time	2.0	50			0		0		0	ns	
		4.5			0		0		0			
		6.0			0		0		0			

Table 7: Capacitive Characteristics

Symbol	Parameter	Test Condition			Value						Unit	
		$V_{CC}$ (V)			$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$C_{IN}$	Input Capacitance					5	10		10		10	pF
$C_{OUT}$	Output Capacitance					10						pF
$C_{PD}$	Power Dissipation Capacitance (note 1)					47						pF

1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation:  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$  (per Flip Flop) and the  $C_{PD}$  when n pcs of Flip Flop operate, can be gained by the following equation:  $C_{PD(TOTAL)} = 30 + 17 \times n$  (pF)

Figure 4: Test Circuit



TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$V_{CC}$
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 50\text{pF}/150\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_1 = 1\text{K}\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

Figure 5: Waveform - CK To Qn Propagation Delays, CK Fmax, Dn To CK Setup And Hold Times (f=1MHz; 50% duty cycle)

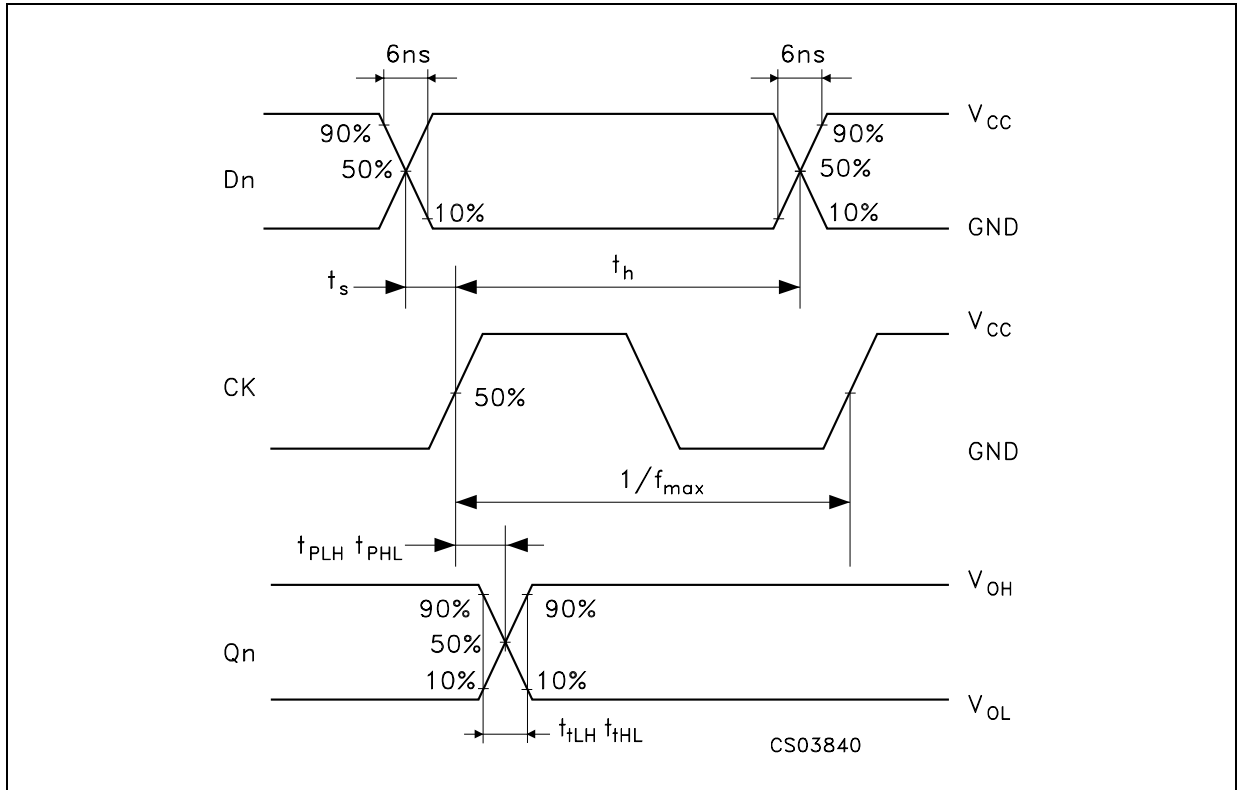
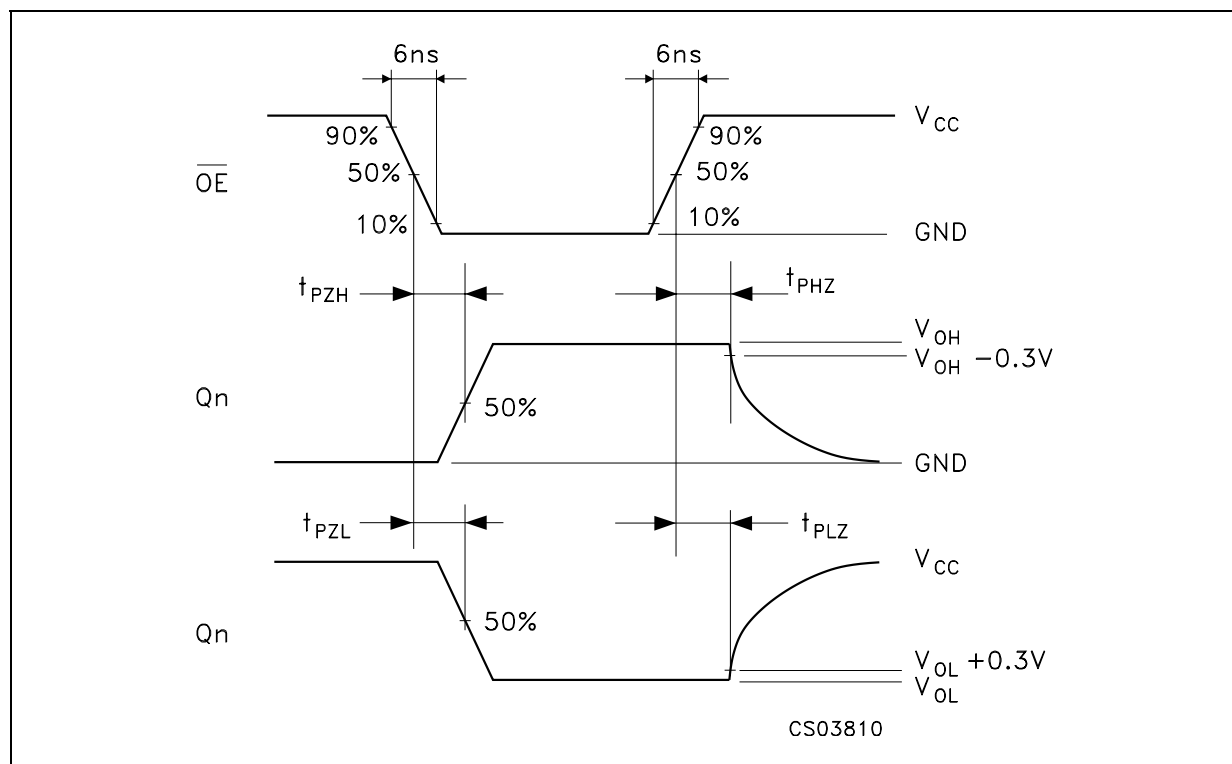
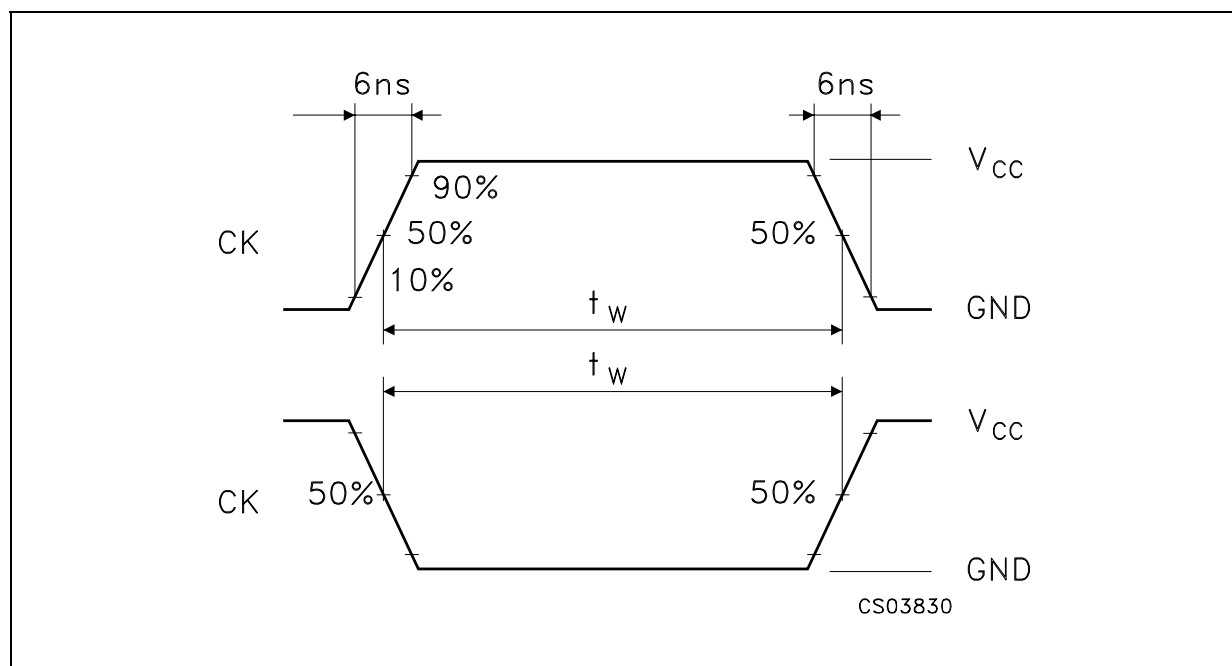
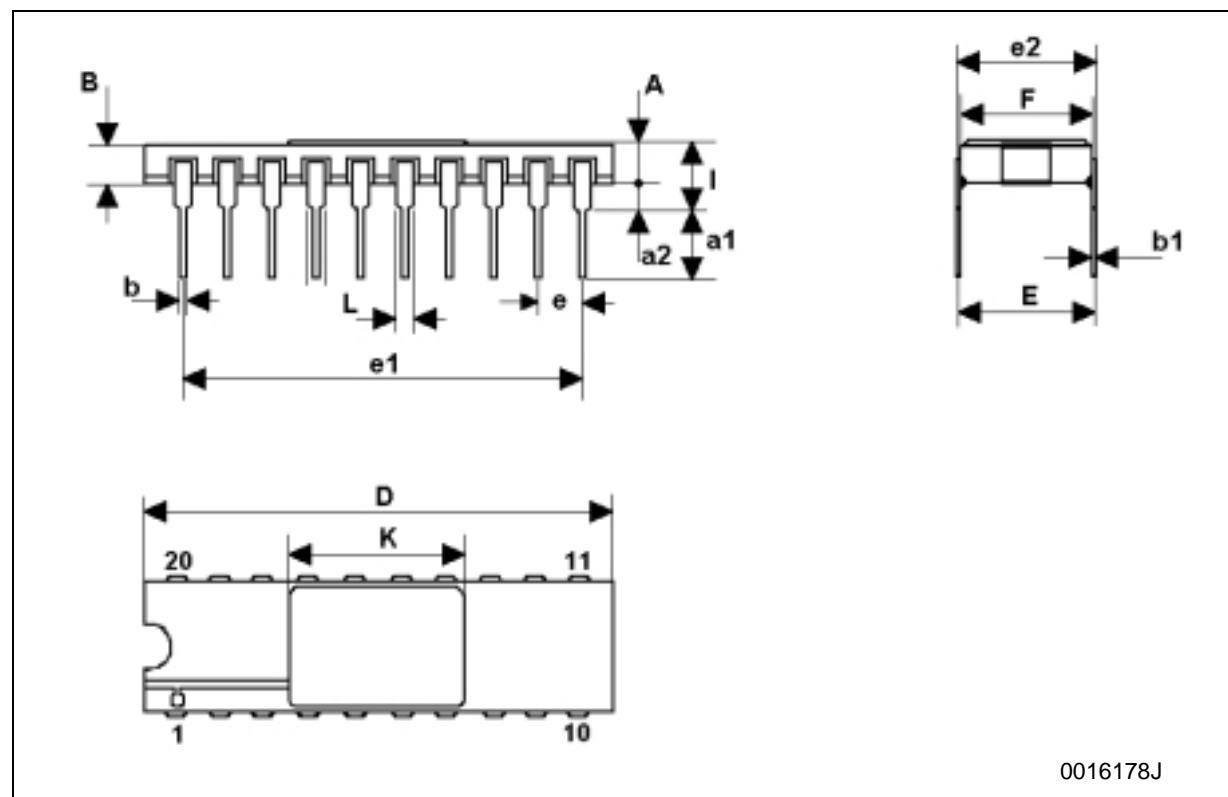


Figure 6: Waveform - Output Enable And Disable Times ( $f=1\text{MHz}$ ; 50% duty cycle)Figure 7: Waveform - Minimum Pulse Width (CK) ( $f=1\text{MHz}$ ; 50% duty cycle)

## DILC-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.71	0.083		0.107
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.93	2.03	2.23	0.076	0.080	0.088
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	25.14	25.40	25.65	0.990	1.000	1.010
e	7.36	7.62	7.87	0.290	0.300	0.310
e1		2.54			0.100	
e2	22.73	22.86	22.99	0.895	0.900	0.905
e3	7.62	7.87	8.12	0.300	0.310	0.320
F	7.29	7.49	7.70	0.287	0.295	0.303
I			3.86			0.152
K	11.30		11.56	0.445		0.455
L	1.14	1.27	1.40	0.045	0.050	0.055

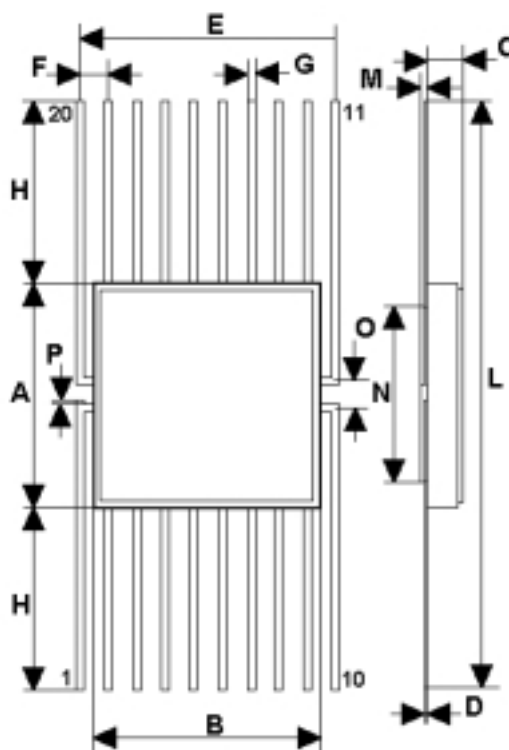


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## FPC-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	9.98	10.16	10.34	0.393	0.400	0.407
B	9.98	10.16	10.34	0.393	0.400	0.407
C	1.45	1.61	1.78	0.57	0.63	0.070
D	0.10	0.127	0.18	0.004	0.005	0.007
E	11.30	11.43	11.56	0.445	0.450	0.455
F		1.27			0.050	
G	0.38	0.43	0.48	0.015	0.017	0.019
H	7.24		8.16	0.285		0.320
L	24.46		26.67	0.960		1.050
M	0.45	0.50	0.55	0.018	0.020	0.022
N		7.87			0.310	
O	1.14	1.27	1.40	0.045	0.050	0.055
P	0.10	0.18	0.25	0.004	0.007	0.010



016032F

**Table 8: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
10-May-2004	1	First Release

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