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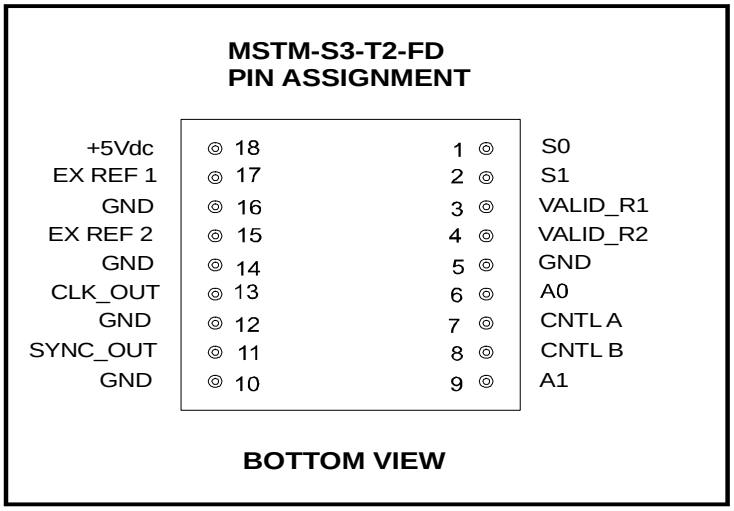
Stratum 3 Simplified Control Timing Modules (MSTM-S3-T2-FD)

DESCRIPTION

The Connor-Winfield Stratum 3 Miniature Simplified Control Timing Module acts as a complete system clock module for general Stratum 3 timing applications. The MSTM is designed for external control functions. Full external control input allows for selections and monitoring of any of four possible operating states: 1) Holdover, 2) External Reference #1, 3) External Reference #2, and 4) Free Run. The table below illustrates the control signal inputs and corresponding operational states:

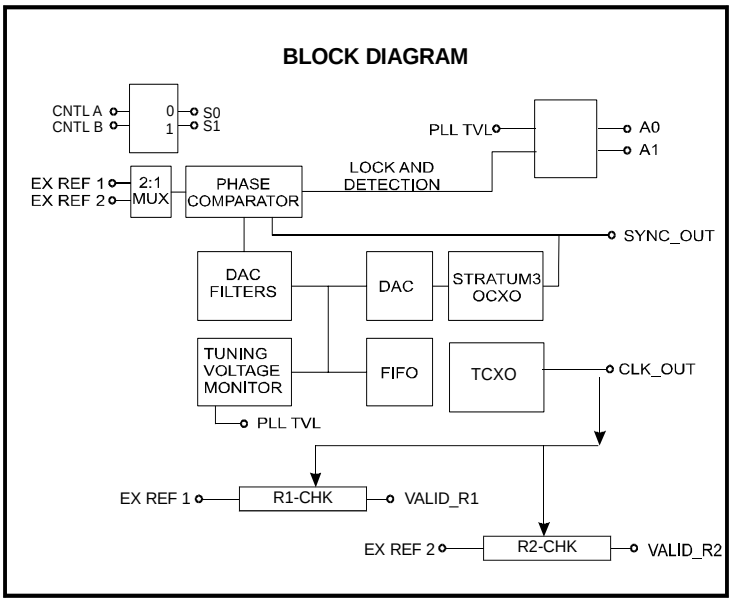
In the absence of External Control Inputs (A,B), the MSTM enters the Free Run mode and signals an External Alarm. The MSTM will enter other operating modes upon application of a proper control signal. Mode 1 operation (A=1, B=0) results in an output signal that is phase locked to the External Reference Input #1. Mode 2 operation (A=0, B=1) results in an output signal that is phase locked to External Reference Input #2. Holdover mode operation (A=1, B=1) results in an output signal at or near the frequency as determined by the latest (last) locked-signal input values and the holdover performance of the MSTM.

Fig. 1.0



The primary feature of this model is the Reference Frequency Detector (RFD). This is an independent circuit that monitors both reference inputs simultaneously to determine that a signal is present and its frequency is within a valid range. A logical one on the outputs VALID_R1 and VALID_R2 indicates that the signals applied to EX_REF1 and EX_REF2 respectively have been detected and have a frequency that is within at least +/- 4.6 ppm of nominal. A range of +/-4.6 ppm is guaranteed for the life of the module. The actual range is somewhat more than twice that to account for normal drift and aging that will occur. When, for example, the reference applied to EX_REF1 disappears, VALID_R1 will go to a logical zero within 500 microseconds. When the signal returns at a frequency within +/- 4.6 ppm of nominal the VALID_R1 output will return to a logical one after a 4-second delay. The delay is a validation period that requires the output of the frequency detector to remain stable for 4 seconds before confirming the status of the reference applied. This eliminates the incessant toggling of the frequency detector that occurs when the reference frequency is at the threshold frequency of the detector

Fig. 2.0



The function of the RFD is not related to the operational alarms, LOL and TVL, which monitor the operation of the PLL relative to the selected active reference. In fact the operational alarms function only at the extreme edge of the PLL operating range. This means that it is quite possible for the active reference to drift out of range of the Reference Frequency Detector and still remain well within the capture range of the PLL and not activate the operational alarms. If the other reference was still marked valid by the RFD it might make sense to switch to the better reference before the selected reference drifts completely out of range.

Alarm signals are generated at the Alarm Output during Holdover and Free Run operation. Alarm Signals are also generated by loss-of-lock, loss of Reference, and by a Tune-Limit indication from the PLL. A Tune-Limit alarm signal indicates that the OCXO tuning voltage is approaching within 10% the limits of its lock capability and that the External Reference Input may be erroneous. A high level indicates an alarm condition. Real-time indication of the operational mode is available from outputs S0 and S1, which are determined from internal mode registers.

Control loop filters effectively attenuate any reference jitter and smooth out phase transients.

Table 1.0

CONTROL INPUT		OPERATIONAL MODE		Alarm Outputs		State Outputs	
A	B			**A0**	**A1**	**S0**	**S1**
0	0	Free Run (Default)		0	0	0	0
1	0	External	Normal	0	0	1	0
		Reference #1	TVL	1	0	1	0
		(While locked	LOR	0	1	1	0
		to Valid Ref)	LOL (>17 ppm)	1	1	1	0
0	1	External	Normal	0	0	0	1
		Reference #2	TVL	1	0	0	1
		(While locked	LOR	0	1	0	1
		to Valid Ref)	LOL (>17 ppm)	1	1	0	1
1	1	Holdover		0	0	1	1

Table 2.0

Condition	**Qualification Outputs**	
	VALID_R1	**VALID_R2**
Ref 1 Within ± 4.6ppm	1	X
Ref 1 > ± 4.6 ppm	0	X
Ref 1 (No Signal)	0	X
Ref 2 Within ± 4.6 ppm	X	1
Ref 2 > ± 4.6 ppm	X	0
Ref 2 (No Signal)	X	0

Fig. 3.0

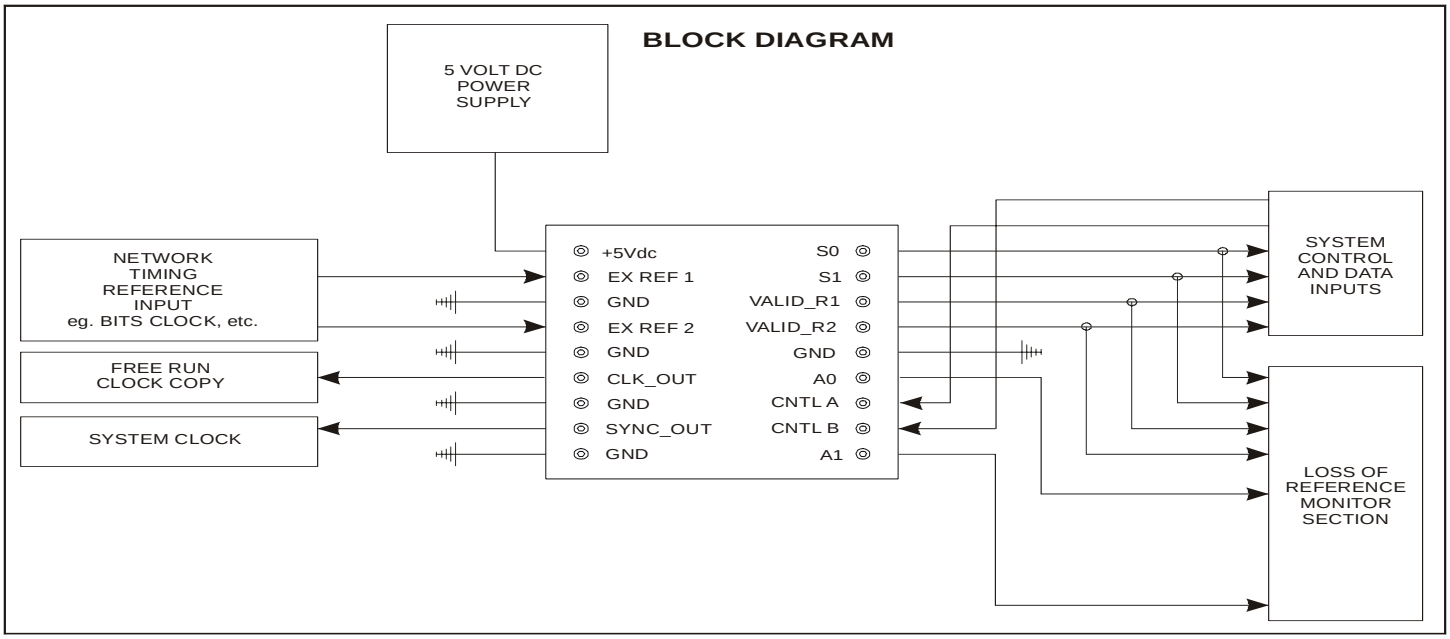


Fig. 4.0

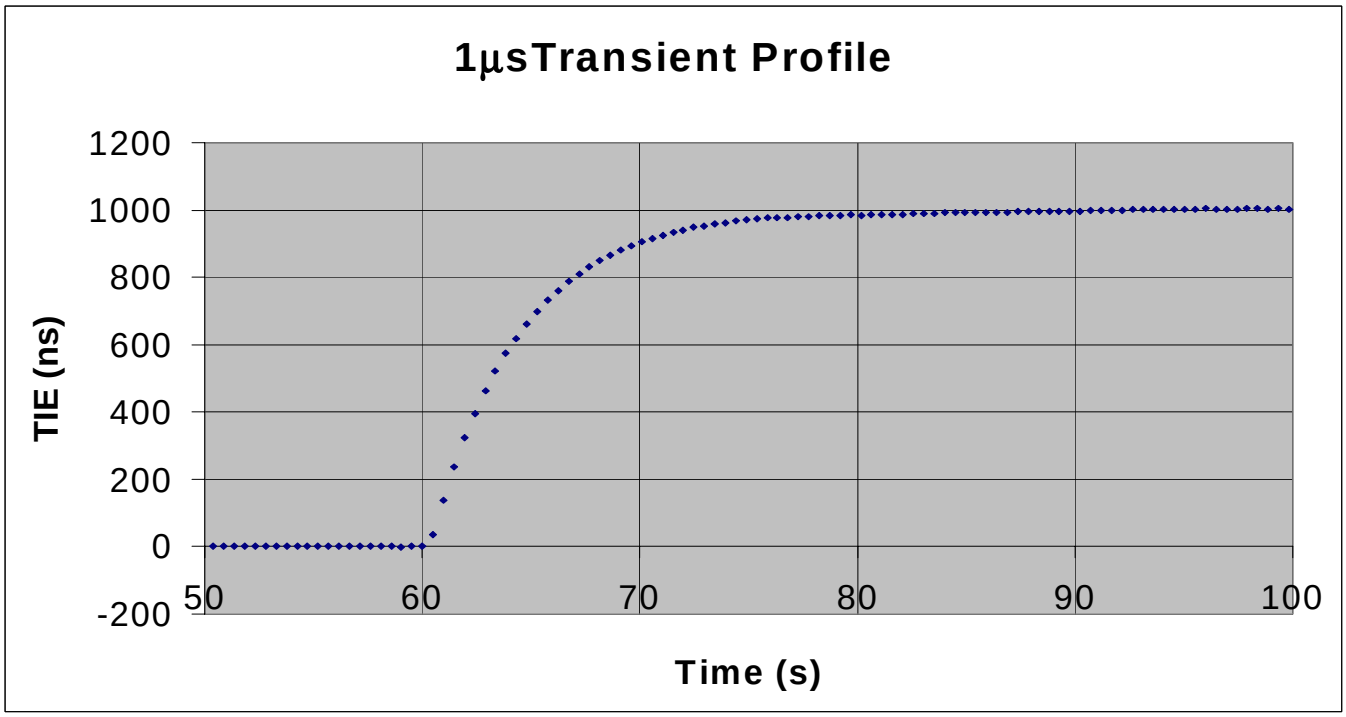


Fig 5.0

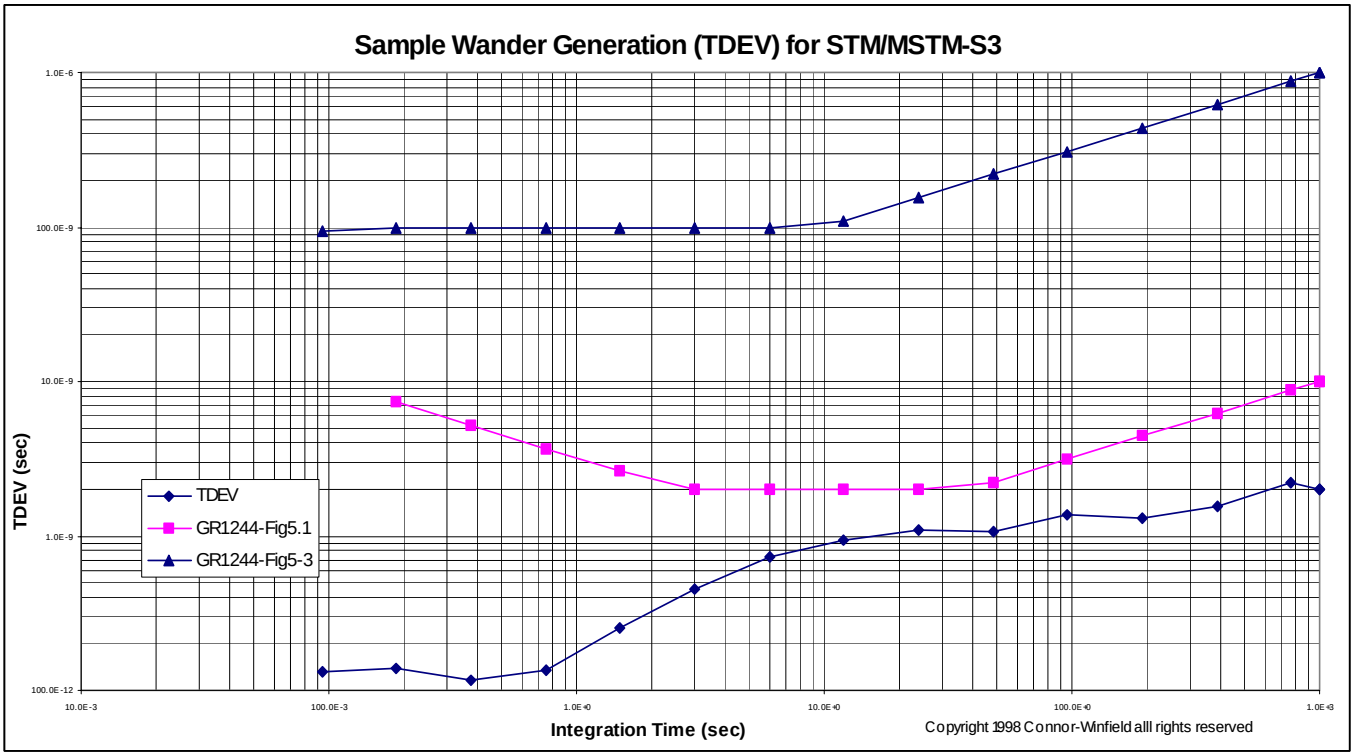


Fig. 6.0

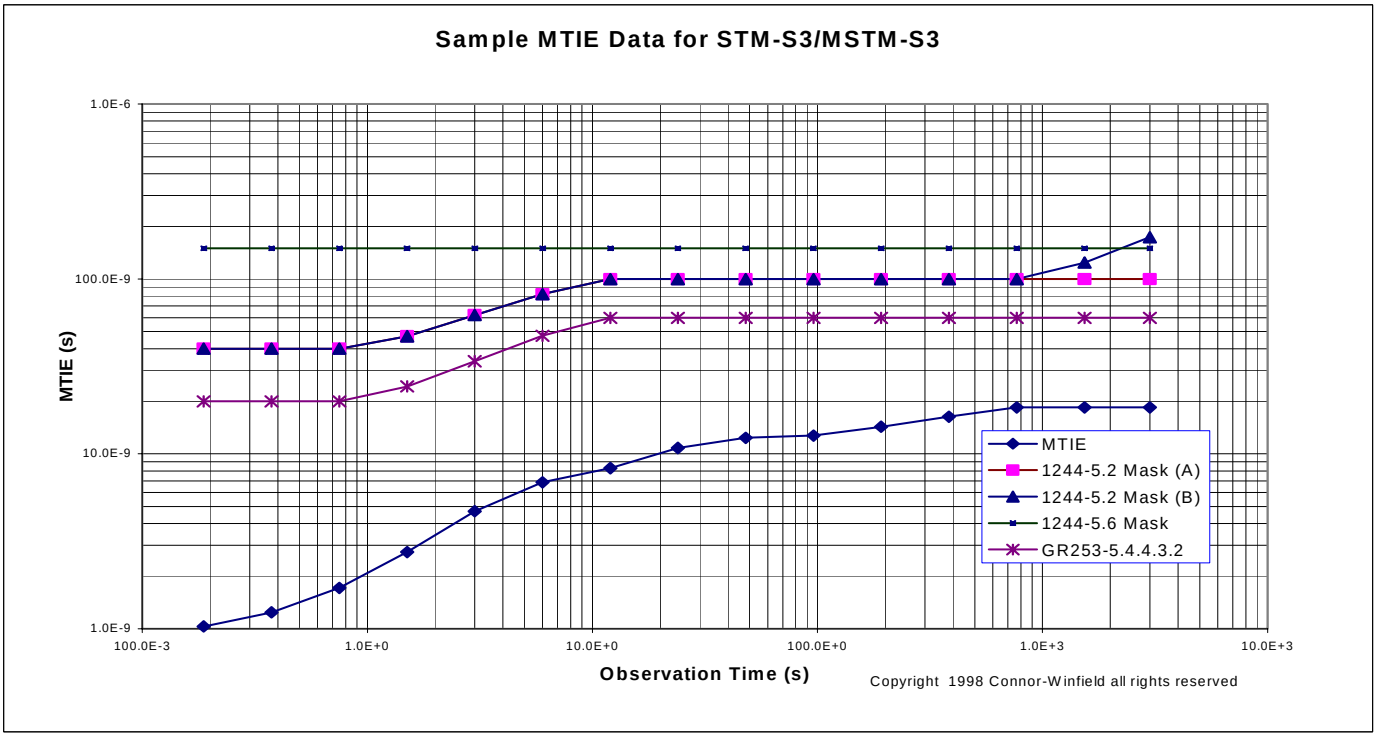


Fig. 7.0

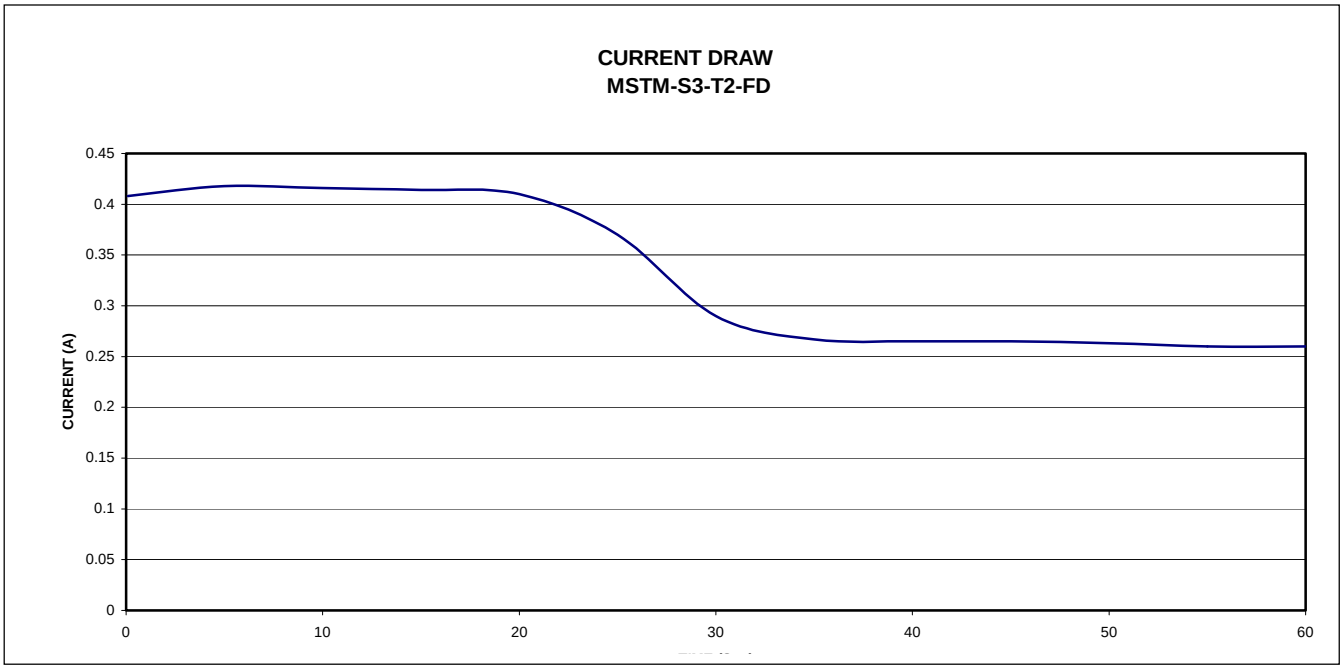


Table 3.0

VALID REFERENCE THRESHOLDS

	MINIMUM	NOMINAL	MAXIMUM
VALID_R1	±4.6 ppm	±9.2 ppm	±13.8 ppm
VALID_R2	±4.6 ppm	±9.2 ppm	±13.8 ppm

Table 4.0

FREQUENCY DETECTOR RANGE OVER LIFETIME USE

DETECTOR FREQUENCY OFFSET	VALID_R1/R2 RANGE	UNITS
0	±9.2	ppm
+4.6	+13.8 -4.6	ppm
-4.6	+4.6 -13.8	ppm

Table 5.0

	<-4.6 ppm	VALID REFERENCE	>4.6 ppm	NO REFERENCE
VALID_R1	0	1	0	0
VALID_R2	0	1	0	0

Fig. 8

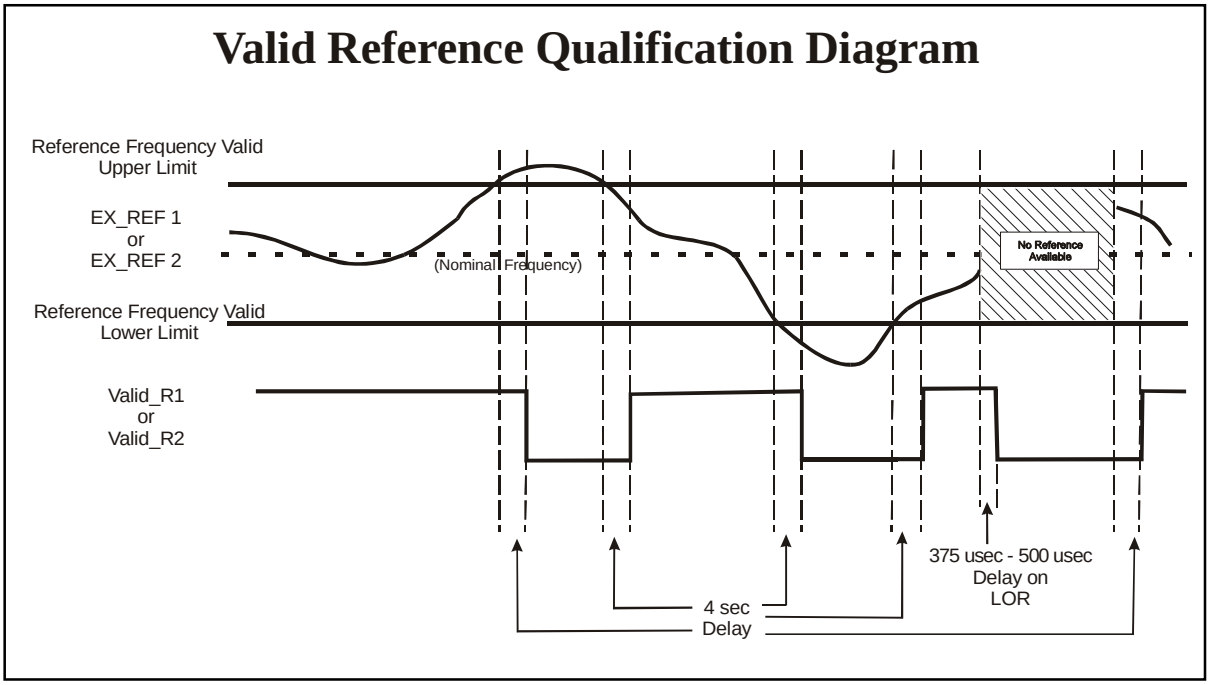


TABLE 6.0 ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTES
V_{CC}	Power supply voltage (Vcc to GND)	-0.5	5.0	+7.0	Volts	1.0
V_{IN}	Input voltage with respect to ground	-0.5		V_{cc}+.05	Volts	1.0
T_{STG}	Storage temperature	-65.0		+150.0	Deg. C	1.0

TABLE 7.0 INPUT AND OUTPUT CHARACTERISTICS

SYMBOL	PARAMETER	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTES
V_{IH}	High level input voltage (TLL Compatible)	2.0		V_{CC}	V	
V_{IL}	Low level input voltage (TLL Compatible)	0		0.8	V	
T_{IN}	Input signal transition time			250	nS	
C_{IN}	Input capacitance			15	pF	
V_{OH}	High level output voltage @ IOH=-8.0 mA, VCC minimum	2.4			V	
V_{OL}	Low level output voltage @ IOH=8.0 mA, VCC maximum			0.4	V	
T_{HL}	Clock out transition time high-to-low, no load		4.0		nS	
T_{LH}	Clock out transition time low-to-high, no load		4.0		nS	
T_{RIP}	Input 8 KHz reference signal positive pulse width	30			nS	
T_{RIN}	Input 8 KHz reference signal negative pulse width	30			nS	
T_{OP}	Standard Operating Temperature	0		70	Deg. C	

TABLE 8.0 SPECIFICATIONS

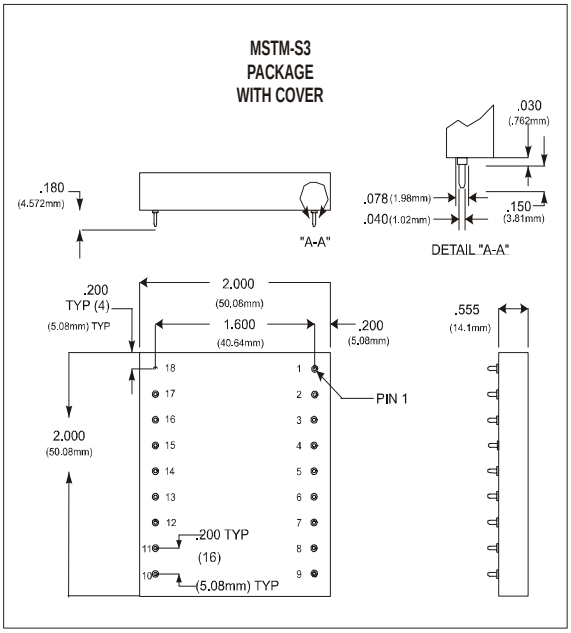
PARAMETER		NOTES
Frequency Range (SYNC_OUT)	19.44 MHz	2.0
Frequency Range (CLK_OUT)	19.44 MHz	
Supply Current	See Fig. 7.0	
Timing Reference Inputs	8 KHz	3.0
Jitter and Phase Tolerance	Ref-GR-1244-CORE 4.2-4.4	
Wander Generation	Ref-GR-1244-CORE 5.3	
Free-Run Accuracy	±4.6 ppm	
Holdover Stability	±0.37 ppm	4.0
Initial Offset	0.05 ppm	
Temperature	0.28 ppm	
Drift	0.04 ppm	
Holdover History	30 seconds	
Pull-in/ Hold-in Range	±4.6 ppm Minimum	5.0
Lock Time	<100 secs	
Correction Period	125 µS	
TVL Alarm	Reference is nearing operational limit	6.0

PIN DESCRIPTIONS

Table 9.0

MSTM-S3 PIN #	PIN NAME	PIN DESCRIPTION
1	**S0**	State Output Bit 0
2	**S1**	State Output Bit 1
3	**VALID_R1**	Reference #1 Validation
4	**VALID_R2**	Reference #2 Validation
5	**Gnd**	Ground
6	**A0**	Alarm Bit 0
7	**CNTL A**	Mode control input.
8	**CNTL B**	Mode control input.
9	**A1**	Alarm Bit 1
10	**Gnd**	Ground
11	**SYNC_OUT**	Synchronized output.
12	**Gnd**	Ground
13	**CLK_OUT**	Non-synchronized ±4.6 ppm Output
14	**Gnd**	Ground
15	**EX REF 2**	External Reference #2 Input. (8KHz)
16	**Gnd**	Ground
17	**EX REF 1**	Input. External Reference #1 Input. (8KHz)
18	**+5 Vdc**	+5 Volt DC Supply

Fig 8.0



NOTES FOR TABLES 1-7

NOTES:

1.0 Operation of this device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

2.0 Consult factory for other frequencies.

3.0 REF-GR1244-CORE 3.2.1 R3-1.

4.0 Holdover stability is the cumulative fractional frequency offset containing Initial Offset, Temperature, and Drift components as described by Bellcore GR-1244-CORE 5.2

5.0 Pull-in range is the minimum frequency deviation on the reference inputs to the timing module that can be overcome to pull itself into synchronization with the reference.

6.0 See Table 1.0 for conditions of S0 and S1 outputs

DATA SHEET REVISION HISTORY

REVISION	REVISION DATE	NOTE
A00	2/21/01	Advance Information Release
A01	5/3/01	Added Table 3.0 and Fig. 8
A02	10/24/01	Corrected Table 1.0