



N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, c}	Q _g (Typ.)
40	0.0021 at V _{GS} = 10 V	110	240 nC
	0.0024 at V _{GS} = 4.5 V	110	

FEATURES

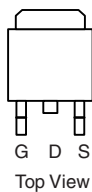
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested

RoHS
COMPLIANT

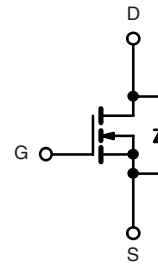
APPLICATIONS

- Synchronous Rectification
- Power Supplies

TO-263



Top View



N-Channel MOSFET

Ordering Information: SUM110N04-2m1P-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	40	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 175 °C)	I _D	T _C = 25 °C	110 ^{a, c}
		T _C = 70 °C	110 ^c
		T _A = 25 °C	29 ^b
		T _A = 70 °C	23 ^b
Pulsed Drain Current	I _{DM}	250	A
Avalanche Current Pulse	I _{AS}	80	
Single Pulse Avalanche Energy	E _{AS}	320	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	110 ^{a, c}
		T _A = 25 °C	2.6 ^b
Maximum Power Dissipation	P _D	T _C = 25 °C	312 ^a
		T _C = 70 °C	200
		T _A = 25 °C	3.13 ^b
		T _A = 70 °C	2.0 ^b
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^b	R _{thJA}	32	40	°C/W
Maximum Junction-to-Case	R _{thJC}	0.33	0.4	

Notes:

a. Based on T_C = 25 °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. Calculated based on maximum junction temperature. Package limitation current is 110 A.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		41		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.2		2.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	120			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		0.0017	0.0021	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		0.002	0.0024	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		180		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		18800		pF
Output Capacitance	C_{oss}			1550		
Reverse Transfer Capacitance	C_{rss}			850		
Total Gate Charge	Q_g	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		240	360	nC
Gate-Source Charge	Q_{GS}			40		
Gate-Drain Charge	Q_{GD}			22		
Gate Resistance	R_g	$f = 1\text{ MHz}$		0.85	1.3	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 1.0\text{ }\Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		20	30	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			77	115	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 1.0\text{ }\Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		102	155	
Rise Time	t_r			62	95	
Turn-Off Delay Time	$t_{d(off)}$			180	270	
Fall Time	t_f			60	90	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			110	A
Pulse Diode Forward Current ^a	I_{SM}				200	
Body Diode Voltage	V_{SD}	$I_S = 20\text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		50	75	ns
Body Diode Reverse Recovery Charge	Q_{rr}			70	105	nC
Reverse Recovery Fall Time	t_a			30		ns
Reverse Recovery Rise Time	t_b			20		

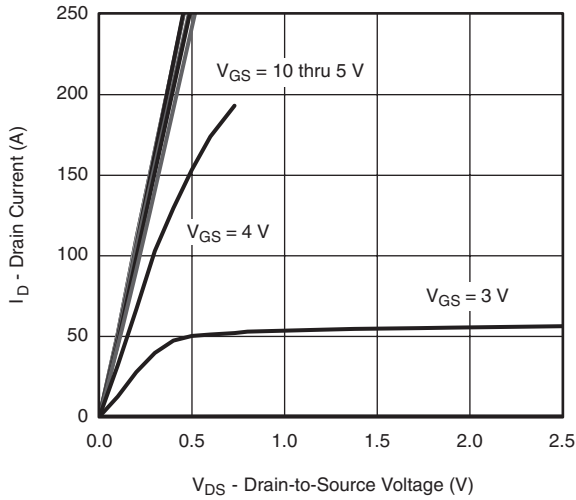
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

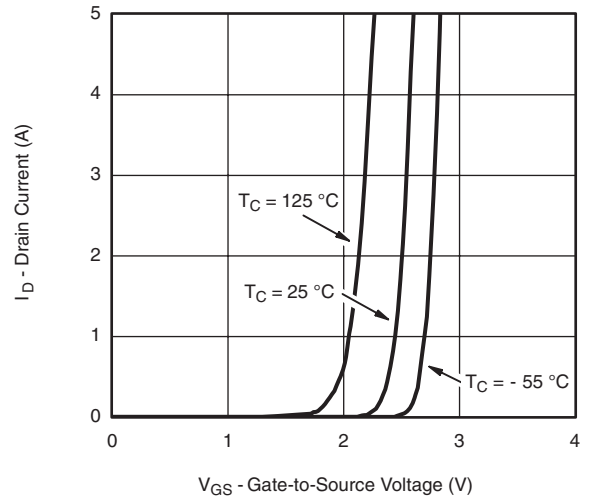
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



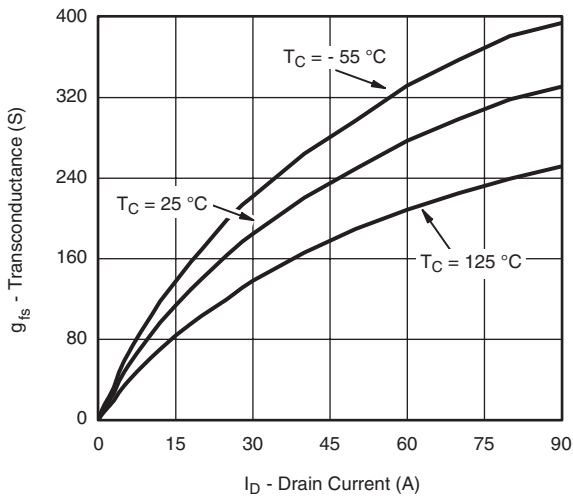
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



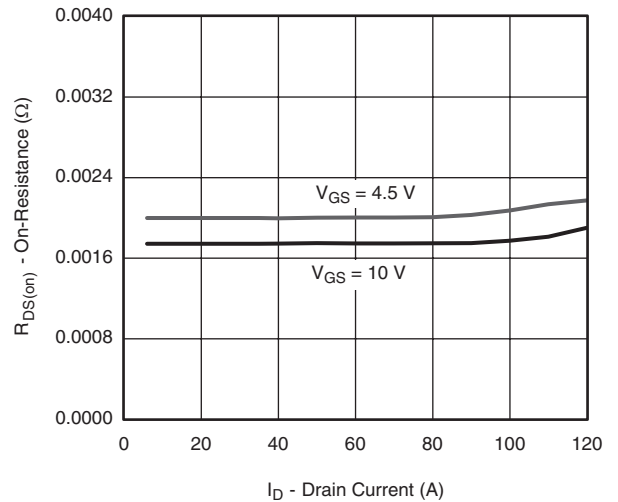
Output Characteristics



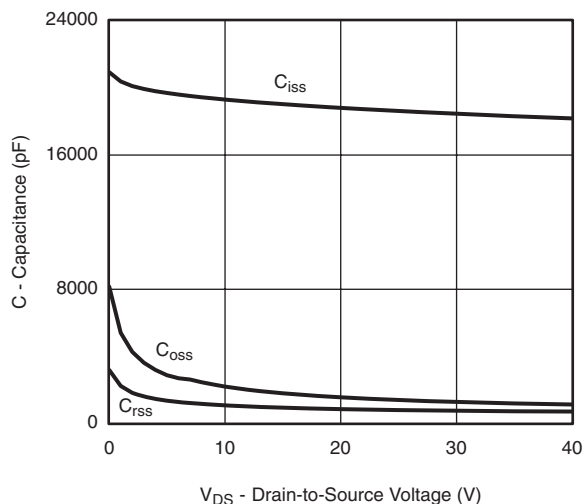
Transfer Characteristics



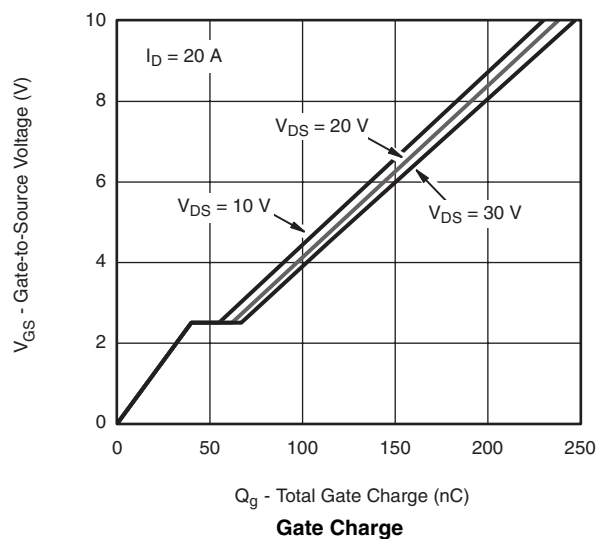
Transconductance



On-Resistance vs. Drain Current



Capacitance



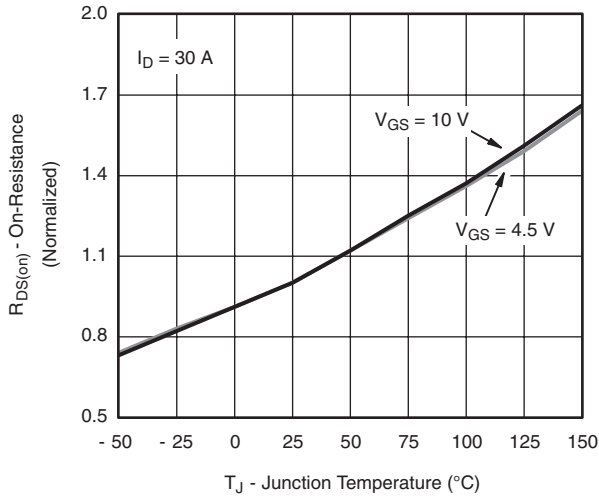
Gate Charge

SUM110N04-2m1P

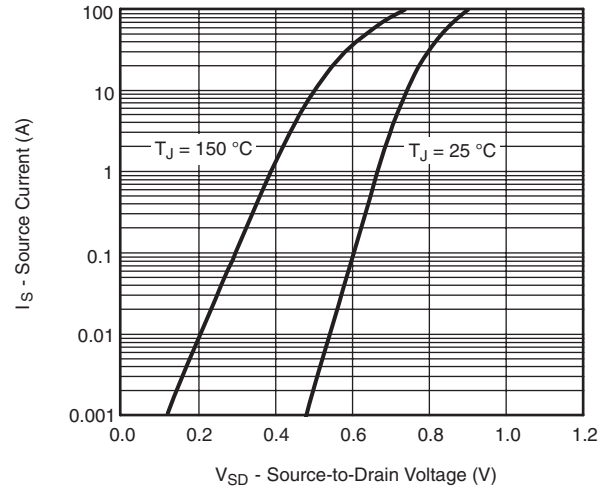


Vishay Siliconix

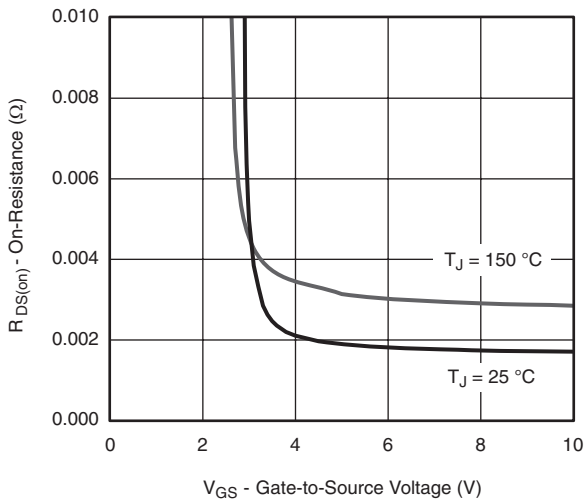
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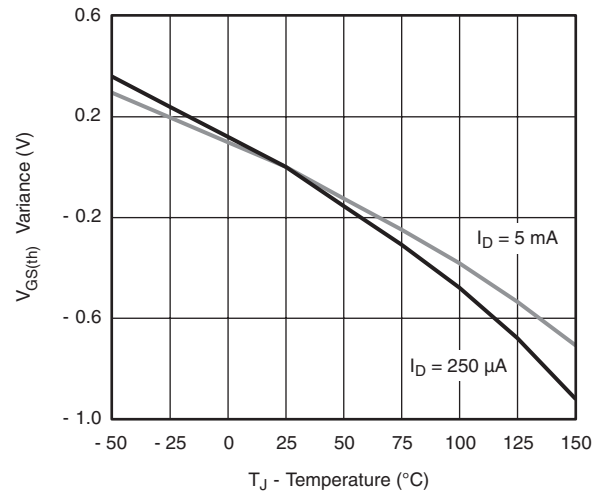
On-Resistance vs. Junction Temperature



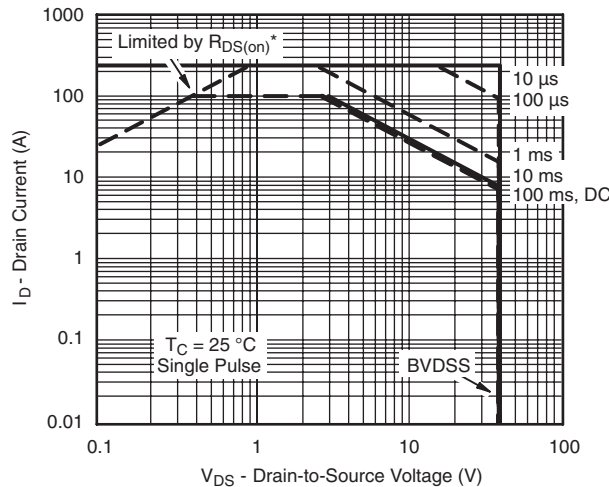
Forward Diode Voltage vs. Temperature



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

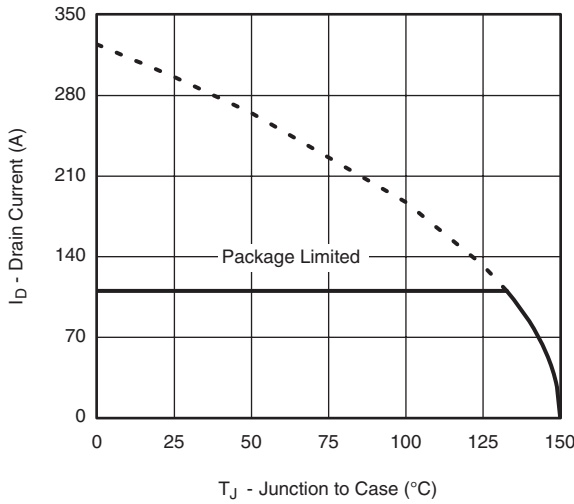


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

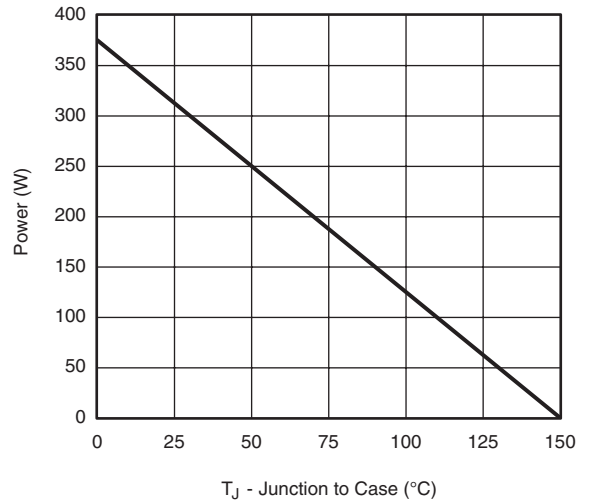
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

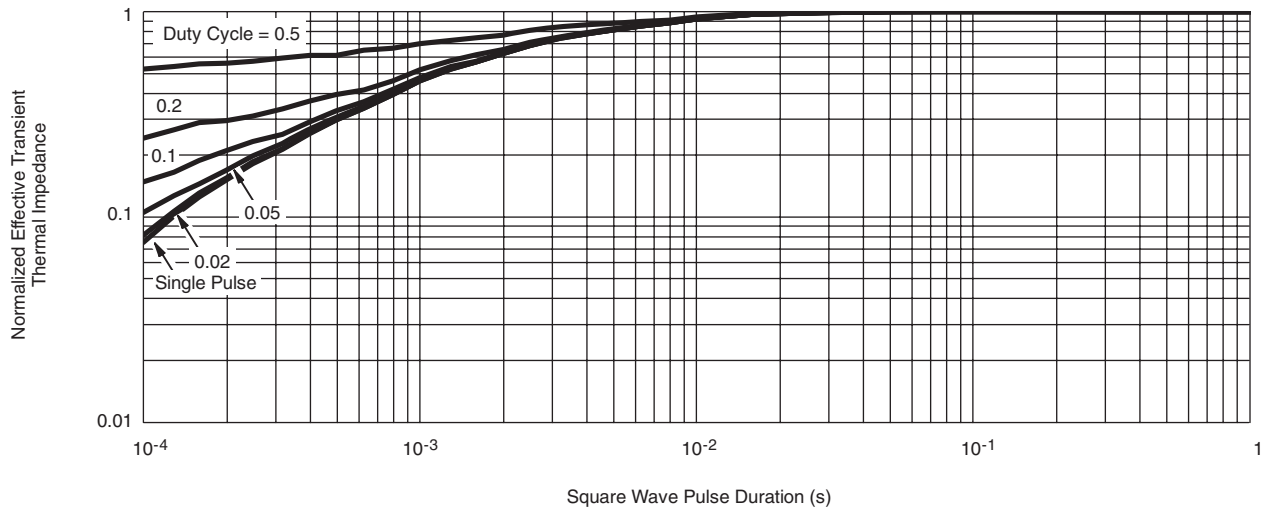


Current Derating*



Power Derating

* The power dissipation P_D is based on T_{J(max)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Case

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