XC9515 Series

2 channel Synchronous Step-Down DC/DC Converter with Manual Reset

■GENERAL DESCRIPTION

The XC9515 series consists of 2 channel synchronous step-down DC/DC converters and a voltage detector with delay circuit built-in. The DC/DC converter block incorporates a P-channel 0.35Ω (TYP.) driver transistor and a synchronous N-channel 0.35Ω (TYP.) switching transistor. By minimizing ON resistance of the built-in transistors, the XC9515 series can deliver highly efficient and a stable output current up to 800mA. With high switching frequencies of 1MHz, a choice of small inductor is possible. The series has a built-in UVLO (under-voltage lock-out) function, therefore, the internal P-channel driver transistor is forced OFF when input voltage becomes 1.8V or lower (for XC9515A, 2.7V or lower). The voltage detector block can be set delay time freely by connecting an external capacitor. With the manual reset function, the series can output a reset signal at any time.

■APPLICATIONS

- ●DVDs
- ●Blu-ray Disk
- ●LCD TVs, LCD modules
- ●Multifunctional printers
- ●Photo printers
- ●Set top boxes

■FEATURES

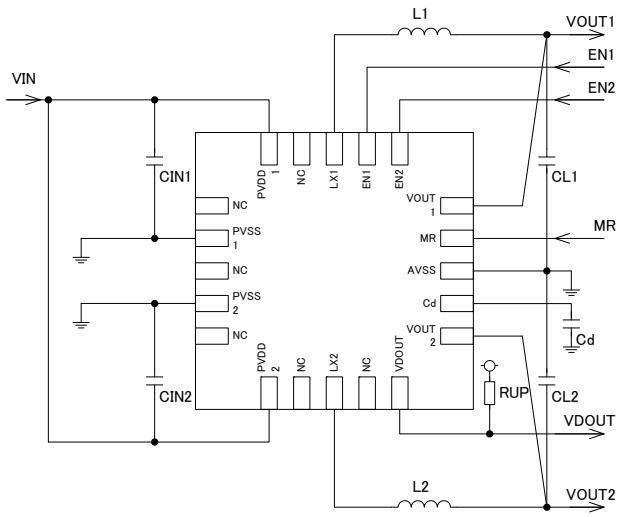
DC/DC Block

Input Voltage Range	: 2.5V～5.5V
Output Voltage	: V_{OUT1}=1.2V～4.0V V_{OUT2}=1.2V～4.0V (Accuracy ±2%)
Oscillation Frequency	: 1MHz (Accuracy ±15%)
High Efficiency	: 95% (V_{IN}=5V, V_{OUT}=3.3V)
Output Current	: 800mA
Control	: PWM control
Protection Circuits	: Thermal Shutdown : Integral Latch（Over Current Limit） : Short Protection Circuit
Ceramic Capacitor Compatible	

Voltage Detector (VD) Block

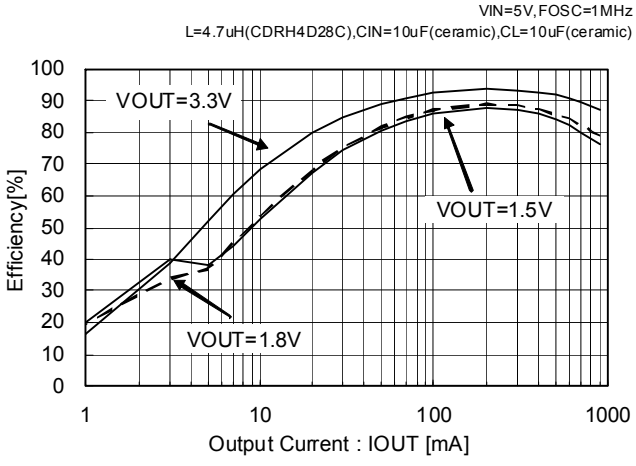
Detect Voltage Range	: 2.0～5.5V（Accuracy ±2%）
Delay Time	: 173 ms (When Cd=0.1μF is connected)
Output Configuration	: N-channel open drain
Package	: QFN-20

■TYPICAL APPLICATION CIRCUIT

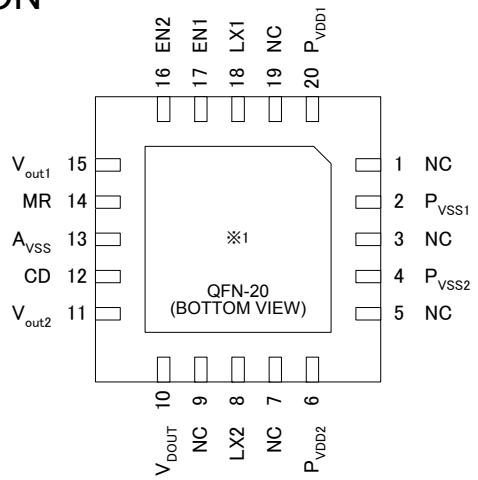


■ TYPICAL PERFORMANCE CHARACTERISTICS

● Efficiency vs. Output Current



■PIN CONFIGURATION



■ PIN ASSIGNMENT

QFN-20

PIN NUMBER	PIN NAME	FUNCTION	PIN NUMBER	PIN NAME	FUNCTION
1	NC	No Connection	11	V_{OUT2}	Output Voltage Sense 2
2	P_V_{SS1}	Power Ground 1	12	Cd	Delay Capacitor Connection
3	NC	No Connection	13	A_V_{SS}	Analog Ground
4	P_V_{SS2}	Power Ground 2	14	MR	Manual Reset
5	NC	No Connection	15	V_{OUT1}	Output Voltage Sense1
6	P_V_{DD2}	Power Supply 2	16	EN2	CH2 ON/OFF Control
7	NC	No Connection	17	EN1	CH1 ON/OFF Control
8	LX2	Switching Output 2	18	LX1	Switching Output 1
9	NC	No Connection	19	NC	No Connection
10	V_{DOUT}	Voltage Detector output	20	P_V_{DD1}	Power Supply 1

*1 Back metal pad voltage ：V_{SS} level

（The back metal pad should be soldered to enhance mounting strength and heat release. If the pad needs to be connected to other circuit, care should be taken for the pad voltage level.）

■FUNCTION CHART

●EN1, EN2 and MR pins are internally pulled up. *2)

PIN	LEVEL	OPERATIONAL STATUS
EN1	High , Open	DC/DC_CH1 Operation
	Low	DC/DC_CH1 Stop
EN2	High , Open	DC/DC_CH2 Operation
	Low	DC/DC_CH2 Stop
MR	High , Open	VD_OUT Detect RESET Signal Output
	Low	VD_OUT Force RESET Signal Output

EN1, EN2 and MR pins are internally pulled up so that the levels of High and Open are same function.

●EN1, EN2 and MR pins are left open internally. *2)

PIN	LEVEL	OPERATIONAL STATUS
EN1	High	DC/DC_CH1 Operation
	Low	DC/DC_CH1 Stop
EN2	High	DC/DC_CH2 Operation
	Low	DC/DC_CH2 Stop
MR	High	VD_OUT Detect RESET Signal Output
	Low	VD_OUT Force RESET Signal Output

EN1, EN2 and MR pins are floated inside so that these pins shall not be left open outside.

*2) Please refer to the PRODUCTION CLASSIFICATION to see the combination of pull-up status regarding the EN1, EN2, and MR pins.

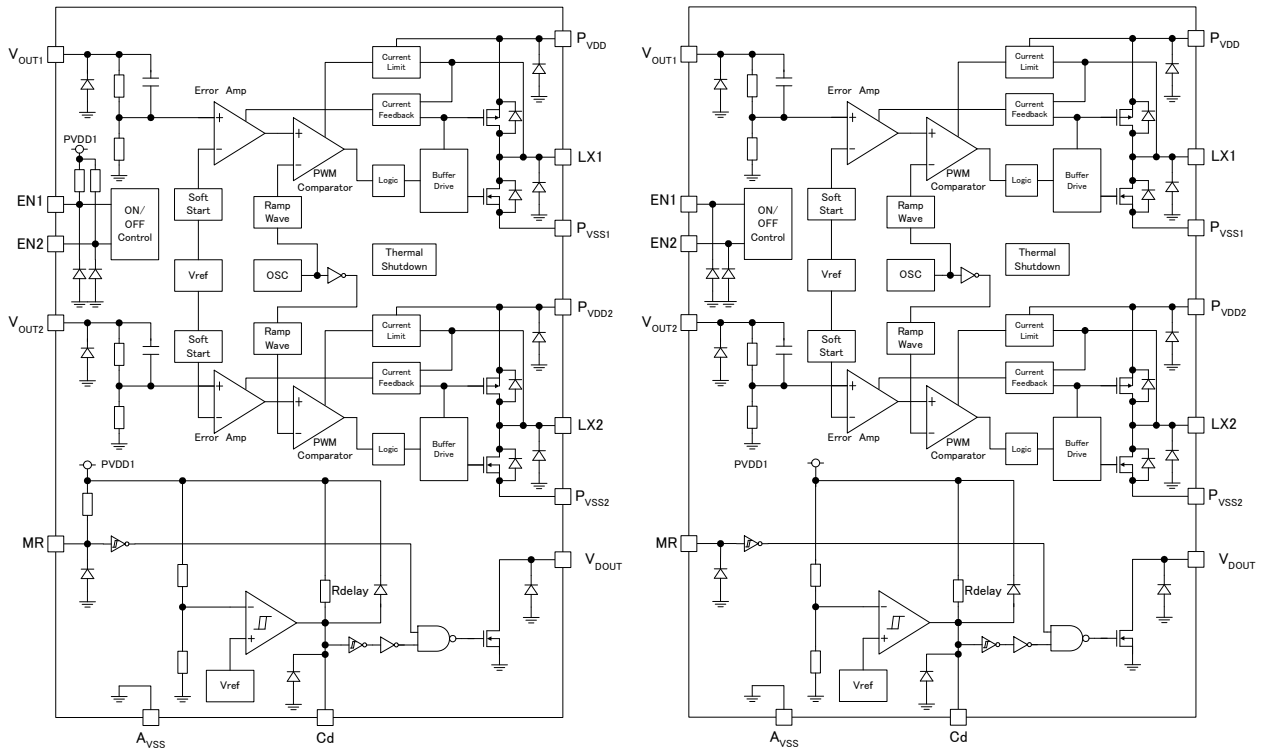
■PRODUCT CLASSIFICATION

●Ordering Information (Standard products)

XC9515①②③④⑤⑥

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Input Voltage & UVLO	A	: Input Voltage Range 5V±10%, UVLO Voltage 2.7V (TYP.)
		B	: Input Voltage Range 2.5V～5.5V, UVLO Voltage 1.8V (TYP.)
②	EN & MR logic control conditions	A	: EN1, EN2, MR pins are not pulled up internally
		B	: EN1, EN2 pins have built-in pull-up resistors, MR pin has a built-in pull-up resistor
		C	: EN1, EN2 Pins are not pulled up internally, MR pin has a built-in pull-up resistor
		D	: EN1, EN2 pins have built-in pull-up resistors, MR pin are not pulled up internally
③④	Set Voltage Combinations	01～	: Based on Torex Standard Product Number
⑤	Package	Z	: QFN-20
⑥	Device Orientation	R	: Embossed tape, Standard feed
		L	: Embossed tape, Reverse feed

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNITS
P_V_{DD1}・P_V_{DD2} Pin Voltage		P_VDD1, P_VDD2	-0.3～6.5	V
V_{OUT1}・V_{OUT2} Pin Voltage		VOUT1, VOUT2	-0.3～6.5	V
Cd Pin Voltage		VCd	-0.3～P_$V_{DD1.2}$ + 0.3	V
V_{DOUT} Pin Voltage		V_{DOUT}	-0.3～6.5	V
V_{DOUT} Pin Current		IDOUT	10	mA
EN1・EN2・MR Pin Voltage		VEN1, VEN2, VMR	-0.3～6.5	V
LX1・LX2 Pin Voltage		VLx1, VLx2	-0.3～P_$V_{DD1.2}$+0.3	V
LX1・LX2 Pin Current		ILx1, ILx2	1500	mA
Power Dissipation	QFN-20	Pd (Free air)	300	mW
		Pd (Wiring on PCB)	1000	
Operating Temperature Range		Topr	-40 ～ +85	℃
Storage Temperature Range		Tstg	-55 ～ +125	℃

* P_$V_{DD1.2}$ stands for P_V_{DD1}=P_V_{DD2}

A_V_{SS}=P_V_{SS1}=P_V_{SS2}=0V

■ELECTRICAL CHARACTERISTICS

XC9515AB04xx

● DC/DC CH1, CH2 (V_{OUT1}=1.5V, V_{OUT2}=3.3V, f_{OSC} =1MHz, EN1・2 Pull-up inside) Ta =25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Input Voltage	V_{IN}		4.5	5.0	5.5	V	–
Output Voltage 1	V_{OUT1}	Connected to the external components, P_$V_{DD1・2}$=V_{EN1}=V_{EN2}=0V, I_{OUT1}=30mA	1.470	1.500	1.530	V	①
Output Voltage 2	V_{OUT2}	Connected to the external components, P_$V_{DD1・2}$=V_{EN2}=V_{EN1}=0V, I_{OUT2}=30mA	3.234	3.300	3.366	V	①
Maximum Output Current 1・2 (*1)	$I_{OUTMAX1}$ $I_{OUTMAX2}$		800	–	–	mA	①
Current Limit 1・2	I_{LIM1} ・ I_{LIM2}		1000	–	–	mA	②
Oscillation Frequency	f_{OSC}	Connected to the external components, I_{OUT}=10mA	0.85	1.00	1.15	MHz	①
Maximum Duty Cycle	MAXDTY	V_{OUT1}=V_{OUT2}=0V	100	–	–	%	②
Minimum Duty Cycle	MINDTY	V_{OUT1}=V_{OUT2}=V_{IN}	–	–	0	%	②
Efficiency 1 (*2)	EFFI1	Connected to the external components, P_$V_{DD1・2}$=V_{EN1}=5.0V, V_{EN2}=0V, V_{OUT1}=1.5V, I_{OUT}1=200mA	–	89	–	%	①
Efficiency 2 (*2)	EFFI2	Connected to the external components, P_$V_{DD1・2}$=V_{EN2}=5.0V, V_{EN1}=0V, V_{OUT2}=3.3V, I_{OUT2}=200mA	–	94	–	%	①
LX1・2 "H" ON Resistance	R_{LX1H}・R_{LX2H}	V_{OUT1}=V_{OUT2}=0V, I_{Lx1}=I_{Lx2}=100mA (*3)	–	0.35(*4)	–	Ω	③
LX1・2 "L" ON Resistance	R_{LX1L}・R_{LX2L}		–	0.35(*4)	–	Ω	–
Integral Latch Time 1・2	t_{LAT1}・ t_{LAT2}	LX1 and LX2 are pulled down by a resistor of 200Ω V_{OUT1}=Setting Voltage × 0.9, V_{OUT2}= Setting Voltage × 0.9(*5)	–	6	–	ms	⑦
Soft-Start Time 1・2	t_{SS1}・ t_{SS2}	Time until EN1, EN2 or both pins changes from 0V to V_{IN} and voltage becomes $V_{OUT1・2}$ × 0.95, $I_{OUT1・2}$=10mA	–	1.3	–	ms	①
EN1・2 "H" Level Voltage	V_{EN1H}・ V_{EN2H}	V_{OUT1}=V_{OUT2}=0V Voltage which LX1 or LX2 becomes "H"(*6)	1.2	–	5	V	④
EN1・2 "L" Level Voltage	V_{EN1L}・ V_{EN2L}	V_{OUT1}=V_{OUT2}=0V Voltage which LX1 or LX2 becomes "L"(*6)	AVSS	–	0.4	V	④
EN1・2 "H" Level Current	I_{EN1H}・I_{EN2H}	P_$V_{DD1・2}$=V_{EN1}=V_{EN2}=5.5V	–		0.1(*8)	μA	④
EN1・2 "L" Level Current	I_{EN1L}・I_{EN2L}	P_$V_{DD1・2}$=5.5V, V_{EN1}=V_{EN2}=0V	–	-6(*8)	–	μA	④
LX1・2 "H" Leakage Current (*7)	I_{LEAK1H}・ I_{LEAK2H}	P_$V_{DD1・2}$=V_{LX1}=V_{LX2}=5.5V, V_{EN1}=V_{EN2}=0V	–	–	1.0(*9)	μA	④
LX1・2 "L" Leakage Current	I_{LEAK1L}・ I_{LEAK2L}	P_$V_{DD1・2}$=5.5V, V_{LX1}=V_{LX2}=V_{EN1}=V_{EN2}=0V	-3.0(*9)	–	–	μA	④

Test Conditions：
* P_$V_{DD1・2}$ stands for P_V_{DD1}=P_V_{DD2}
**Unless otherwise stated, P_$V_{DD1・2}$=5V, V_{EN1}=V_{EN2}= P_$V_{DD1・2}$
*** A_V_{SS}=P_V_{SS1}=P_V_{SS2}=0V
NOTE :
*1 : When the difference between the input and the output is small, some cycles may be skipped completely before current maximizes. If current is further pulled from this state, output voltage will decrease because of P-ch driver ON resistance.
*2 : EFFI = { (output voltage x output current) / (input voltage x input current) } x 100
*3 : On resistance (Ω)= (V_{IN} - Lx pin measurement voltage) / 100mA
*4 : Designed value.
*5 : Time until it short-circuits LX1 (LX2 in the side of 2CH) with GND via 1Ω of resistor from an operational state and is set to Lx=0V from current limit pulse generating.
*6 : "H" is judged as "H">V_{IN}-0.1V, "L" is judged as "L"<0.1V.
*7 : When temperature is high, a current of approximately 20μA (maximum) may leak.
*8 : Current which EN1 and EN2 are measured separately.
*9 : Lead current which LX1 and LX2 are measured separately.

■ELECTRICAL CHARACTERISTICS (Continued)

XC9515AB04xx

●Voltage Detector (VD) (MR pin Pull-up Inside) Block Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Detect Voltage	$V_{DF(E)}$ (*1)		$V_{DF(T)}$ ×0.98	$V_{DF(T)}$ (*2)	$V_{DF(T)}$ ×1.02	V	⑤
Hysteresis Width	V_{HYS}	$V_{HYS}=(V_{DR(E)}$ (*3) $- V_{DF(E)}) / V_{DF(E)} \times 100$	–	5.0	–	%	–
VD Output Current	I_{DOUT}	$P\_V_{DD1\cdot2}=V_{DF}$-0.01V, Apply 0.5V to V_{DOUT}	5.0	6.6	8.0	mA	④
Delay Resistance	R_{DLY}		–	2.5	–	MΩ	–
MR "H" Level Voltage	V_{MRH}	V_{DOUT}="H" Level Voltage (*3)	1.2	–	5.5	V	④
MR "L" Level Voltage	V_{MRL}	V_{DOUT}="L" Level Voltage (*3)	AVSS	–	0.4	V	④
MR "H" Level Current	I_{MRH}	$P\_V_{DD1\cdot2}=V_{MR}$=5.5V	–	–	0.1	μA	④
MR "L" Level Current	I_{MRL}	$P\_V_{DD1\cdot2}$=5.5V, V_{MR}=0V	–	-6.0	–	μA	④

Test Conditions：

* $P\_V_{DD1\cdot2}$ stands for $P\_V_{DD1}=P\_V_{DD2}$

**Unless otherwise stated, $P\_V_{DD1\cdot2}$=5V, $V_{EN1}=V_{EN2}=P\_V_{DD1\cdot2}$

*** $A\_V_{SS}=P\_V_{SS1}=P\_V_{SS2}$=0V

NOTE :

*1：$V_{DF(E)}$=Detect Voltage

*2：$V_{DR(E)}$=Release Voltage

*3："H" is judged as "H">V_{IN}-0.1V, "L" is judged as "L"<0.1V

XC9515AB04xx

●Whole Circuit (V_{OUT1}=1.5V, V_{OUT2}=3.3V, f_{OSC}=1MHz, EN1・2 Pull-up Inside) Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Supply Current 1	I_{DD1}	$V_{OUT1}=V_{OUT2}$=Setting Voltage x 0.9	–	950	1500	μA	⑥
Supply Current 2	I_{DD2}	$V_{OUT1}=V_{OUT2}$=Setting Voltage x 1.1（Oscillation stops）	–	75	145	μA	⑥
Stand-by Current	I_{STB}	$V_{EN1}=V_{EN2}$=0V	–	18	33	μA	⑥
UVLO Detect Voltage	V_{UVLOF}	V_{IN} voltage which V_{OUT1}=0V and LX pin becomes "L" (*1)	2.4	1.8	3.0	V	②
UVLO Release Voltage	V_{UVLOR}	V_{IN} voltage which V_{OUT1}=0V and LX pin becomes "H" (*1)	–	–	3.5	V	②
Thermal Shutdown Temperature	T_{TSD}		–	150	–	°C	–
Thermal Shutdown Hysteresis Width	T_{HYS}		–	20	–	°C	–

Test Conditions：

* $P\_V_{DD1\cdot2}$ stands for $P\_V_{DD1}=P\_V_{DD2}$

**Unless otherwise stated, $P\_V_{DD1\cdot2}$=5V, $V_{EN1}=V_{EN2}=P\_V_{DD1\cdot2}$

*** $A\_V_{SS}=P\_V_{SS1}=P\_V_{SS2}$=0V

NOTE :

*1："H" is judged "H">V_{IN}-0.1V, "L" is judged "L"<0.1V

■ELECTRICAL CHARACTERISTICS (Continued)

XC9515BA06xx

●DC/DC CH1, CH2 (V_{OUT1}=1.5V, V_{OUT2}=3.3V, f_{OSC}=1MHz, EN1 and EN2 pins are internally floating) Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Input Voltage	V_{IN}		2.5		5.5	V	
Output Voltage1	V_{OUT1}	Connected to the external components, $P_{VDD1,2}$=EN1, EN2=0V I_{OUT1}=30mA	1.470	1.500	1.530	V	①
Output Voltage2	V_{OUT2}	Connected to the external components, $P_{VDD1,2}$=EN2, EN1=0V I_{OUT2}=30mA	3.234	3.300	3.366	V	①
Maximum Output Current 1・2 (*1)	$I_{OUTMAX1}$ $I_{OUTMAX2}$		800			mA	①
Current Limit 1・2	I_{LIM1} ・I_{LIM2}		1000			mA	②
Oscillation Frequency	f_{OSC}	Connected to the external components, I_{OUT}=10mA	0.85	1.00	1.15	MHz	①
Maximum Duty Cycle	MAXDTY	V_{OUT1}=V_{OUT2}=0V	100			%	②
Minimum Duty Cycle	MINDTY	V_{OUT1}=V_{OUT2}=V_{IN}			0	%	②
Efficiency 1 (*2)	EFFI1	Connected to the external components, $P_{VDD1,2}$=EN1=5.0V, EN2=0V V_{OUT1}=1.5V, I_{OUT1}=200mA		89		%	①
Efficiency 2 (*2)	EFFI2	Connected to the external components, $P_{VDD1,2}$=EN2=5.0V, EN1=0V V_{OUT2}=3.3V, I_{OUT2}=200mA		94		%	①
LX1・2 "H" ON Resistance	R_{LX1H}・R_{LX2H}	V_{OUT1}=V_{OUT2}=0V, ILx1=ILx2=100mA(*3)		0.35(*4)		Ω	③
LX1・2 "L" ON Resistance	R_{LX1L}・R_{LX2L}			0.35(*4)		Ω	-
Integral Latch Time 1・2	t_{LAT1}・t_{LAT2}	LX1 and LX2 are pulled down by a resistor of 200Ω V_{OUT1}= Setting Voltage×0.9, V_{OUT2}= Setting Voltage×0.9 (*5)		6		ms	⑦
Soft-Start Time 1・2	t_{SS1}・t_{SS2}	Time until EN1, EN2 or both pins changes from 0V to V_{IN} and voltage becomes $V_{OUT1,2}$×0.95, $I_{OUT1,2}$=10mA		1.3		ms	①
EN1・2 "H" Voltage	V_{EN1H}・V_{EN2H}	V_{OUT1}=V_{OUT2}=0V Voltage which LX1 or LX2 becomes "H" (*6)	1.2		5	V	④
EN1・2 "L" Voltage	V_{EN1L}・V_{EN2L}	V_{OUT1}=V_{OUT2}=0V Voltage which LX1 or LX2 becomes "L" (*6)	AVSS		0.4	V	④
EN1・2 "H" Current	I_{EN1H}・I_{EN2H}	$P_{VDD1,2}$=EN1=EN2=5.5V			0.1(*8)	μA	④
EN1・2 "L" Current	I_{EN1L}・I_{EN2L}	$P_{VDD1,2}$=5.5V, EN1=EN2=0V	-0.1(*8)			μA	④
LX1・2 "H" Leak Current (*7)	I_{leak1H}・I_{leak2H}	$P_{VDD1,2}$=LX1=LX2=5.5V, EN1=EN2=0V			1.0(*9)	μA	④
LX1・2 "L" Leak Current	I_{leak1L}・I_{leak2L}	$P_{VDD1,2}$=5.5V, LX1=LX2=EN1=EN2=0V	-3.0(*9)			μA	④

Test Conditions：
* $P\_V_{DD1,2}$ stands for P_V_{DD1}=P_V_{DD2}
**Unless otherwise stated, $P\_V_{DD1,2}$=5V, V_{EN1}=V_{EN2}= $P\_V_{DD1,2}$
*** A_V_{SS}=P_V_{SS1}=P_V_{SS2}=0V
NOTE :
*1：When the difference between the input and the output is small, some cycles may be skipped completely before current maximizes. If current is further pulled from this state, output voltage will decrease because of P-ch driver ON resistance.
*2：EFFI = { (output voltage x output current) / (input voltage x input current) } x 100
*3：On resistance (Ω)= (V_{IN} - Lx pin measurement voltage) / 100mA
*4：Designed value.
*5：Time until it short-circuits LX1 (LX2 in the side of 2CH) with GND via 1Ω of resistor from an operational state and is set to Lx=0V from current limit pulse generating.
*6："H" is judged as "H">V_{IN}-0.1V, "L" is judged as "L"<0.1V.
*7：When temperature is high, a current of approximately 20μA (maximum) may leak.
*8：Current which EN1 and EN2 are measured separately.
*9：Lead current which LX1 and LX2 are measured separately.

■ELECTRICAL CHARACTERISTICS (Continued)

XC9515BA06xx

●VD (MR pin is internally floating) Ta=25 °C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Detect Voltage	$V_{DF(E)}$ (*1)		2.94	3.00	3.06	V	⑤
Hysteresis Width	V_{HYS}	$V_{HYS}=\{V_{DR(E)}$ (*2)$-V_{DF(E)}\}/ V_{DF(E)}\times100$		5.0		%	-
VD Output Current	I_{DOUT}	$P\_V_{DD1\cdot2}=V_{DF}$-0.01V, Apply 0.5V to V_{DOUT}	5.0	6.6	8.0	mA	④
Delay Resistance	R_{DLY}			2.5		MΩ	-
MR "H" Level Voltage	V_{MR}	V_{DOUT}="H" Level Voltage (*3)	1.2		5.5	V	④
MR "L" Level Voltage	V_{MR}	V_{DOUT}="L" Level Voltage (*3)	AVSS		0.4	V	④
MR "H" Level Current	I_{MR}	$P_{VDD1\cdot2}$=MR=5.5V			0.1	μA	④
MR "L" Level Current	I_{MR}	$P_{VDD1\cdot2}$=5.5V,MR=0V	-0.1(*8)			μA	④

Test Conditions：

* $P\_V_{DD1\cdot2}$ stands for $P\_V_{DD1}=P\_V_{DD2}$

**Unless otherwise stated, $P\_V_{DD1\cdot2}$=5V, $V_{EN1}=V_{EN2}=P\_V_{DD1\cdot2}$

*** $A\_V_{SS}=P\_V_{SS1}=P\_V_{SS2}$=0V

NOTE :

*1：$V_{DF(E)}$=Detect Voltage

*2：$V_{DR(E)}$=Release Voltage

*3："H" is judged as "H">V_{IN}-0.1V, "L" is judged as "L"<0.1V

XC9515BA01xx

●Whole Circuit (V_{OUT1}=1.5V, V_{OUT2}=3.3V, f_{OSC}=1MHz, EN1 and EN2 pins are internally floating) Ta=25 °C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Supply Current 1	I_{DD1}	$V_{OUT1}=V_{OUT2}$= Setting Voltage × 0.9		950	1500	μA	⑥
Supply Current 2	I_{DD2}	$V_{OUT1}=V_{OUT2}$= Setting Voltage × 1.1 (Oscillation stops)		75	145	μA	⑥
Stand-by Current	I_{STB}	EN1=EN2=0V		5.5	11	μA	⑥
UVLO Detect Voltage	V_{UVLOF}	V_{IN} voltage which V_{OUT1}=0V and L_X pin becomes "L" (*1)	1.5	1.8	2.1	V	②
UVLO Release Voltage	V_{UVLOR}	V_{IN} voltage which V_{OUT1}=0V and L_X pin becomes "H" (*1)			2.3	V	②
Thermal Shutdown Temperature	T_{TSD}			150		°C	-
Thermal Shutdown Hysteresis Width	T_{HYS}			20		°C	-

Test Conditions：

* $P\_V_{DD1\cdot2}$ stands for $P\_V_{DD1}=P\_V_{DD2}$

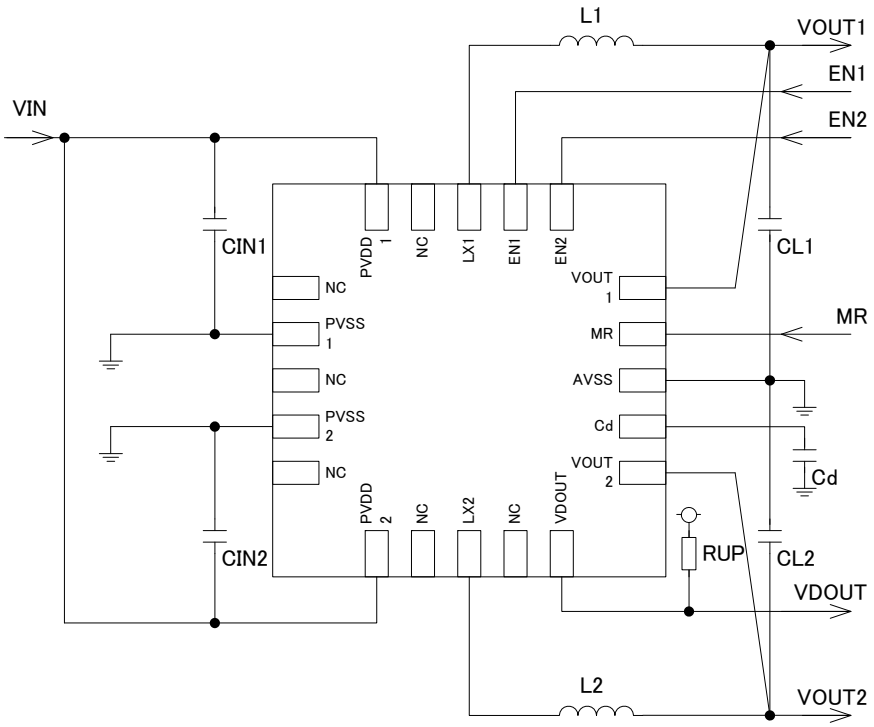
**Unless otherwise stated, $P\_V_{DD1\cdot2}$=5V, $V_{EN1}=V_{EN2}=P\_V_{DD1\cdot2}$

*** $A\_V_{SS}=P\_V_{SS1}=P\_V_{SS2}$=0V

NOTE :

*1："H" is judged "H">V_{IN}-0.1V, "L" is judged "L"<0.1V

■TYPICAL APPRICATION CIRCUIT



＜Example of the External Components＞

L1 ：4.7μH（CDRH4D28C, SUMIDA）
L2 ：4.7μH（CDRH4D28C, SUMIDA）
C_{IN1} ：10μF（ceramic）
C_{IN2} ：10μF（ceramic）
C_{L1} ：10μF（ceramic）
C_{L2} ：10μF（ceramic）
RUP ：100kΩ

■OPERATIONAL EXPLANATION

XC9515 series consists of a reference voltage source, ramp wave circuit, error amplifier, PWM comparator, phase compensation circuit, output voltage adjustment resistors, P-channel driver transistor, N-channel synchronous switching transistor, current limit circuit, UVLO circuit and others. The series ICs compare, using the error amplifier, the voltage of the internal voltage reference source with the feedback voltage from V_{OUT} pin through split resistors, R_{FB1} and R_{FB2}. Phase compensation is performed on the resulting error amplifier output, to input a signal to the PWM comparator to determine the turn-on time during PWM operation. The PWM comparator compares, in terms of voltage level, the signal from the error amplifier with the ramp wave from the ramp wave circuit, and delivers the resulting output to the buffer driver circuit to cause the Lx pin to output a switching duty cycle. This process is continuously performed to ensure stable output voltage. The current feedback circuit monitors the P-channel driver transistor current for each switching operation, and modulates the error amplifier output signal to provide multiple feedback signals. This enables a stable feedback loop even when a low ESR capacitor, such as a ceramic capacitor, is used, ensuring stable output voltage.

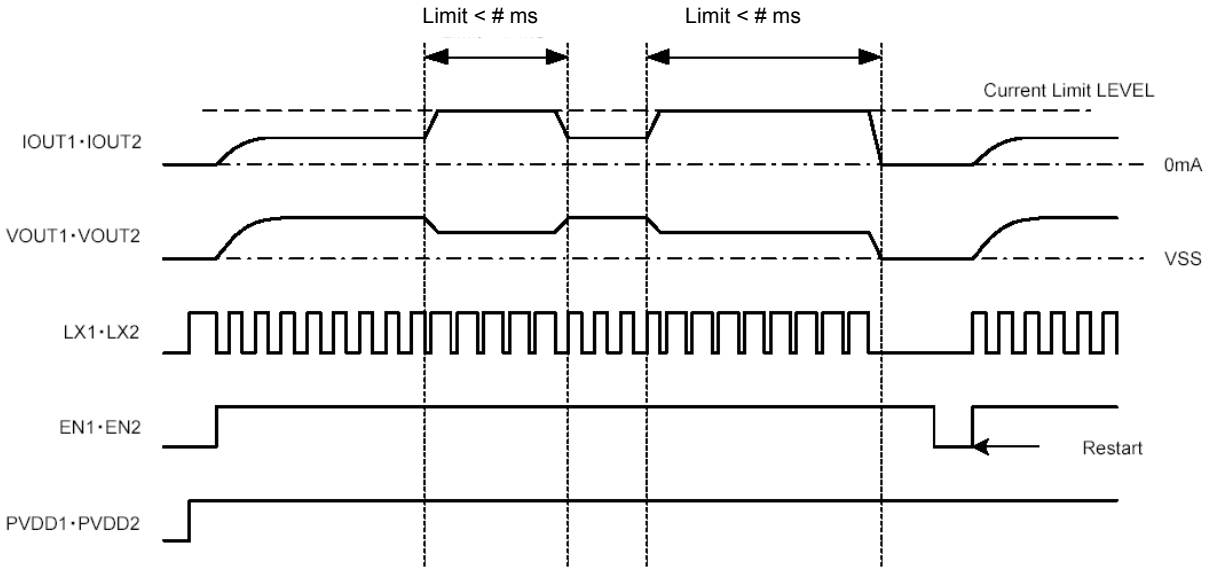
<Reference Voltage Source>
The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

<Ramp Wave Circuit>
The ramp wave circuit determines switching frequency. The frequency is fixed internally at 1MHz. Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation, and to synchronize all the internal circuits.

<Error Amplifier>
The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage divided by the internal split resistor, R_{FB1} and R_{FB2}. When a voltage lower than the reference is fed back, the output voltage of the error amplifier increases. The gain and frequency characteristics of the error amplifier output are fixed internally to deliver an optimized signal to the mixer.

<Current Limit>
The current limiter circuit of the XC9515 series monitors the current flowing through the P-channel MOS driver transistor connected to the Lx pin, and features a combination of the current limit mode and the latch mode.

①When the driver current is greater than a specific level (peak value of coil current), the current limit function operates to off the pulses from the Lx pin at any giving timing.
②When the driver transistor is turned off, the limiter circuit is then released from the current limit detection state.
③At the next pulse, the driver transistor is turned on. However, the transistor is immediately turned off in the case of an over current state.
④When the over current is eliminated, the IC resumes its normal operation.
The IC waits for the over current state to end by repeating the steps ① to ③. If an over current state continues for a few ms and the above three steps are repeatedly performed, the IC performs the function of latching the OFF state of the driver transistor. Both two DC/DC blocks stop operations when either CH1 or CH2 of protection circuit is activated. At this time, both Lx1 and Lx2 become high impedance. Once the IC is in latch mode, operations can be resumed by either turning the IC off after letting EN1 and EN2 pins down to low level, or by restoring power. For restoring power, the IC should be turned off after P_V_{DD1} and P_V_{DD2} voltages drop below the low level of EN1 and EN2 pin.) The latch operation can be released from the current limit detection state because of the circuit's noise. Also, depending on the state of the PC Board, latch time may become longer and latch operation may not work. In order to avoid the effect of noise, the board should be laid out so that capacitors are placed as close to the chip as possible.



■OPERATIONAL EXPLANATION (Continued)

<Thermal Shutdown>

For protecting the IC from heat damage, the thermal shutdown circuit monitors the chip temperature. When the chip temperature reaches 150℃, the thermal shutdown circuit operates and the driver transistor will be set to OFF. As the chip temperature drops to 130℃ by stopping current flow, the soft-start function operates to turn the output on.

<Short-Circuit Protection>

The short-circuit protection circuit monitors the FB voltage. If the output is shorted incorrectly with the ground, the short-circuit protection circuit operates and turns the driver transistor off to latch when the FB voltage becomes less than half of the setting voltage. Both two DC/DC blocks stop operations when either CH1 or CH2 of protection circuit is activated. At this time, both Lx1 and Lx2 become high impedance. Once the IC is in latch mode, operations can be resumed by either turning the IC off after letting both ends of EN1 and EN2 pins down to low level, or by restoring power. (The P_V_{DD1} and P_V_{DD2} voltages should be less than the low level of the EN1 and EN2 pins when restoring power.)

<Soft Start Function>

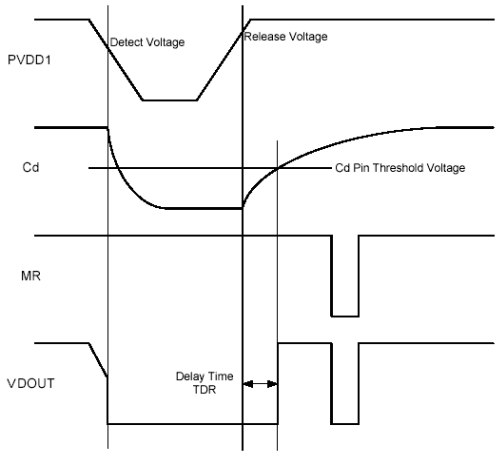
The soft-start circuit protects against inrush current, when the power is switched on, and also to protect against voltage overshoot. It should be noted, however, that this circuit does not protect the load capacitor (C_L) from inrush current. With the Vref voltage limited and depending upon the input to the error amps, the operation maintains a balance between the two inputs of the error amps and controls the EXT1 pin's ON time so that it doesn't increase more than is necessary.

<UVLO Circuit>

When the V_{IN} pin voltage becomes1.8V (TYP.) or lower (for XC9515A, 2.7V or lower), the P-channel output driver transistor is forced OFF to prevent false pulse output caused by unstable operation of the internal circuitry. When the V_{IN} pin voltage becomes 1.9V (TYP.) or higher (for XC9515A, 3.0V or lower), switching operation takes place. By releasing the UVLO function, the IC performs the soft-start function to initiate output startup operation.

<Voltage Detector Block>

The series' detector function monitors the voltage divided by resistors connected to the P_V_{DD1} pin, as well as monitoring the voltage of the internal reference voltage source via the comparator. Because of hysteresis at the detector function, output at the V_{DOUT} pin will invert when the sense pin voltage of the detector block (P_V_{DD1}) increases above the release voltage (105% of the detect voltage). The output configuration of the V_{DOUT} pin is N-channel open drain, therefore, a pull-up resistor is required. The voltage detector block has a manual reset (MR) pin. By setting the MR pin at low level, the V_{DOUT} pin is forced to be at low level.



By connecting a capacitor (Cd) to the Cd pin, the XC9515 series can set a delay time to V_{DOUT} pin's output signal when releasing voltage. The delay time can be calculated from the internal resistance, Rdelay (2.5MΩ fixed TYP.) and the value of Cd as per the following equation. As selecting the capacitor (Cd), the delay time can be set freely.

t_{DR} (Delay time) ＝Cd x Rdelay x 0.69

●Release Delay Ta=25°C

Delay Capacity Cd [μF]	Release Delay t_{DR} (TYP.) [ms]	Release Delay t_{DR} (MIN.～MAX.) [ms]
0.01	17	10～24
0.022	38	23～53
0.047	81	49～113
0.1	173	103～242
0.22	380	228～532
0.47	811	487～1135
1	1725	1035～2415

■NOTES ON USE

1. Please use this IC within the stated maximum ratings. The IC is liable to malfunction should the ratings be exceeded.

2. Please apply the same electrical potential to the P_V_{DD1} and P_V_{DD2} pins. Even where either CH1 or CH2 is used, both P_V_{DD1} and P_V_{DD2} pins should have the same electrical potential. Applying the electrical potential to only one side causes malfunction. Also the same electrical potential should be applied to the P_V_{SS1}, P_V_{SS2} and A_V_{SS} pins.

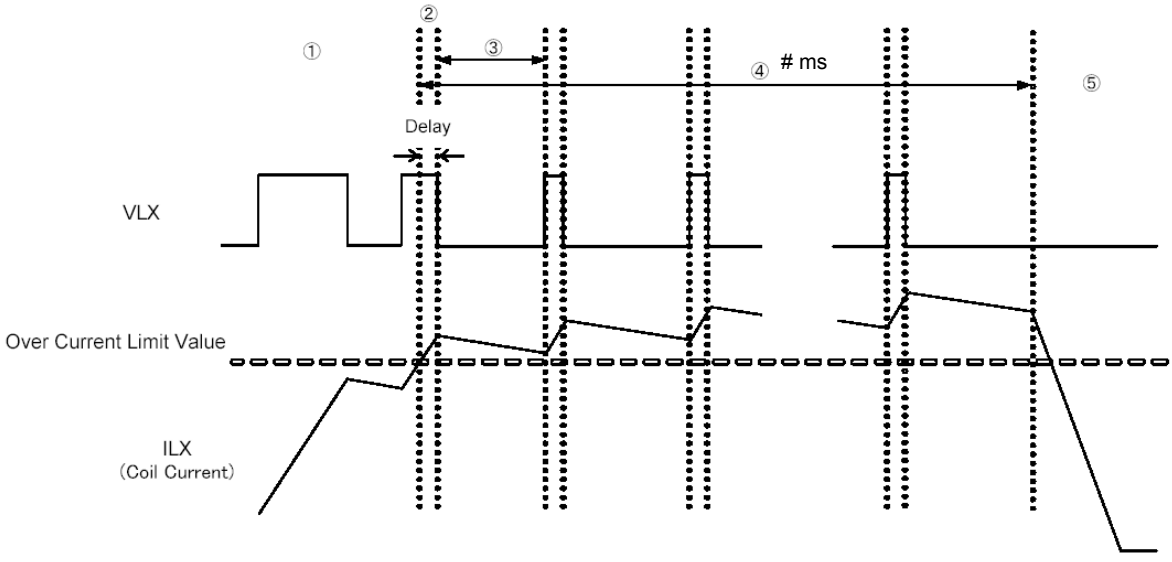
3. The XC9515 series is designed for use with ceramic output capacitors. If, however, the potential difference between dropout voltage or output current is too large, a ceramic capacitor may fail to absorb the resulting high switching energy and the output could be unstable. If the input-output potential difference is large, use a larger output capacitor to compensate for insufficient capacitance.

4. When the peak current, which exceeds limit current flows within the specified time, the built-in driver transistor is turned off (the integral latch circuit). During the time until it detects limit current and before the built-in transistor can be turned off, the current for limit current flows; therefore, care must be taken when selecting the rating for the coil.

5. When the input voltage is low, limit current may not be reached because of voltage falls caused by ON resistance or serial resistance of the coil.

6. Since the potential difference for input voltage has occurred to the both ends of a coil, the time changing rate of the coil current is large when the P-channel driver transistor is ON. On the other hand, since the V_{OUT} pin short-circuits to the GND when the N-channel transistor is ON and there is almost no potential difference of the coil both ends, the time changing rate of the coil current becomes very small.
   This operation is repeated and the delay time of the circuit also influences, therefore, the coil current is converged on the current value beyond the amount of current which should be restricted essentially.
   The short-circuit protection does not operate during the soft-start time. As soon as the soft-start time finishes, the short-circuit protection starts to operate and the circuit becomes disable.
   The delay time of the circuit also influences when step-down ratio is large, as the result, a current more than over current limit may flow. Please do not exceed the absolute maximum ratings of the coil.

   ① A current flows to the driver transistor up to the current limit (I_{LIM}).
   ② For the delay time of the circuit, a current more than the I_{LIM} flows after the I_{LIM} decide until the P channel driver transistor turns off.
   ③ Time changing rate of the coil current becomes very small because there is no potential difference between both ends of the coil.
   ④ The Lx pin oscillates a narrow pulse during the soft-start time because of the current limit.
   ⑤ The circuit is latched since the short-circuit protection operates and the P-channel driver transistor is turned off.



■NOTES ON USE (Continued)

7. Driving current below the minimum operating voltage may lead malfunction to the UVLO circuit because of the noise.

8. Depending on the PC board condition, the latch function may be released from limit current detection state and the latch time may extend or fail to reach the latch operation. Please locate the input capacitance as close to the IC as possible.

9. Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the coil inductance, capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.

10. With the DC/DC converter block of the IC, the peak current of the coil is controlled by the current limit circuit. Since the peak current increases when dropout voltage or load current is high, current limit starts operating, and this can lead to instability. When peak current becomes high, please adjust the coil inductance value and fully check the circuit operation. In addition, please calculate the peak current according to the following formula:

    Peak current: Ipk = (V_{IN} - V_{OUT}) x OnDuty / (2 x L x fosc) + I_{OUT}
    L: Coil Inductance Value, f_{OSC}: Oscillation Frequency

11. When the load current is light in PWM control, very narrow pulses will be outputted, and there is the possibility that some cycles may be skipped completely.

12. When the difference between V_{IN} and V_{OUT} is small, and the load current is heavy, very wide pulses will be outputted and there is the possibility that some cycles may be skipped completely.

13. If the power input pin voltage is assumed to decrease rapidly (ex. from 6.0V to 0V) at the release of the operation although delay capacitance (Cd) pin is connected, please connect an Shottky barrier diode between the power input (P_V_{DD1}) pin and the delay capacitance (Cd) pin.

14. Please connect a pull-up resistor with 100 to 200kΩ to the output pin of the voltage detector block (V_{DOUT}).

15. The delay time of the voltage detector block in heavy load may extend because of the noise of the DC/DC block. Precipitous and large voltage fluctuation at the power input pin may cause malfunction of the IC.

16. Use of the IC at voltages below the minimum operating voltage may lead the output voltage drop before achieving over current limit.

17. When P_VDD1 and P_VDD2 power supply pins and EN1 and EN2 enable pins are in undefined states, the latch protection circuit may not be reset so that the IC operation does not start correctly. Power supply and enable pins （EN1,EN2） should be grounded before starting the IC operation.
    【Undefined state conditions for each pin】
    P_V_{DD1}=P_V_{DD}2=0.1V ~ 1.2V
    V_{EN1}=V_{NE2}= 0.4V ~ 1.2V

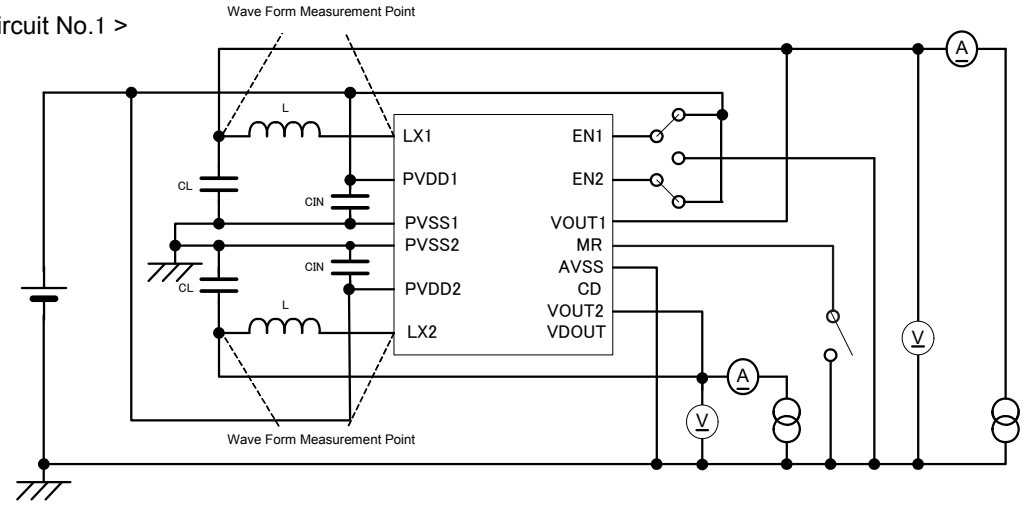
18. UVLO function works even if when V_{IN} input voltage falls below the UVLO voltage in very short time period like a few ten nanoseconds.

●Instruction on Pattern Layout

1. In order to stabilize V_{IN}'s voltage level, we recommend that a by-pass capacitor (C_{IN1} and C_{IN2}) be connected as close as possible to the P_V_{DD1} • P_V_{DD2} pins and P_V_{SS1} • P_V_{SS2} pins.
2. Please mount each external component as close to the IC as possible.
3. Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
4. Make sure that the V_{SS} traces are as thick as possible, as variations in the V_{SS} potential caused by high V_{SS} currents at the time of switching may result in instability of the DC/DC converter.

■TEST CIRCUITS

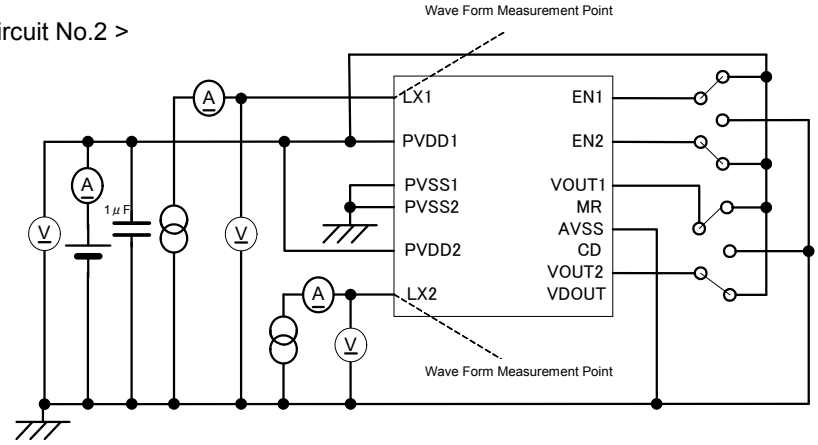
< Test Circuit No.1 >



※ External Components

L : 4.7μH(CDRH4D28C : SUMIDA)
CIN : 10μF (ceramic)
CL : 10μF (ceramic)

< Test Circuit No.2 >



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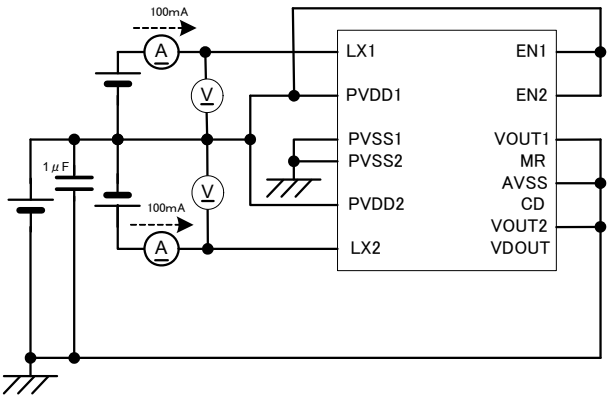

■TEST CIRCUITS (Continued)

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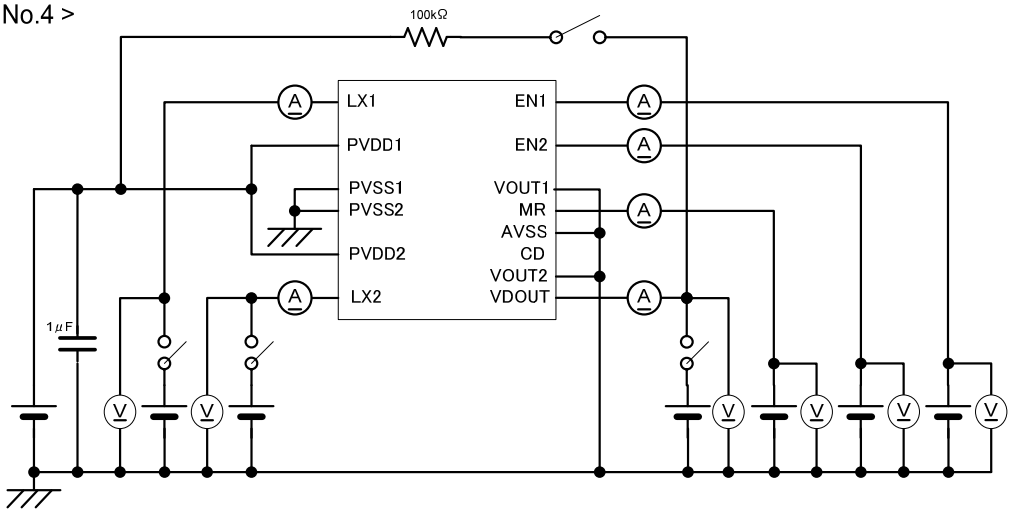

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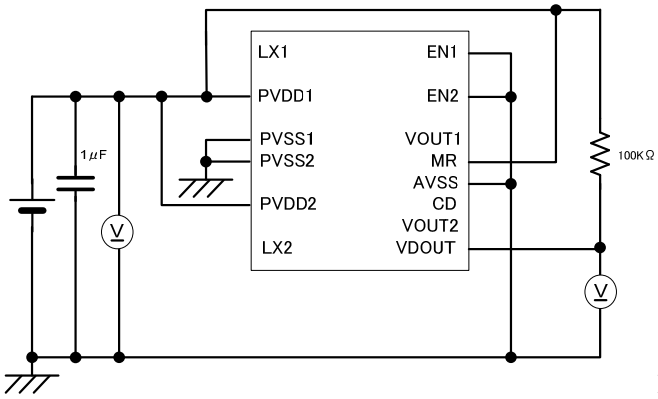

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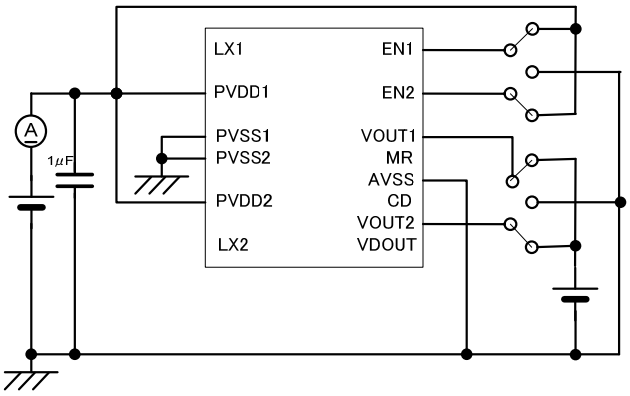

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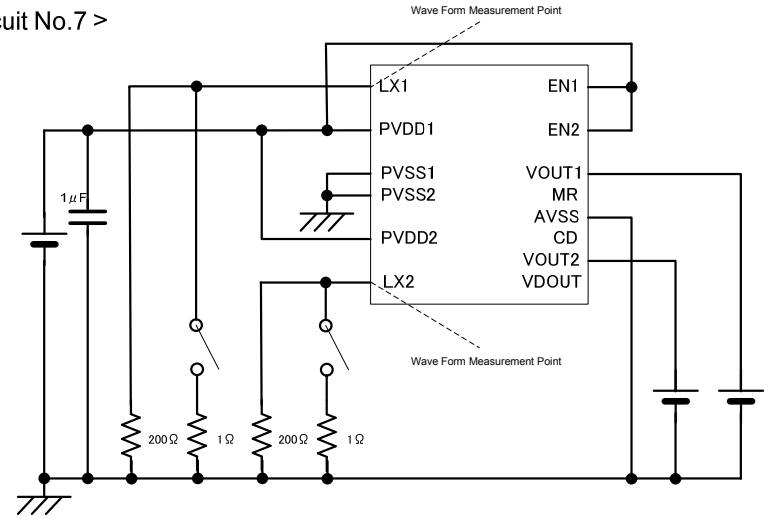
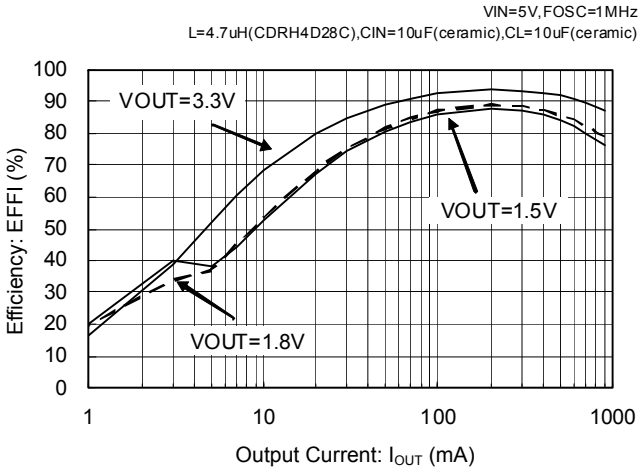
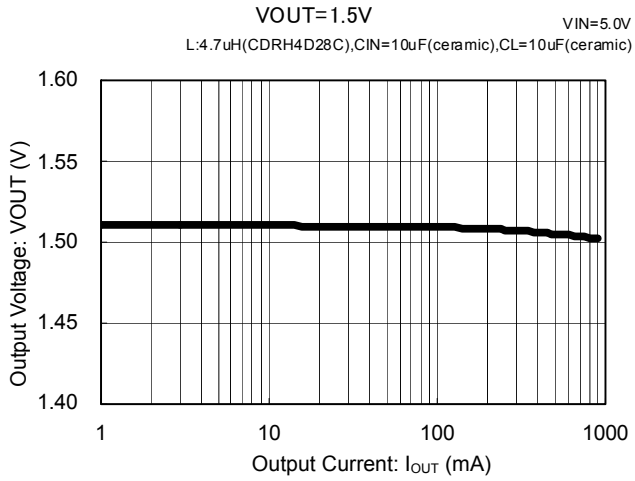


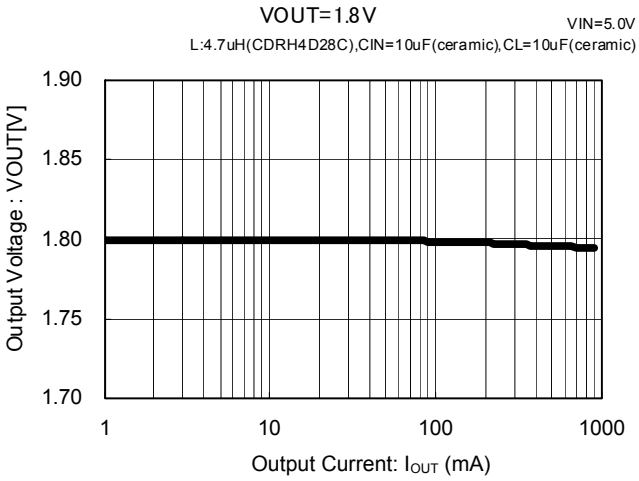
■TYPICAL PERFORMANCE CHARACTERISTICS

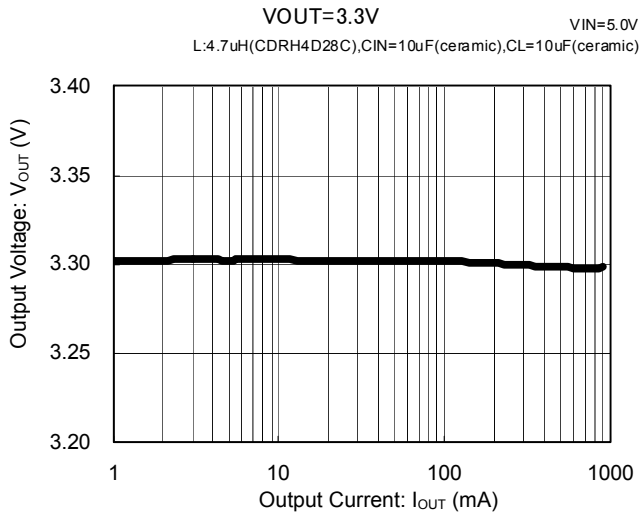
(1) Efficiency vs. Output Current



(2) Output Voltage vs. Output Current





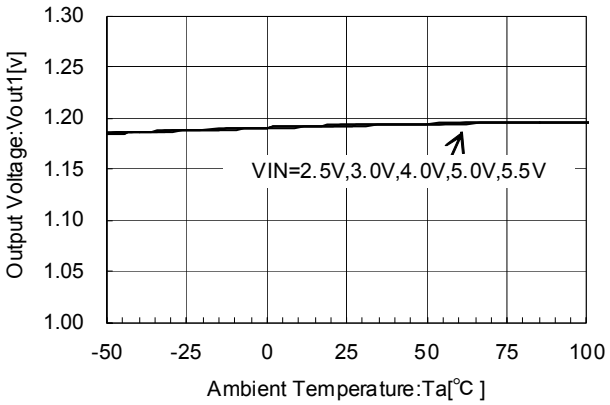


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(3) Output Voltage vs. Ambient Temperature

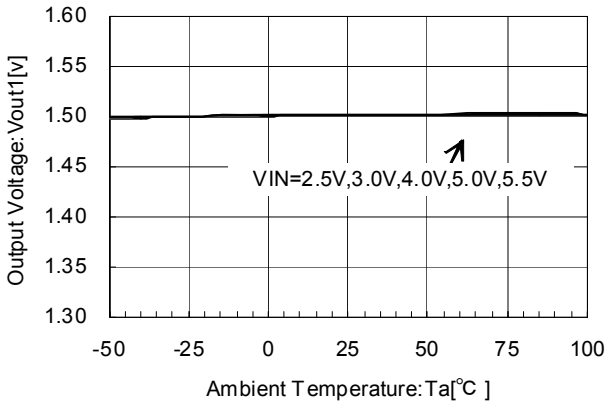
V_{OUT}=1.2V

VIN=2.5V,3.0V,4.0V,5.0V,5.5V
L:4.7uH(CDRH4D28C),CIN=10uF(ceramic),CL=10uF(ceramic)



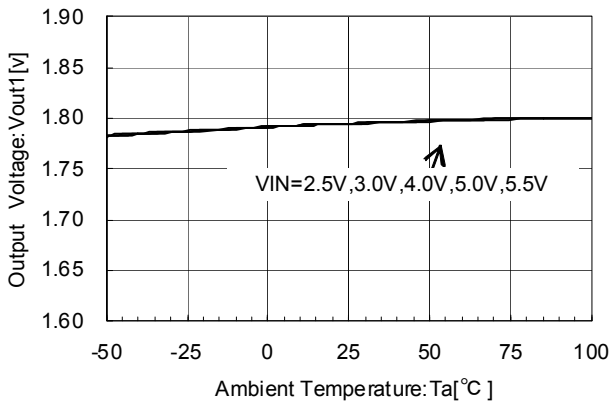
V_{OUT}=1.5V

VIN=2.5V,3.0V,4.0V,5.0V,5.5V
L:4.7uH(CDRH4D28C),CIN=10uF(ceramic),CL=10uF(ceramic)



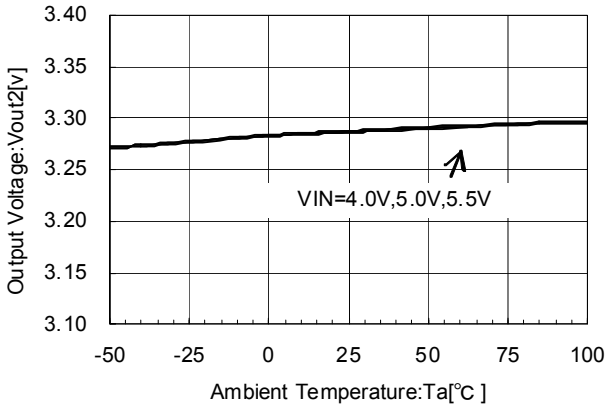
V_{OUT}=1.8V

VIN=2.5V,3.0V,4.0V,5.0V,5.5V
L:4.7uH(CDRH4D28C),CIN=10uF(ceramic),CL=10uF(ceramic)



V_{OUT}=3.3V

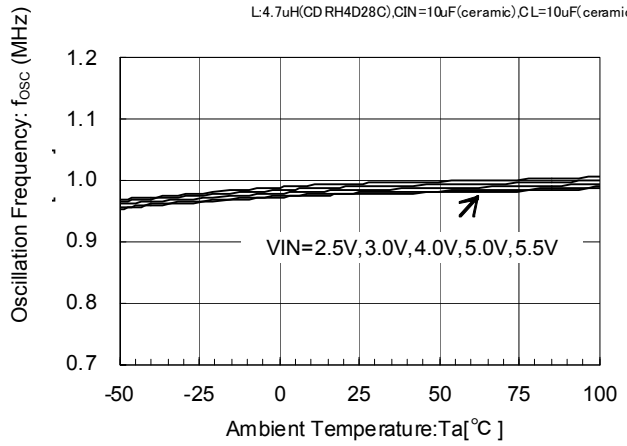
VIN=4.0V,5.0V,5.5V
L:4.7uH(CDRH4D28C),CIN=10uF(ceramic),CL=10uF(ceramic)



(4) Oscillation Frequency vs. Ambient Temperature

f_{OSC}=1MHz

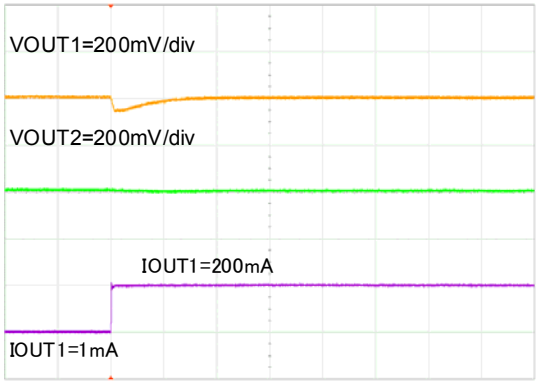
VIN=2.5V,3.0V,4.0V,5.0V,5.5V
L:4.7uH(CDRH4D28C),CIN=10uF(ceramic),CL=10uF(ceramic)



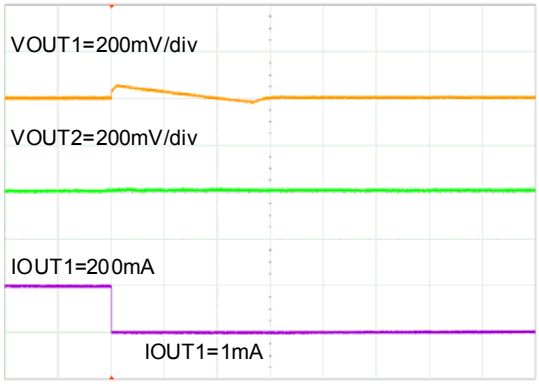
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(5) Load Transient Response

V_{IN}=5V, V_{OUT1}=1.5V, V_{OUT2}=3.3V, f_{OSC}=1MHz

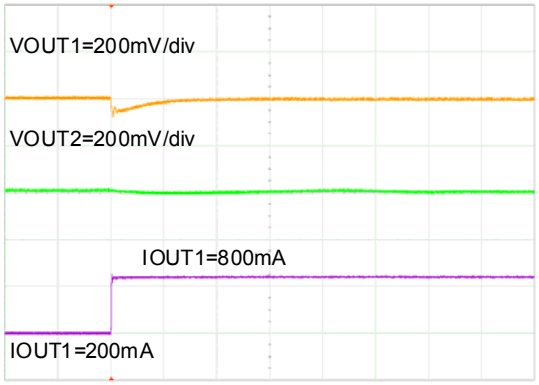


50μs/div

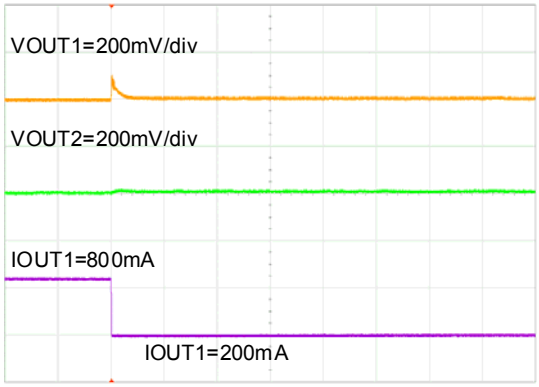


200μs/div

V_{IN}=5V, V_{OUT1}=1.5V, V_{OUT2}=3.3V, f_{OSC}=1MHz

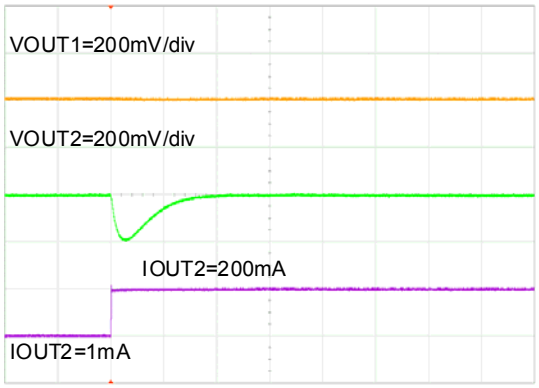


50μs/div



200μs/div

V_{IN}=5V, V_{OUT1}=1.5V, V_{OUT2}=3.3V, f_{OSC}=1MHz



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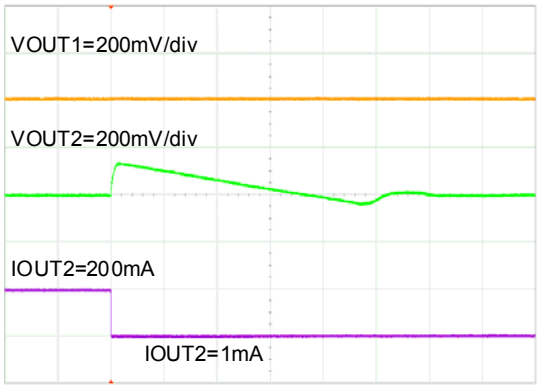
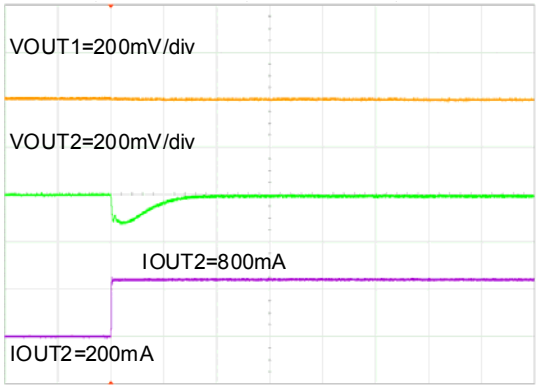
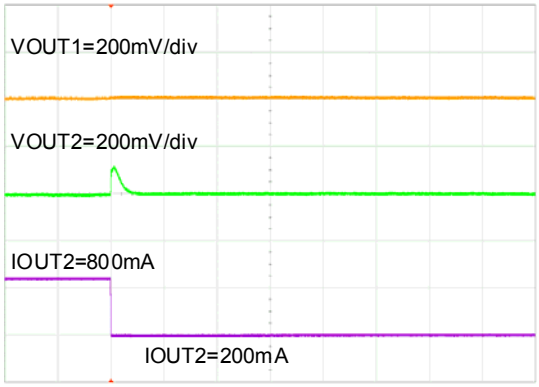


200μs/div

V_{IN}=5V, V_{OUT1}=1.5V, V_{OUT2}=3.3V, f_{OSC}=1MHz



50μs/div

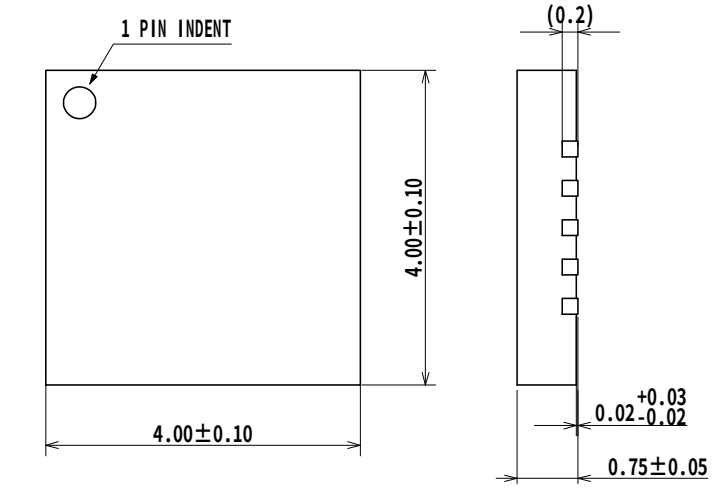


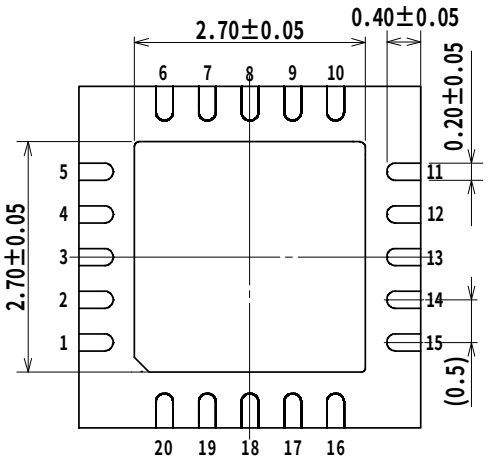
200μs/div

■PACKAGING INFORMATION

●QFN-20

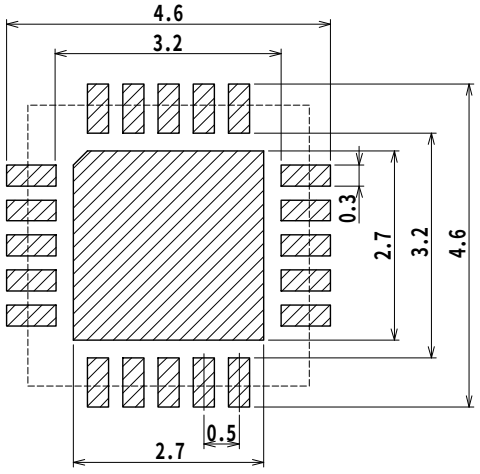
Unit: mm



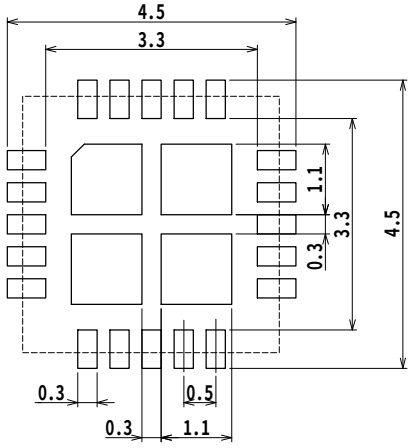


*The solder filet may not be formed because of no plating at side.

●QFN-20 Reference Pattern Layout



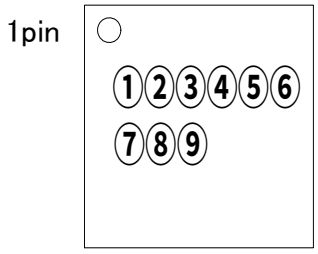
●QFN-20 Reference Metal Mask Design



Thickness of solder paste：120μm (reference)

■MARKING RULE

●QFN-20



QFN-20
(TOP VIEW)

●Standard Product

①②③Represent product series

MARK			PRODUCT SERIES
①	②	③	
5	1	5	XC9515******

④⑤⑥⑦Represents integer number of setting voltage

MARK				PRODUCT SERIES
④	⑤	⑥	⑦	
0	0	0	1	XC95150001**

⑧⑨Represents production lot number
Order of 01, …09, 10, 11, …99, 0A, …0Z, 1A, …9Z, A0, …Z9, AA, …ZZ.
(G, I, J, O, Q, W excepted)
*No character inversion used.

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