SCG6500NT Synchronous Clock Generator

PLL

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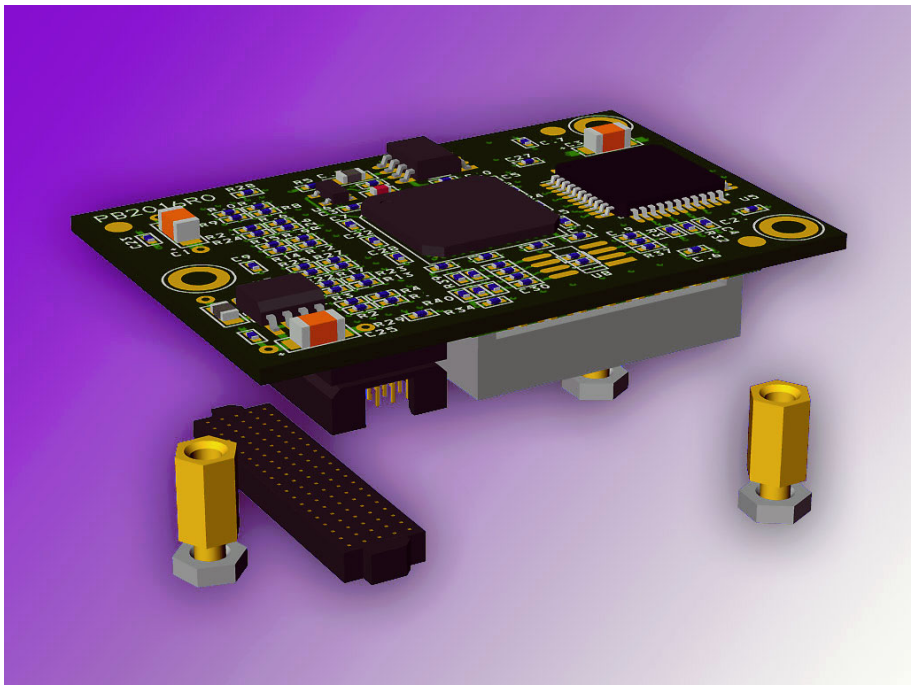

Features

- Digital PLL Control
- 622.08 MHz LVPECL Output, Ultra-low Jitter
- 155.52 MHz LVPECL Output, Ultra-low Jitter
- Two 77.76 MHz LVPECL Outputs, Low Litter
- 8 kHz LVPECL Output
- Dual 8 kHz Input References
- Supports Manual and Autonomous Modes
- 3.3 V_{DC} Power Supply

Applications

The SCG6500NT is designed for use as a reference input for OC-192 Framers and SERDES. It generates less than 1 psRMS jitter over the OC-192 bandwidth.

SCG6500NT is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization for TDM, PDH, SONET, and SDH network equipment. The SCG6500NT provides a jitter filtered, wander following output signal synchronized to a superior Stratum or peer input reference signal.

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General Description

The SCG6500NT unit provides high precision phase lock loop frequency translation for the telecommunication applications. The SCG6500NT unit generates LVPECL outputs from an intrinsically low jitter, voltage controlled crystal oscillator. The SCG6500NT unit can be configured to provide a jitter attenuated, internal reference.

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The SCG6500NT include the following features: Free Run, and alarm outputs for Loss-of-Reference, (LORA, LORB), Loss-of-Lock, (LOL). The LVPECL outputs may be put into a disable condition for external testing purposes.

The SCG6500NT is a 3.3 Volt component. The unit can be used in applications that require temperature rating of 0° - 70° C. The SCG6500NT package dimensions are 1.3" x 1.963" x 0.45" on a eight layer FR4 board with a high speed differential connector.

General Mode Description

The SCG6500NT may be operated in any one of three modes, **Manual**, **Autonomous Non-Revertive**, or **Autonomous Revertive Mode**.

In **Manual Mode**, the modules operating state is determined solely and exclusively by the Control Inputs. The SCG6500NT will unconditionally follow the Control Inputs. Proper synchronization and module operation are user responsibilities.

In **Autonomous Non-Revertive** or **Revertive Mode**, the modules operating condition is determined by the Control Inputs and the validity of the selected operational condition. The SCG6500NT will follow Control Inputs as long as the selected operating condition is valid.

In autonomous mode the module alarms are monitored to determine the validity of the current operational condition state. If the selected reference becomes invalid the module will attempt to lock to the redundant reference. If no valid references are available the module will set the internal VCXO to Hold Last if the HLV output is active. HLV is a signal indicating that there is a Hold Last value present. The module will set the internal VCXO to Free Run if references A & B are invalid and the HLV output is not active.

For example, the Control Inputs are set to lock to REFA and no alarms are active. The user then sets the Control Inputs to lock to REFB but the LORB alarm is active. The module will remain in lock to REFA. Autonomous mode establishes absolute preference for valid operating conditions; REFA is valid; REFB, though selected, is invalid; the module remains in lock to the valid reference, REFA.

**Note the module doesn't assume responsibility for reference qualification.*

Reference qualification is a user responsibility. The module only verifies that a signal is present but cannot check for Stratum quality. A signal must be present for 10 seconds before the module considers it a valid reference.

In **Autonomous Revertive Mode**, the Control Inputs set a preferred reference. The module will revert to the preferred reference as long as it is considered valid.

In **Autonomous Non-Revertive Mode**, there is no preferred reference. The module will remain on a reference as long as it is considered valid.

Mode Inputs

Table 1

Mode1	Mode 0	Mode
0	X	Manual
1	0	Autonomous Non-Revertive
1	1	Autonomous Revertive

Module Reset

Table 2

Reset	Description
0	Normal Operation
1	Module Reset to power on condition

Control Descriptions

Free Run is an operational state that sets the module output to a nominal frequency.

Lock to Reference A or B is an operational state that phase locks the module output to the respective reference.

Hold Last is an operational state that sets the module output to a previous loop frequency. The value stored in the Hold Last latch is updated once every second.

Table 3 Control Inputs

CTL1	CTL0	Operational Condition
0	0	Free Run
0	1	Lock to Reference A
1	0	Lock to Reference B
1	1	Hold Last

Status Output Descriptions

Control Status Outputs, used to report the current control of the module in both Manual and Autonomous Modes. In Manual Mode the Control Status Outputs reflect the Control Inputs. In Autonomous Mode the Control Status Outputs may be different than the Control Inputs depending on circumstances. When the internal state machine acknowledges the need for a change in control it updates the Control Status Outputs on the next internal clock cycle of 12.86 ns.

Table 4 Control Status Outputs

CS1	CS0	Current Operational Status
0	0	Free Run
0	1	Lock to Reference A
1	0	Lock to Reference B
1	1	Hold Last

Hold Last Valid, used to report that a lock value has been entered into the Hold Last register. In Autonomous Mode the Hold Last Valid output is used to restrict the entry into Hold Last.

Table 5 Hold Last Valid Output

HLV	Description
0	Hold Last Invalid
1	Hold Last Valid

LORA and LORB, used to report that no signal is present on respective reference. LOR alarms are missing pulse detectors and don't indicate frequency out of range. In Autonomous Mode an LOR alarm is blanked to the internal state machine for ten seconds after alarm transitions to non-alarm state. External LOR alarms outputs are not blanked.

Table 6 LORA or LORB Outputs

LORA or LORB	Description
0	No Alarm
1	Loss of Reference

LOL, used to report that the reference is greater than 94° out of phase with the VCXO. LOL alarm is only valid in a lock state (i.e. Lock to Reference A). In Autonomous Mode the LOL is used to start a ten second qualification timer on the respective reference. Once the timer expirers the respective reference is considered valid by the internal state machine.

Table 7 LOL Output

LOL	Description
0	No Alarm
1	Loss of Lock

Output Enable Settings

ENQ1, ENQ2, ENQ3, ENQ4, and **ENQ5** are used to enable and disable the respective output. Logic low on the **ENQ** pin will enable the output. Logic high on the **ENQ** pin will state lock the output.

Table 8 Enable Control Inputs

ENQ#	Output State
0	Enabled
1	State Locked

Absolute Maximum Rating

Table 9

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vcc	Power Supply Voltage	-0.5	-	4.0	Volts	1.0
Vi	Input Voltage	-0.5	-	4.0	Volts	1.0
Ts	Storage Temperature	-40	-	100	°C	1.0

Specifications

Table 10

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{CC}	Power supply voltage	3.125	3.3	3.465	V	2.0
I_{CC}	Power supply current	-	400	TBD	mA	
T_O	Temperature Range	0	-	70	°C	
f_{FR}	Free Run Accuracy	-20	-	20	ppm	
f_{RefA}	Input Reference A	-	8	-	kHz	
f_{RefB}	Input Reference B	-	8	-	kHz	
f_{CAP}	Capture/Pull-in Range	-25	-	25	ppm	
f_{BW}	Jitter Filter Bandwidth	1	3.6	10	Hz	3.0
t_{AQ}	Acquisition Time	-	200	-	ms	4.0
t_{RF}	Output Rise and Fall Time (20%-80%)					
	@622.08 MHz	-	250	-	ps	5.0
	@155.52 MHz	-	300	-	ps	5.0
	@77.76 MHz	-	-	1	ns	5.0
DC	Output Duty Cycle	45	50	55	%	
J_{GEN}	Jitter Generation					
	@622.08 MHz	-	-	0.8	psRMS	6.0
	@155.52 MHz	-	-	1	psRMS	7.0
	@77.76 MHz	-	-	4	psRMS	8.0
J_{PK}	Jitter Transfer Peaking	-	0.1	0.2	dB	
$MTIE_{SR}$	MTIE@Sychronization Rearrangement	-	6	-	ns	

NOTES:
1.0: Operation of the device at these or any other condition beyond those listed under Operating Specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.
2.0: Requires external Regulation and supply decoupling (2.2 uF, 330 pF)
3.0: 3dB loop response
4.0: From a 20 ppm step in reference frequency
5.0: See Recommended Line Termination for load requirements
6.0: Jitter based on SONET OC-192 bandwidth (12 kHz to 80 MHz)
7.0: Jitter based on SONET OC-48 bandwidth (12 kHz to 20 MHz)
8.0: Jitter based on SONET OC-12 bandwidth (12 kHz to 5 MHz)

Input And Output Characteristics

Table 11

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
LVTTL Input and Output Characteristics						
V_{IH}	High Level Input Voltage	2	-	3.6	V	
V_{IL}	Low Level Input Voltage	0	-	0.8	V	
T_{IO}	I/O to Output Valid	-	-	10	nS	
C_O	Output Capacitance	-	-	10	pF	
V_{OH}	High Level Output Voltage, I_{OH} = 04mA	2.4	-	-	V	Vcc Min.
V_{OL}	Low Level Output Voltage, I_{OL} = 8mA	-	-	0.4	V	Vcc Max.
T_{IR}	Input Reference Signal Pulse Width	25.72	-	-	nS	
LVPECL Output Characteristics for Q1 & Q2						
V_{OH}	High Level Output Voltage	2.27	-	2.52	V	
V_{OL}	Low Level Output Voltage	1.49	-	1.68	V	
C_I	Output Capacitance	-	-	10	pF	
T_{skew}	Differential output skew	-	-	50	ps	
LVPECL Output Characteristics for Q3, Q4 & Q5						
V_{OH}	High Level Output Voltage	-	2.48	-	V	
V_{OL}	Low Level Output Voltage	-	0.96	-	V	
C_I	Output Capacitance	-	-	10	pF	
T_{skew}	Differential output skew	-	-	50	ps	

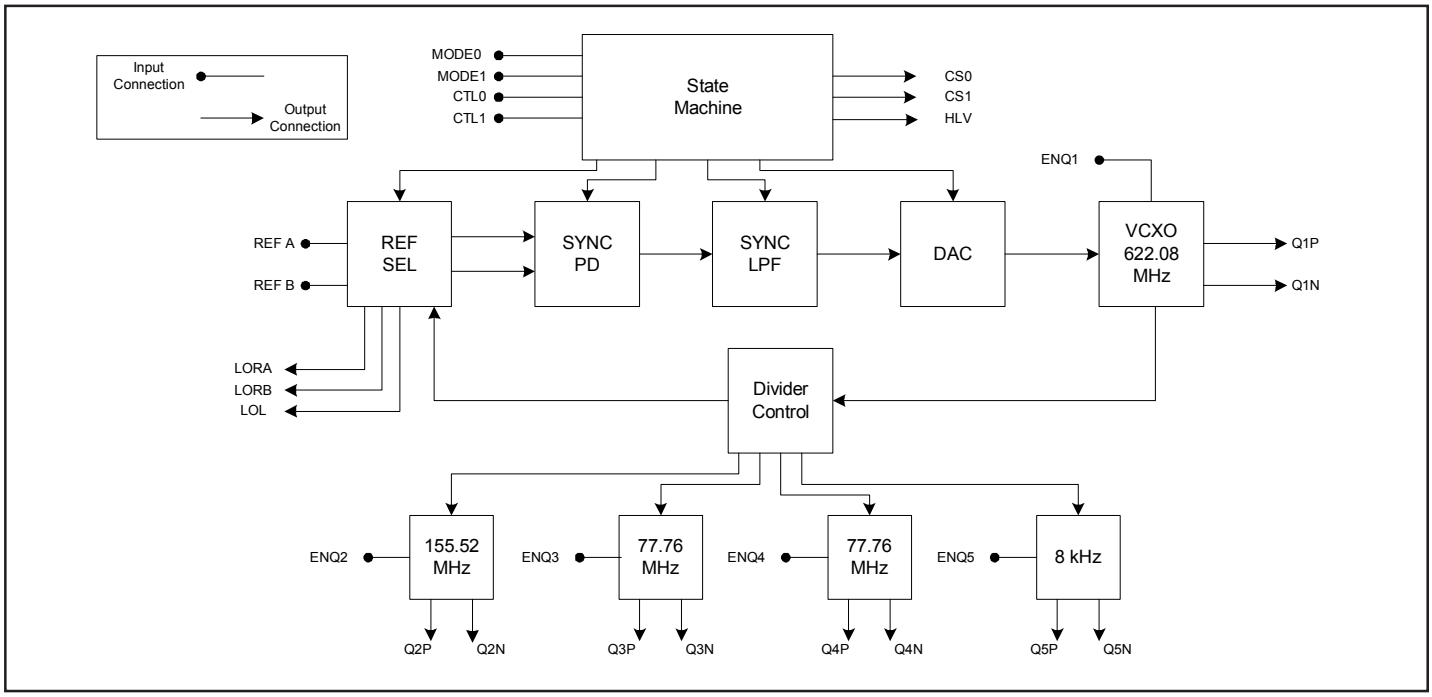
Pin Description

Table 12

Pin #	Pin Name	Description	Input Default State
3,8,13,18, 23,28,33,38, 43,48,53,58, 63,68,73,78, 83,88,93,98	V_{CC}	Supply voltage relative to ground	N/A
1,2,5,7,9, 10,12,16,17, 22,27,31,32, 37,42,46,47, 51,52,57,62, 66,67,72,77, 81,82,87,92, 94,95,96,97,100	GND	Ground	N/A
55	MODE0	Mode Input	Logic 0
75	MODE1	Mode Input	Logic 0
70	CTL0	Control Input	Logic 0
74	CTL1	Control Input	Logic 0
30	RESET	Reset module to power on conditions	Logic 0
15	ENQ1	Active low enable Q1	Logic 0
19	ENQ2	Active low enable Q2	Logic 0
79	ENQ3	Active low enable Q3	Logic 0
60	ENQ4	Active low enable Q4	Logic 0
34	ENQ5	Active low enable Q5	Logic 0
99	REFA	Input reference	N/A
4	REFB	Input reference	N/A
69	CS0	Control Operational Status	N/A
64	CS1	Control Operational Status	N/A
54	HLV	Hold Last Valid	N/A
65	LOL	Loss-of-Lock “Active Reference”	N/A
45	LORA	Loss-of-Reference A	N/A
39	LORB	Loss-of-Reference B	N/A
11	Q1P	Positive LVPECL Differential Output	N/A
6	Q1N	Negative LVPECL Differential Output	N/A
21	Q2P	Positive LVPECL Differential Output	N/A
26	Q2N	Negative LVPECL Differential Output	N/A
36	Q3P	Positive LVPECL Differential Output	N/A
41	Q3N	Negative LVPECL Differential Output	N/A
71	Q4P	Positive LVPECL Differential Output	N/A
76	Q4N	Negative LVPECL Differential Output	N/A
56	Q5P	Positive LVPECL Differential Output	N/A
61	Q5N	Negative LVPECL Differential Output	N/A
84,85, 89,90	JTAG	No connection. Do not connect. Do not connect. No BSDL files available	
14,20,24,25 29,35,40,44, 49,50,59,80,86,91	NC	No connection. Do not connect	

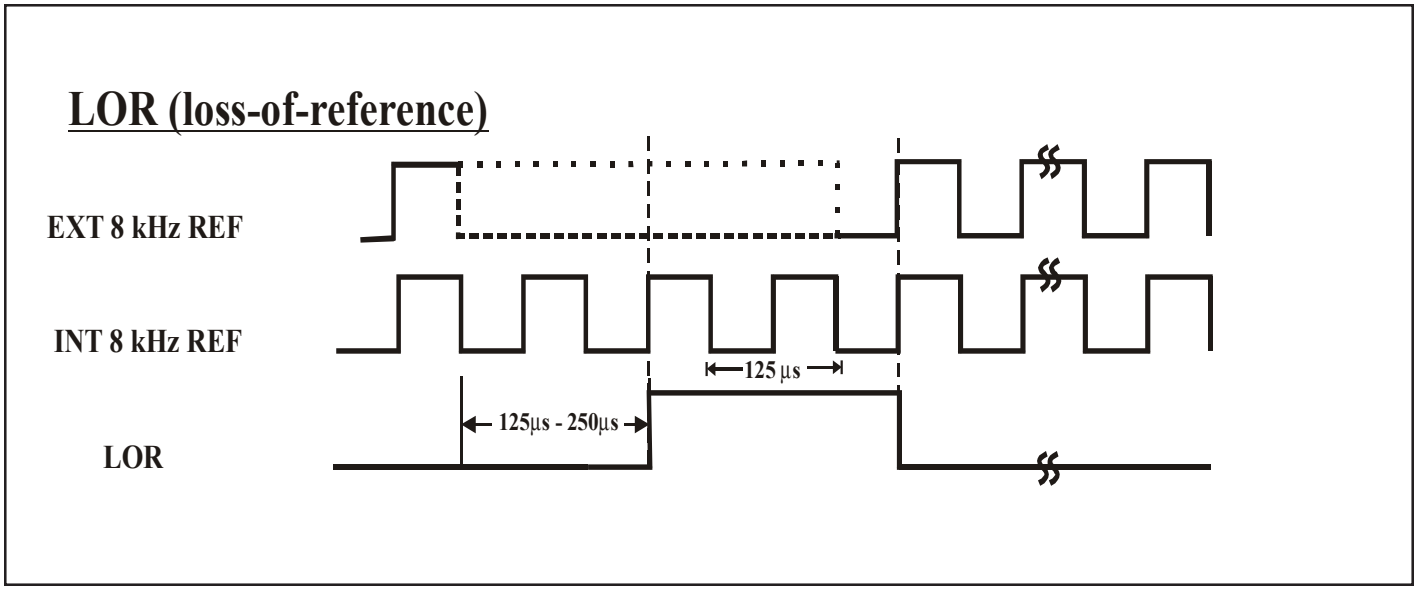
Functional Block Diagram

Figure 1



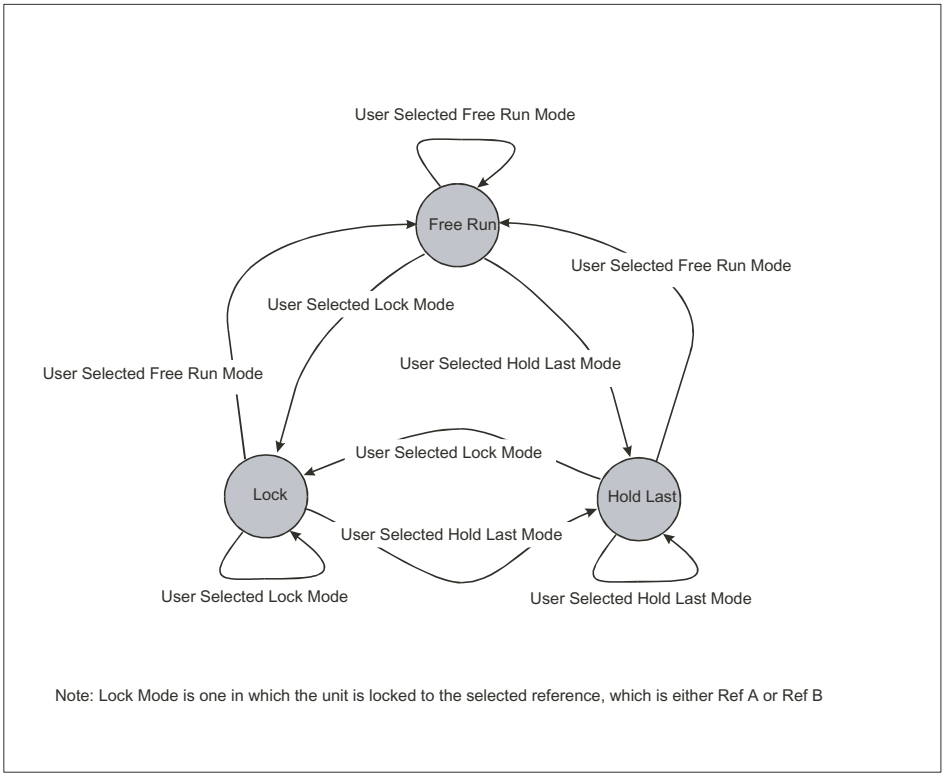
Loss of Reference Timing Diagram

Figure 2



Manual Mode State Machine

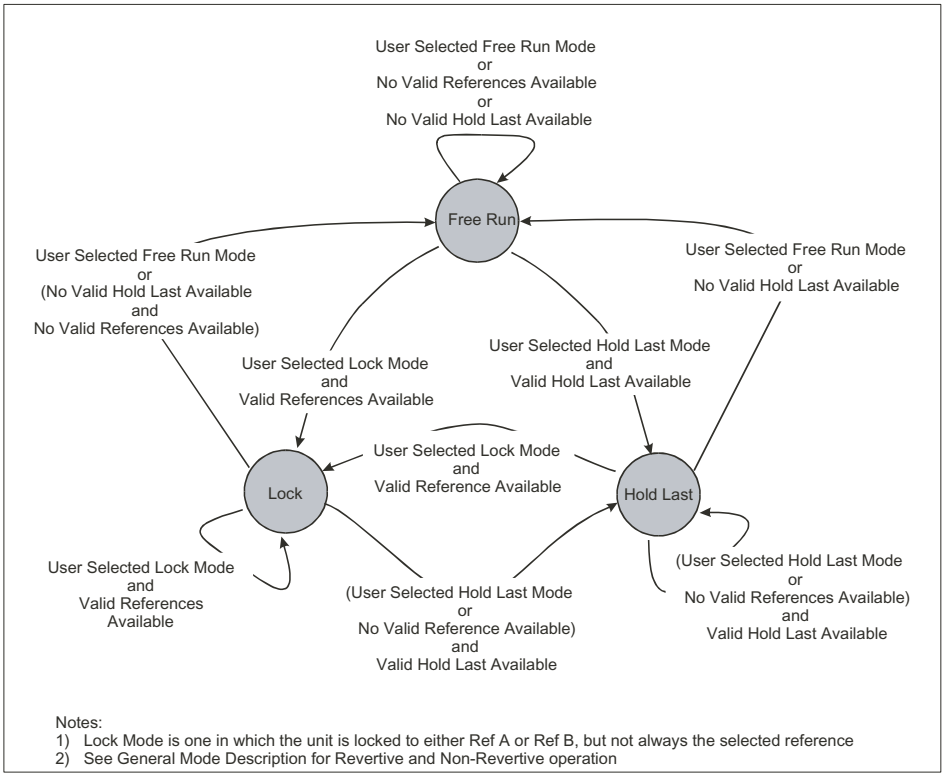
Figure 3



Note: Lock Mode is one in which the unit is locked to the selected reference, which is either Ref A or Ref B

Autonomous Mode State Machine

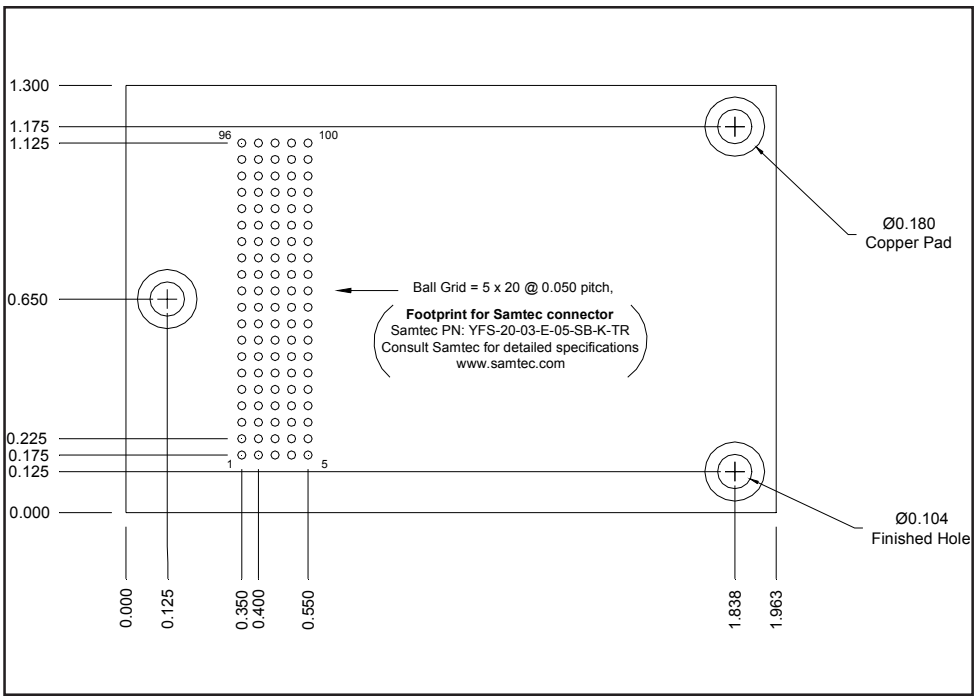
Figure 4



Notes:
1) Lock Mode is one in which the unit is locked to either Ref A or Ref B, but not always the selected reference
2) See General Mode Description for Revertive and Non-Revertive operation

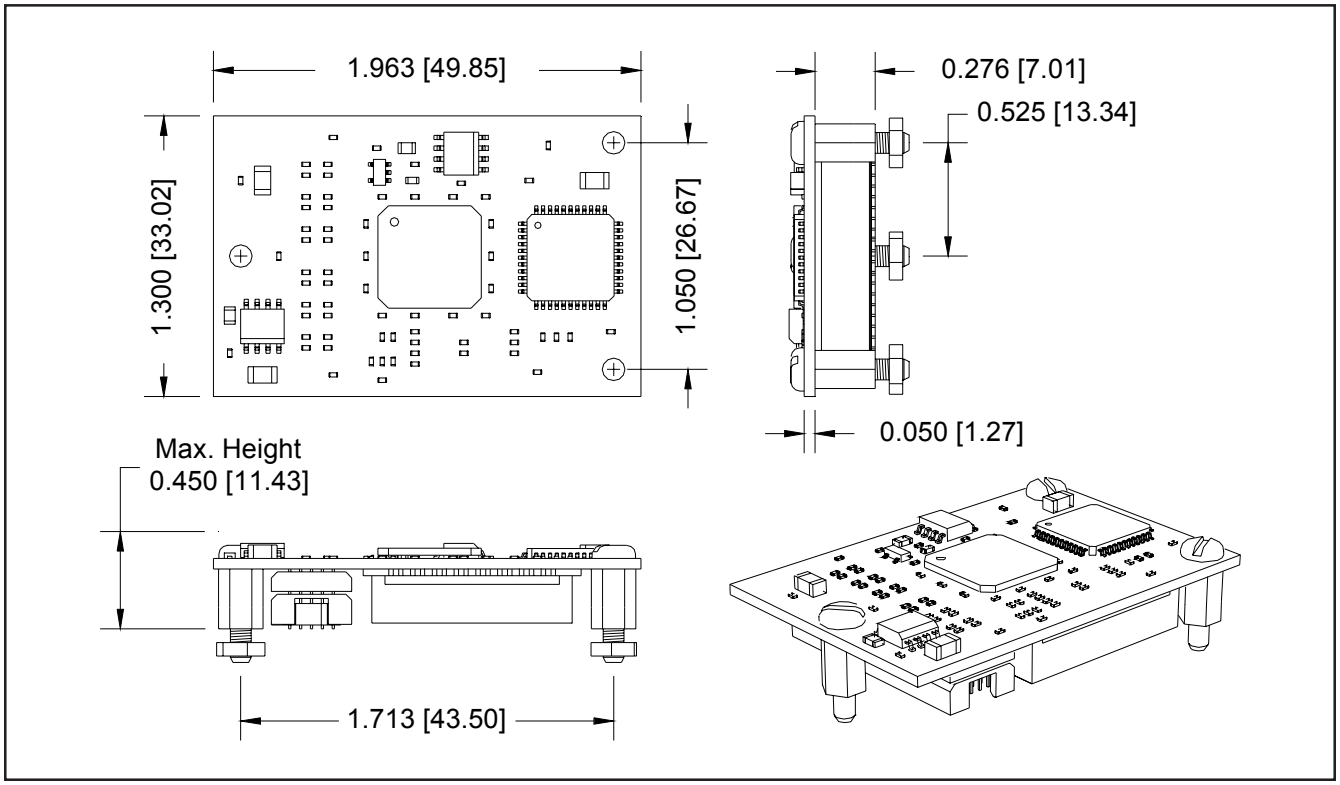
Recommended Connector Placement and Component Keep Out Area

Figure 5



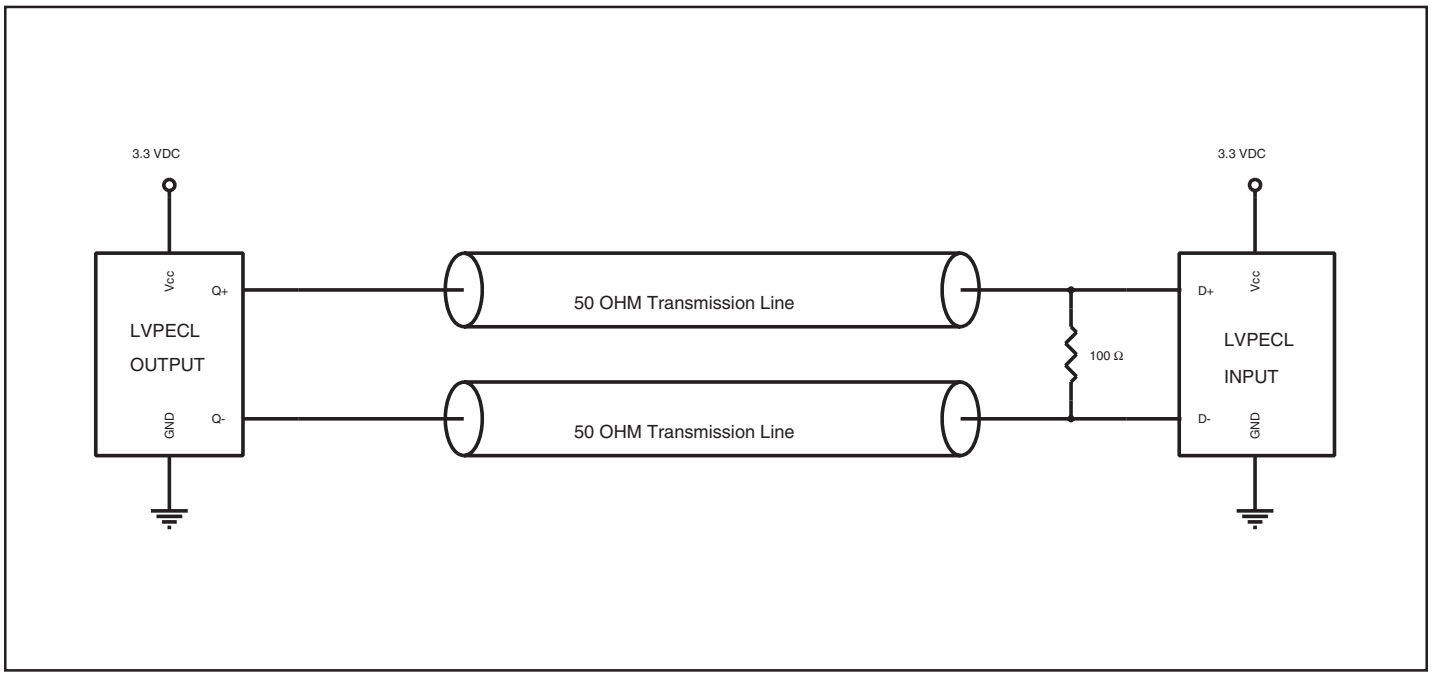
Maximum Dimensions

Figure 6



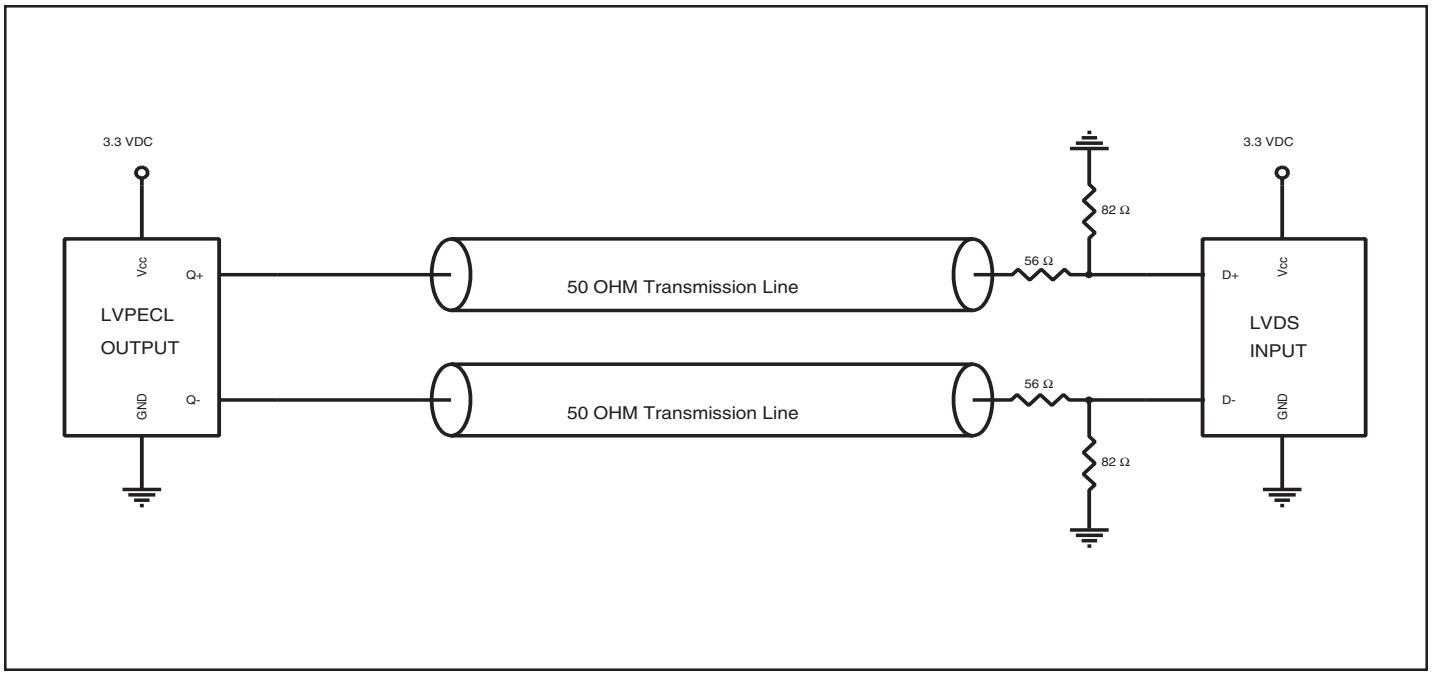
Recommended Line Termination

Figure 7



Recommended LVPECL to LVDS Conversion for Q1 & Q2

Figure 8



Revision	Revision DateNote	
A00	7/20/01	Advance Informational Release
A01	7/24/01	Added Samtec Connector PN
A02	7/30/01	Changed Pin outs
A03	12/03/01	Updated Pin Descriptions
A04	12/10/01	Made correction to diagrams
A05	6/24/02	Added Table 2, Module Reset

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Advance Data Sheet