



STL75NH3LL

N-channel 30 V, 0.004 Ω , 20 A, PowerFLAT™ (6x5)
ultra low gate charge STripFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on) max}	I _D
STL75NH3LL	30V	< 0.0057 Ω	20 A ⁽¹⁾

1. This value is according R_{thj-pcb}

- Improved die-to-footprint ratio
- Very low profile package (1mm max)
- Very low thermal resistance
- Very low gate charge
- Low threshold device

Application

- Switching applications

Description

This application specific Power MOSFET is the latest generation of STMicroelectronics unique “STripFET™” technology. The resulting transistor is optimized for low on-resistance and minimal gate charge. The chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

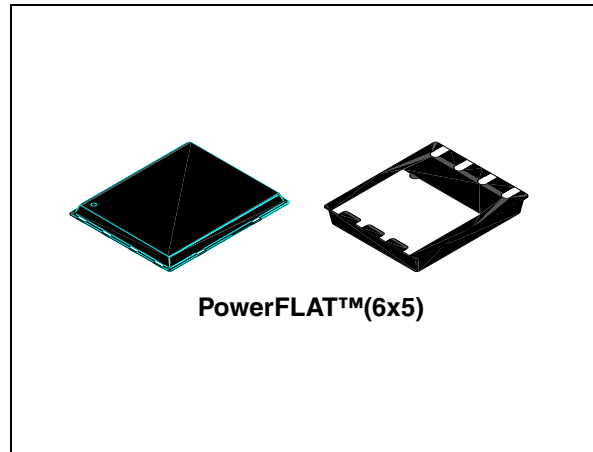


Figure 1. Internal schematic diagram

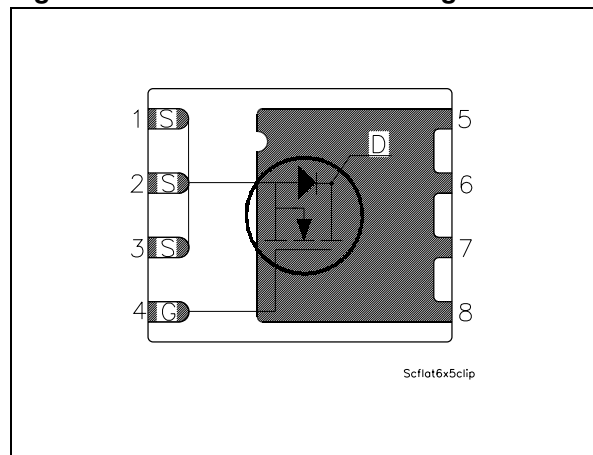


Table 1. Device summary

Order code	Marking	Package	Packaging
STL75NH3LL	L75NH3LL	PowerFLAT™ (6 x 5)	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate-source voltage	± 16	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	75	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	47	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	20	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	12.5	A
$I_{DM}^{(3)}$	Drain current (pulsed)	80	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	60	W
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	4	W
	Derating factor	0.03	W/ $^\circ\text{C}$
T_j	Operating junction temperature	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature		

1. The value is rated according R_{thj-c}
2. This value is according $R_{thj-pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain) max	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	31.3	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch^2 , 2 oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating}, @ 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{DS} = \pm 16 V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 10 A$ $V_{GS} = 4.5 V, I_D = 10 A$		0.004 0.005	0.0057 0.0075	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25 V, f = 1 \text{ MHz},$ $V_{GS} = 0$		1810		pF
C_{oss}	Output capacitance			565		pF
C_{rss}	Reverse transfer capacitance			41		pF
Q_g	Total gate charge	$V_{DD} = 15 V, I_D = 20 A,$ $V_{GS} = 4.5 V$ <i>(see Figure 14)</i>		18	24	nC
Q_{gs}	Gate-source charge			4.8		nC
Q_{gd}	Gate-drain charge			5.3		nC
R_G	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain	0.5	1.5	3	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD} = 15\text{ V}$, $I_D = 10\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16)		8 65		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD} = 15\text{ V}$, $I_D = 10\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16)		30 20		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				20	A
I_{SDM}	Source-drain current (pulsed)				80	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 20\text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		22		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 20\text{ V}$		32		nC
I_{RRM}	Reverse recovery current	(see Figure 15)		1.9		A

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

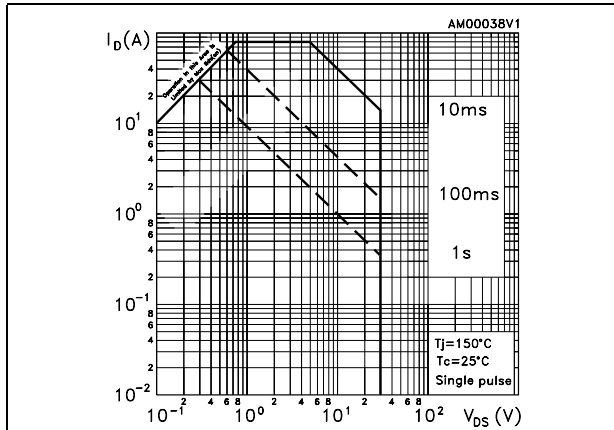


Figure 3. Thermal impedance

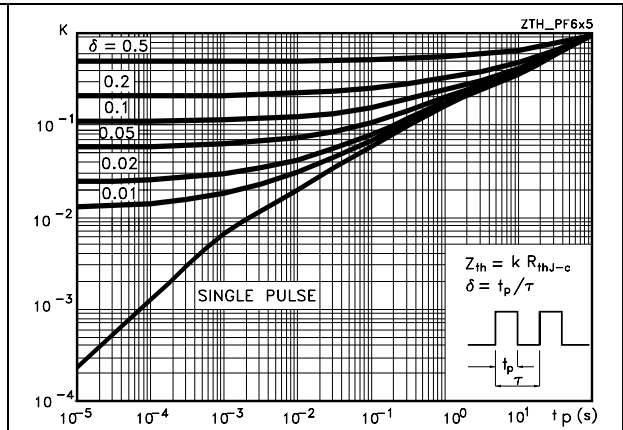


Figure 4. Output characteristics

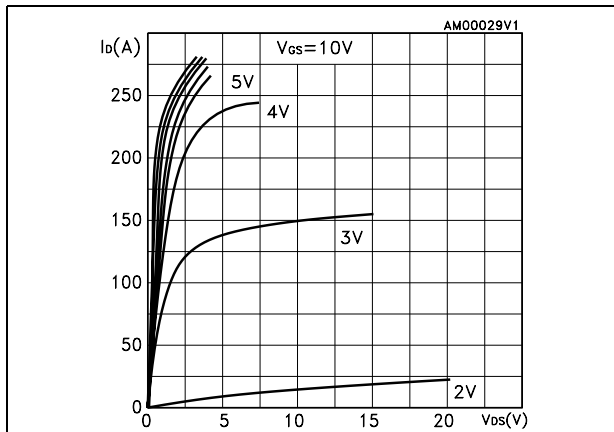


Figure 5. Transfer characteristics

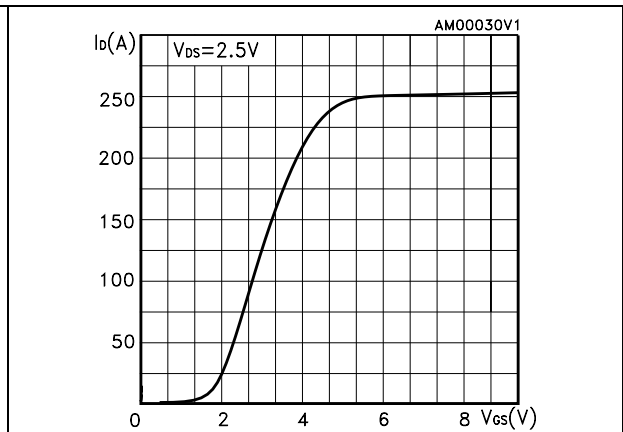


Figure 6. Normalized $B_{V_{DS}}$ vs temperature

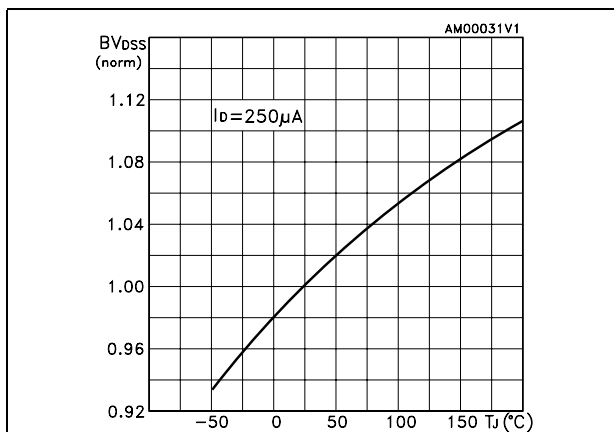


Figure 7. Static drain-source on resistance

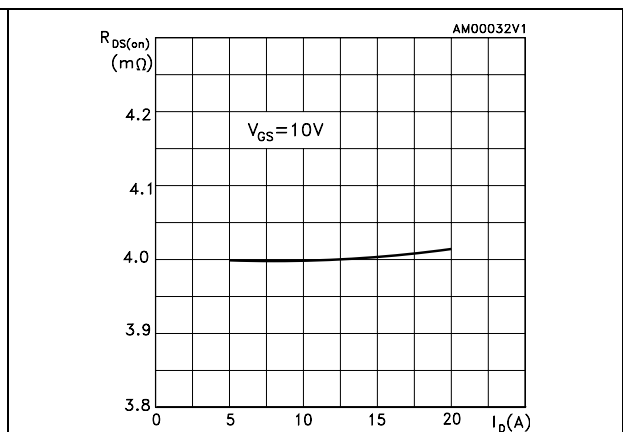


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

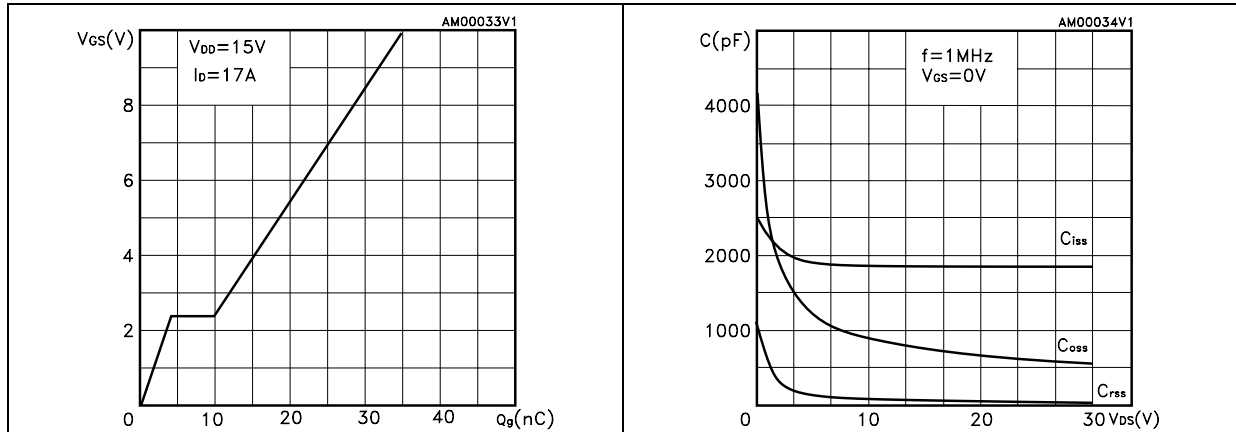


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

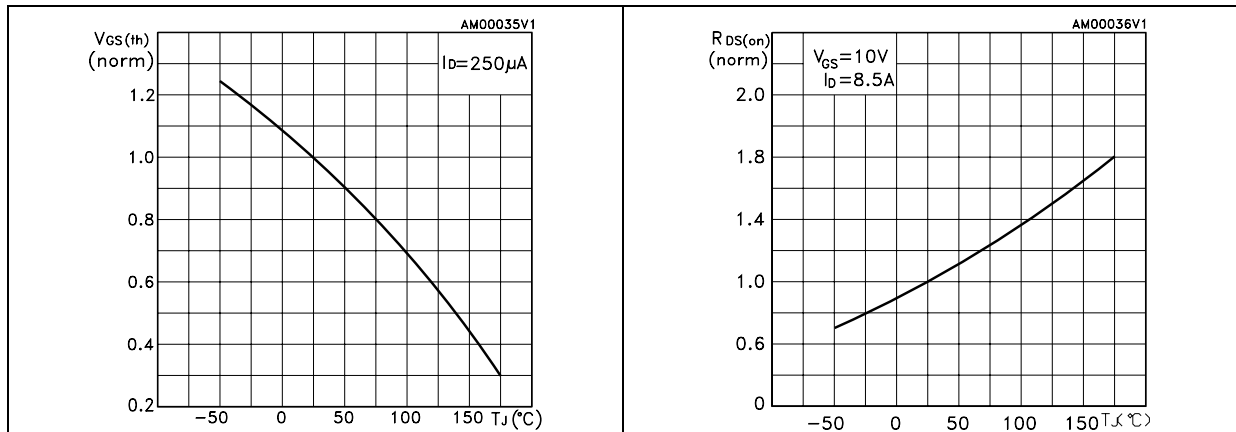
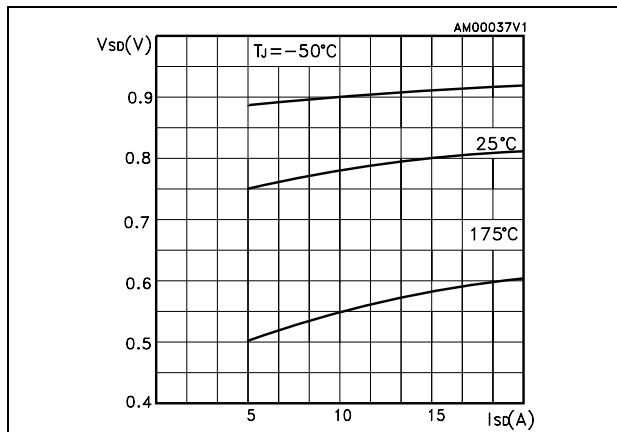


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

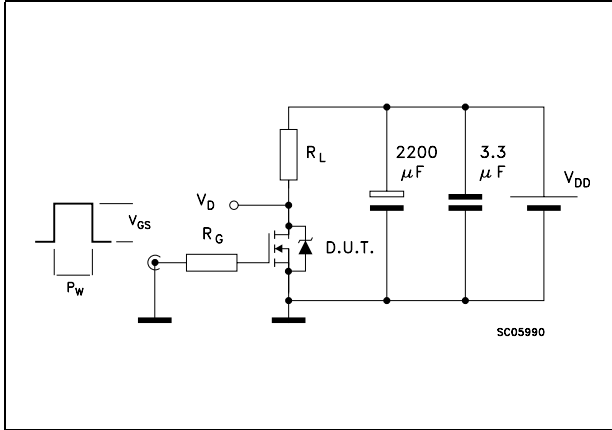


Figure 14. Gate charge test circuit

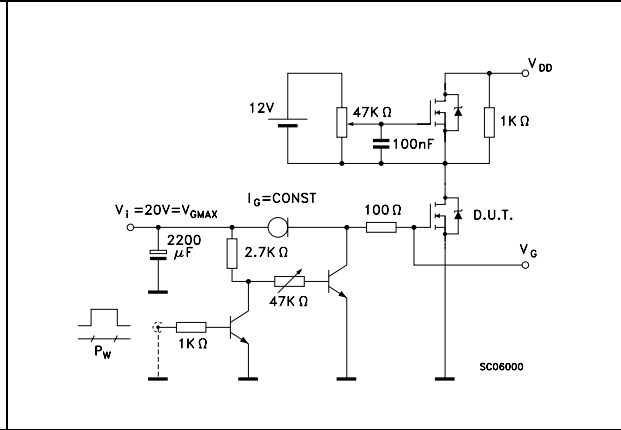


Figure 15. Test circuit for inductive load switching and diode recovery times

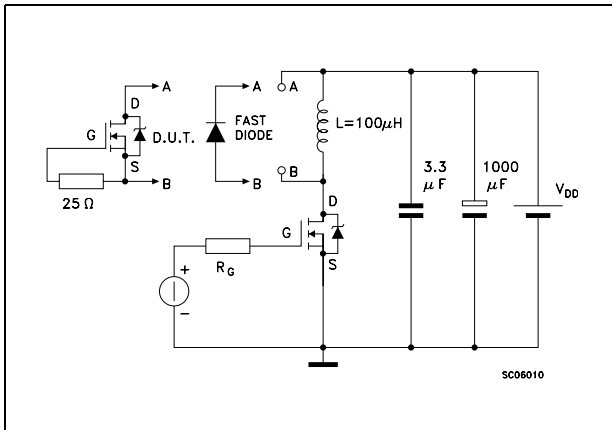


Figure 16. Unclamped inductive load test circuit

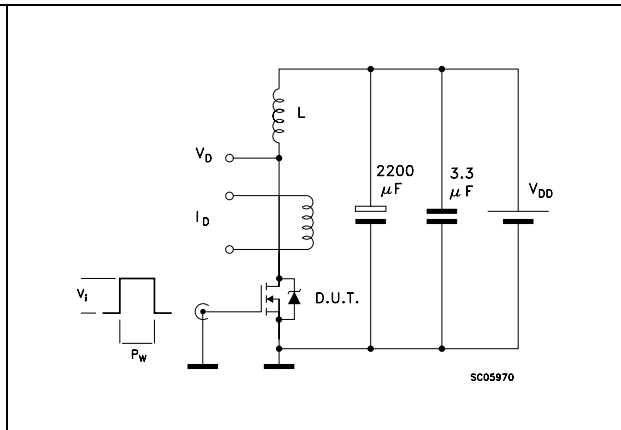


Figure 17. Unclamped inductive waveform

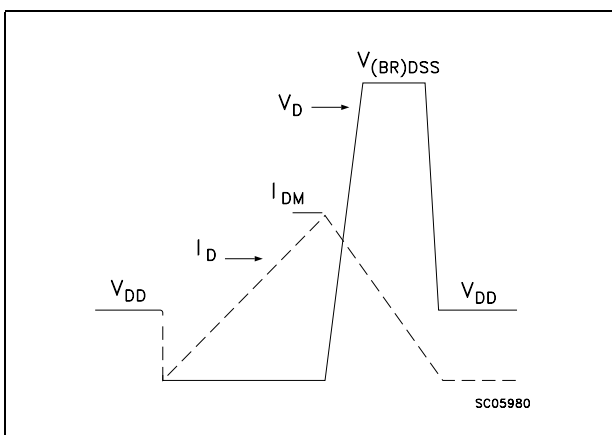
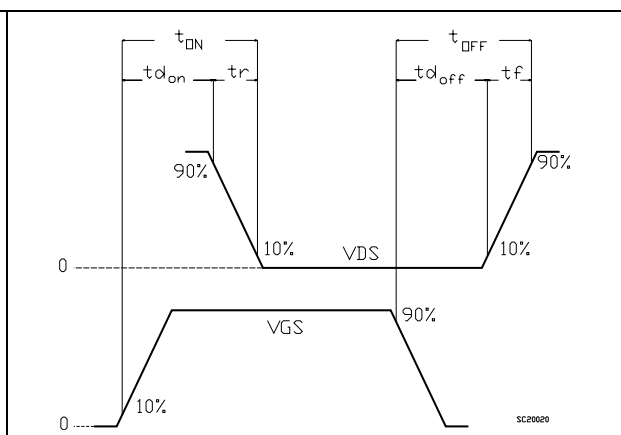


Figure 18. Switching time waveform

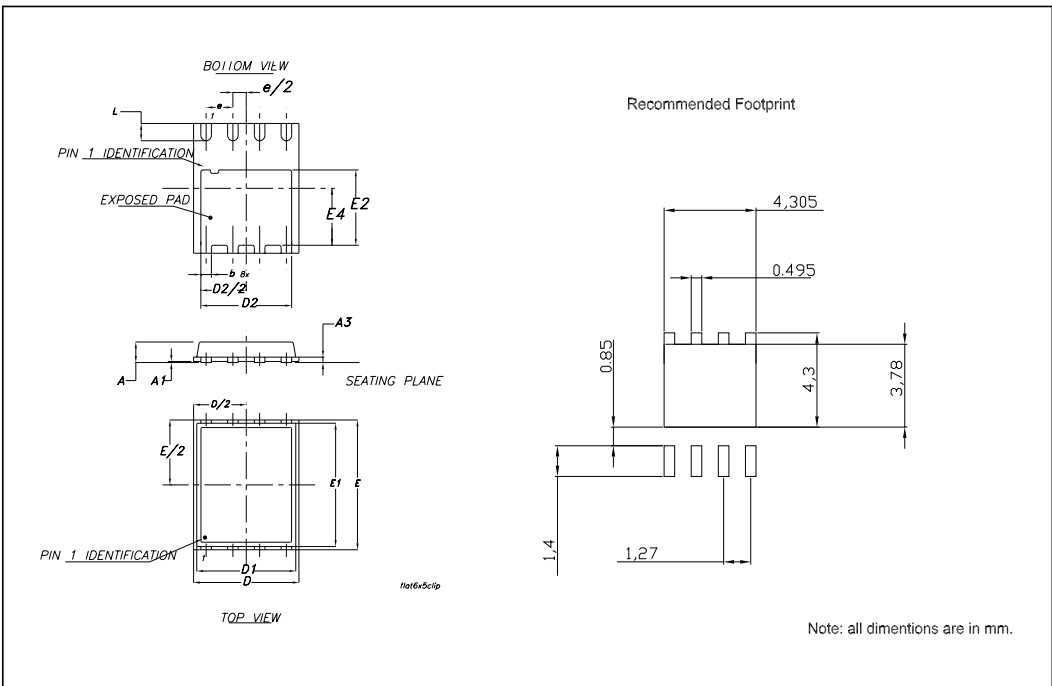


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

PowerFLAT™ (6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
12-Jun-2008	1	First release

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