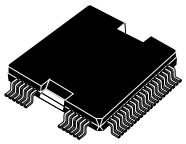
TDA7571

STPDACsw - Fully digital high efficiency power audio amplifier

Features

- Output power 2 x 70W / 1 x 250W @ THD<1%
- I^2S input (F_S = 38 to 48kHz)
- PWM output ($F_{PWM} = F_S$ x 8)
- MCLK input = 256 x F_S
- Operation on 24bit
- ±30V supply voltage (Max.)
- St-by
- Mute
- Stereo/bridge operation selection
- Protections against short circuit across the load
- Chip thermal protection
- External temperature sensor possibility
- Thermal warning pins
- Adjustable clip detector pin



HiQUAD-64

The maximum output current and voltage swing are depending by the output circuitry (power supply, external power transistors and sensing resistors). The device can work as a stereo single-ended channels or a mono bridge power amplifier.

Description

The TDA7571 i is a fully digital switchmode power audio amplifier with I^2S digital input and PWM output.

Table 1. Device summary

Order code	Package	Packing
TDA7571	HiQUAD-64	Tray

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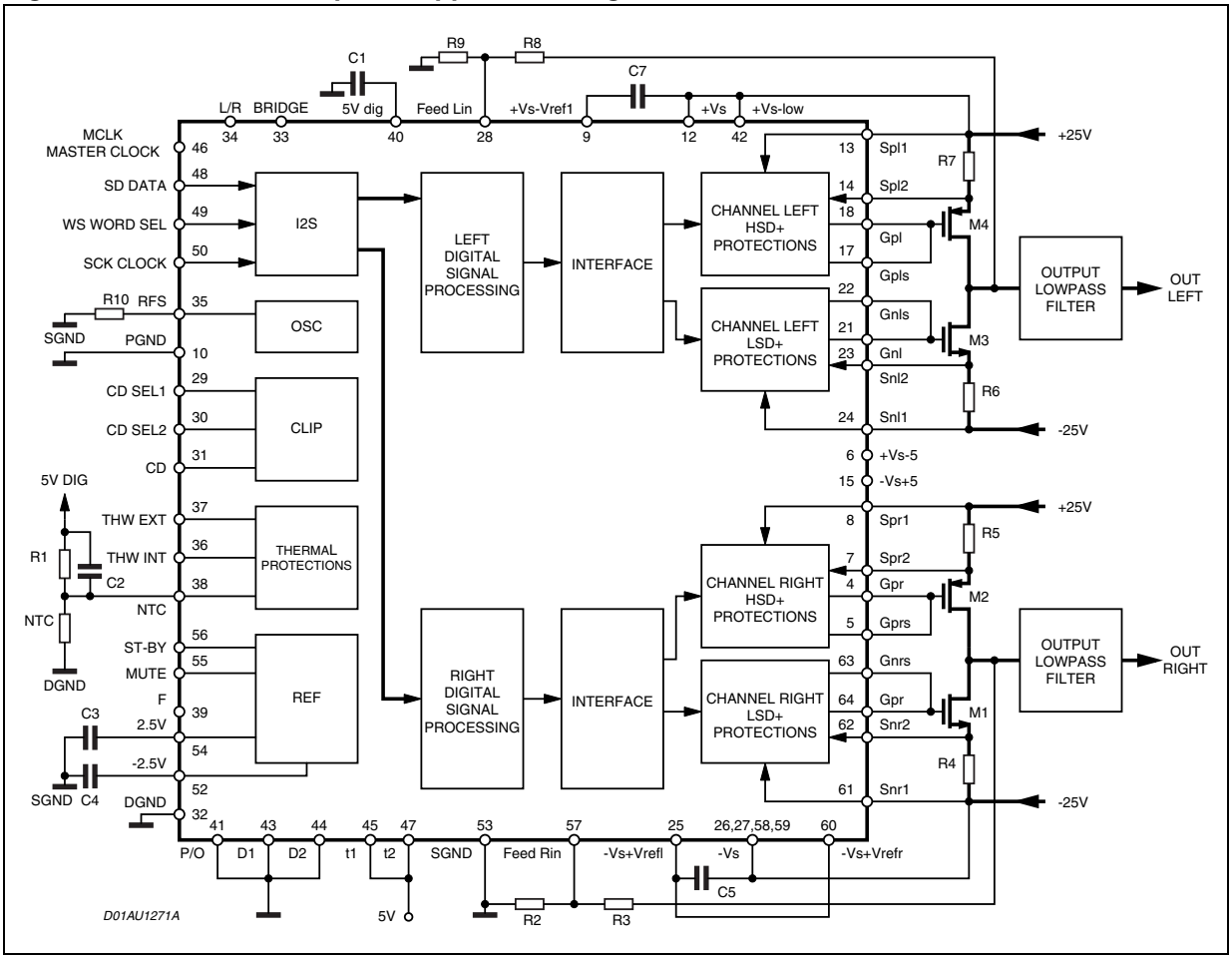
1 Block and simplified application diagram

Figure 1. Block and simplified application diagram



2 Pin description

Figure 2. Pins connection diagram (top view)

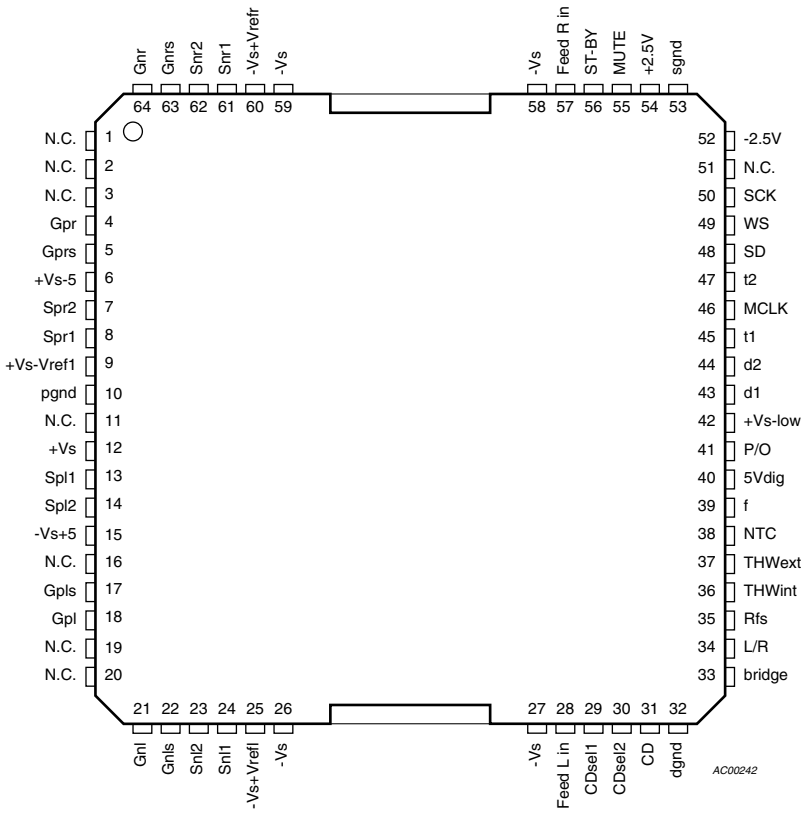


Table 2. Pins description

Pin number	Name	Function	Voltage limit (low)	Voltage limit (high)
1	N.C.	Not connected		
2	N.C.	Not connected		
3	N.C.	Not connected		
4	Gpr	Gate PMOS, right channel	+Vs-12V	30V
5	Gprs	Sense gate PMOS, right channel	+Vs-12V	30V
6	+Vs-5		+Vs-6	
7	Spr2	Sensing 2 PMOS, right channel		30V
8	Spr1	Sensing 1 PMOS, right channel		30V
9	+Vs-Vref1	Supply drivers PMOS	+Vs-12V	30V
10	pgnd	Power ground	0 (ref.)	
11	N.C.	Not connected		

Table 2. Pins description (continued)

Pin number	Name	Function	Voltage limit (low)	Voltage limit (high)
12	+Vs	Positive power supply		30V
13	Spl1	Sensing 1 PMOS, left channel		30V
14	Spl2	Sensing 2 PMOS, left channel		30V
15	-Vs+5			-Vs+6
16	N.C.	Not connected		
17	Gpls	Sense gate PMOS, left channel	+Vs-12V	30V
18	Gpl	Gate PMOS, left channel	+Vs-12V	30V
19	N.C.	Not connected		
20	N.C.	Not connected		
21	Gnl	Gate NMOS, left channel	-30V	-Vs+12V
22	Gnls	Gate NMOS, left channel	-30V	-Vs+12V
23	Snl2	Sensing 2 NMOS, left channel	-30V	
24	Snl1	Sensing 1 NMOS, left Channel	-30V	
25	-Vs+Vrefl	Supply drivers NMOS. left channel	-30V	-Vs+12V
26	-Vs	Negative power supply	-30V	
27	-Vs	Negative power supply	-30V	
28	Feed L in	Feedback network left channel	-5V	5V
29	CDsel1	Clip detector selection 1		5.5V
30	CD sel2	Clip detector selection 2		5.5V
31	CD	Clip detector output		5.5V
32	dgnd	Digital ground	0 (ref)	
33	bridge	Stereo / bridge selection pin 0 = Stereo; 1 = Bridge		6V
34	L / R	Bridge Left/Right Selection 1 = Right; 0 = Left		6V
35	Rfs	pcm-pwm gain conversion resistor		6V
36	THWint	Internal thermal warning output		5.5V
37	THWext	External thermal warning output		5.5V
38	NTC	Sensing resistors network		5.5V
39	f			6V
40	5Vdig	Digital 5V supply output		6V
41	P/O	PLL/FREE running osc. option		6V
42	+Vs-low	Positive voltage supply low power		30
43	d1	Dither 1		6V
44	d2	Dither 2		6V

Table 2. Pins description (continued)

Pin number	Name	Function	Voltage limit (low)	Voltage limit (high)
45	t1			6V
46	MCLK	Master clock input (256 x fs)		6V
47	t2			6V
48	SD	I2S serial data		6V
49	WS	I2S word select		6V
50	SCK	I2S serial clock		6V
51	N.C.	Not connected		
52	-2.5V	Signal -2.5V supply output	-2.75V	
53	sgnd	Signal ground	0 (ref)	
54	+2.5V	Signal 2.5V supply output		2.75V
55	MUTE	Mute input		5.5V
56	ST-BY	Stand by input		6V
57	Feed R in	Feedback network right channel	-5	5V
58	-Vs	Negative voltage supply	-30V	
59	-Vs	Negative voltage supply	-30V	
60	-Vs+Vrefr	Supply drivers NMOS. Right channel	-30V	-Vs+12V
61	Snr1	Sensing 2 NMOS, right channel	-30V	
62	Snr2	Sensing 1 NMOS, right channel	-30V	
63	Gnrs	Sense gate NMOS, right channel	-30V	-Vs+12V
64	Gnr	Gate NMOS, right channel	-30V	-Vs+12V

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$\pm V_s$	Operating supply voltage	±30	V
T_j	Junction temperature, operating range	-40 to 150	°C
T_{stg}	Storage temperature, operating range	-55 to 150	°C

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction to case	3	°C/W

3.3 Electrical characteristics

Table 5. Electrical characteristics

(V_S = ±25V, R_L = 4Ω, f = 1kHz, T_j = 25°C, F_S = 44.1kHz, Single-Ended, application circuit shown in *Figure 3*, 2 x 65W/1 x 130W system, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$\pm V_S$	Operating supply voltage		±12		±30	V
I_q	Quiescent supply current	$V_{st\text{-}by}$ = 5V from $+V_S$		25		mA
		$V_{st\text{-}by}$ = 5V from $+V_S$-low		20		mA
		$V_{st\text{-}by}$ = 5V from $-V_S$		25		mA
$I_{st\text{-}by}$	Quiescent supply current	$V_{st\text{-}by}$ = 0 from $+V_S$		0.3		mA
		$V_{st\text{-}by}$ = 0 from $+V_S$-low		0.2		mA
		$V_{st\text{-}by}$ = 0 from $-V_S$		0.3		mA
V_{os}	Output offset voltage	Output-GND (single-ended)			250	mV
V_{os}	Output offset voltage	Output L - Output R (bridge)			250	mV
P_o	Output power	Single-ended, @ THD = 1% 2 x 70W system		70		W
P_o	Output power	Bridge, @ THD = 1% 1 x 250W system		250		W
P_d	Power dissipation of the TDA7571	@ P_{out} = 25 W, bridge configuration		1.75		W

Table 5. Electrical characteristics (continued)

(V_S = ±25V, R_L = 4Ω, f = 1kHz, T_j = 25°C, F_S = 44.1kHz, Single-Ended, application circuit shown in *Figure 3*, 2 x 65W/1 x 130W system, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
P_{dt}	Power dissipation of the external power transistors	@ P_{out} = 25W, bridge configuration, 1x250W system		10		W
THD	Total harmonic distortion	@ P_{out} = 10 W, single ended		0.1		%
		@ P_{out} = 40 W, bridge		0.05		%
V_{ohs}	Half scale output voltage	single-ended, output voltage @ IN = –6dBFS		10		Vrms
E_n	Output noise @ IN = -999dBFS	"A" weighted, single-ended “A” weighted, bridge		180 100		µV
DR	Dynamic range	“A” weighted, -60dBFS, Single-ended PLL option circuit		85		dB
		“A” weighted, -60dBFS, Bridge free running oscillation option		96		dB
S/N	Signal-to-noise ratio (noise floor)	"A" weighted, single-ended “A” weighted, bridge		100 110		dB
Ge	Gain error	f = 1kHz			1.5	dB
ΔG_e	Delta gain error between channels	f = 1kHz			0.2	dB
c_t	Crosstalk	f = 1kHz, V_o = 1Vrms		60		dB
V_{gspth}	Threshold voltage of the Pchannel V_{gs} sensor (VSpx1 - VGpxs)		2.5	3	3.5	V
V_{gsnth}	Threshold voltage of the Pchannel V_{gs} sensor (VSnxs - VSnx1)		2.5	3	3.5	V
A_m	Mute attenuation	V_o = 1Vrms	80	90		dB
SVR	Supply voltage rejection	f = 100Hz, V_r = 0.5V	50	60		dB
F_{SW}	Switching frequency			F_S x 8		KHz
V_{il}	3.3V Logic inputs low level voltage	pin: ST-BY, MUTE, SD, WS, SCK, MCLK bridge			1.5	V
V_{ih}	3.3V Logic inputs high level voltage		2.3			V
V_{il}	5V Logic inputs low level voltage	pin: L/R, CD SEL1, CD SEL2, P/O, D1, D2. (these pins are typically connected to the DGND or 5V dig pins)			1.5	V
V_{ih}	5V Logic inputs high level voltage		3.5			V

Table 5. Electrical characteristics (continued)

(V_S = ±25V, R_L = 4Ω, f = 1kHz, T_j = 25°C, F_S = 44.1kHz, Single-Ended, application circuit shown in *Figure 3*, 2 x 65W/1 x 130W system, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Clip detector						
Vcd	Clip detector pin operating voltage (open drain)				10	V
CDl	Clip detector pin leakage current	CD off			1	µA
CDs	Clip detector pin saturation voltage	CD on, 1mA			1	V
CDi	Clip detector THD intervention	CDsel1=0, CDsel2=0 (near clipping detection)			0.5	%
		CDsel1=0, CDsel2=1		1		%
		CDsel1=1, CDsel2=0		5		%
		CDsel1=1, CDsel2=1		8		%
Protections						
T_{hwc}	Chip thermal warning intervention		135	150	165	°C
T_{sdc}	Thermal shut-down chip		145	160	175	°C
T_{sdch}	Thermal shut-down chip hysteresis		7	10	13	°C
T_{hws}	External thermal warning intervention		5Vdig x 0.45	5Vdig x 0.48	5Vdig x 0.51	V
T_{sds}	External shut-down intervention		5Vdig x 0.37	5Vdig x 0.4	5Vdig x 0.43	V
T_{sdsh}	External thermal shut-down hysteresis		5Vdig x 0.037	5Vdig x 0.04	5Vdig x 0.043	V
V_{pp}	Protection intervention voltage Pchannel (Vspx1-Vspx2)		85	100	120	mV
V_{pn}	Protection intervention voltage Nchannel (Vsnx2-Vsnx1)		85	100	120	mV
I_{spx1}	Current input pins 7, 13		150	200	260	µA
I_{snx1}	Current output pins 7, 13		150	200	260	µA
Drivers						
V_{hgp}	High level output voltage (Gpl, Gpr)			$+V_s$ -10		V
V_{lgp}	Low level output voltage (Gpl, Gpr)			$+V_s$		V
V_{hgn}	High level output voltage (Gnl, Gnr)			$-V_s$		V
V_{lgn}	Low level output voltage (Gnl, Gnr)			$-V_s$ +10		V
I_{hgp}	High level output sink current (Gpl, Gpr, peak)			2.2		A

Table 5. Electrical characteristics (continued)

(V_S = ±25V, R_L = 4Ω, f = 1kHz, T_j = 25°C, F_S = 44.1kHz, Single-Ended, application circuit shown in *Figure 3*, 2 x 65W/1 x 130W system, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{lgp}	Low level output source current (Gpl, Gpr, peak)			2.7		A
I_{hgn}	High level output sink current (Gnl, Gnr, peak)			2.5		A
I_{lgn}	Low level output source current (Gnl, Gnr, peak)			1.7		A
Internal power supply						
5Vdig	5Vdig pin output voltage	Reference: dgnd pin		5		V
2.5V	2.5V pin output voltage	Reference: sgnd pin		2.5		V
-2.5V	-2.5V pin output voltage	Reference: sgnd pin		-2.5		V
Vref1	Vref1 pin output voltage	Reference: + Vs pin		-10		V
Vrefl/Vrefr	Vrefl, Vrefr pin output voltage	Reference: - Vs pin		10		V

Figure 3. PLL option diagram

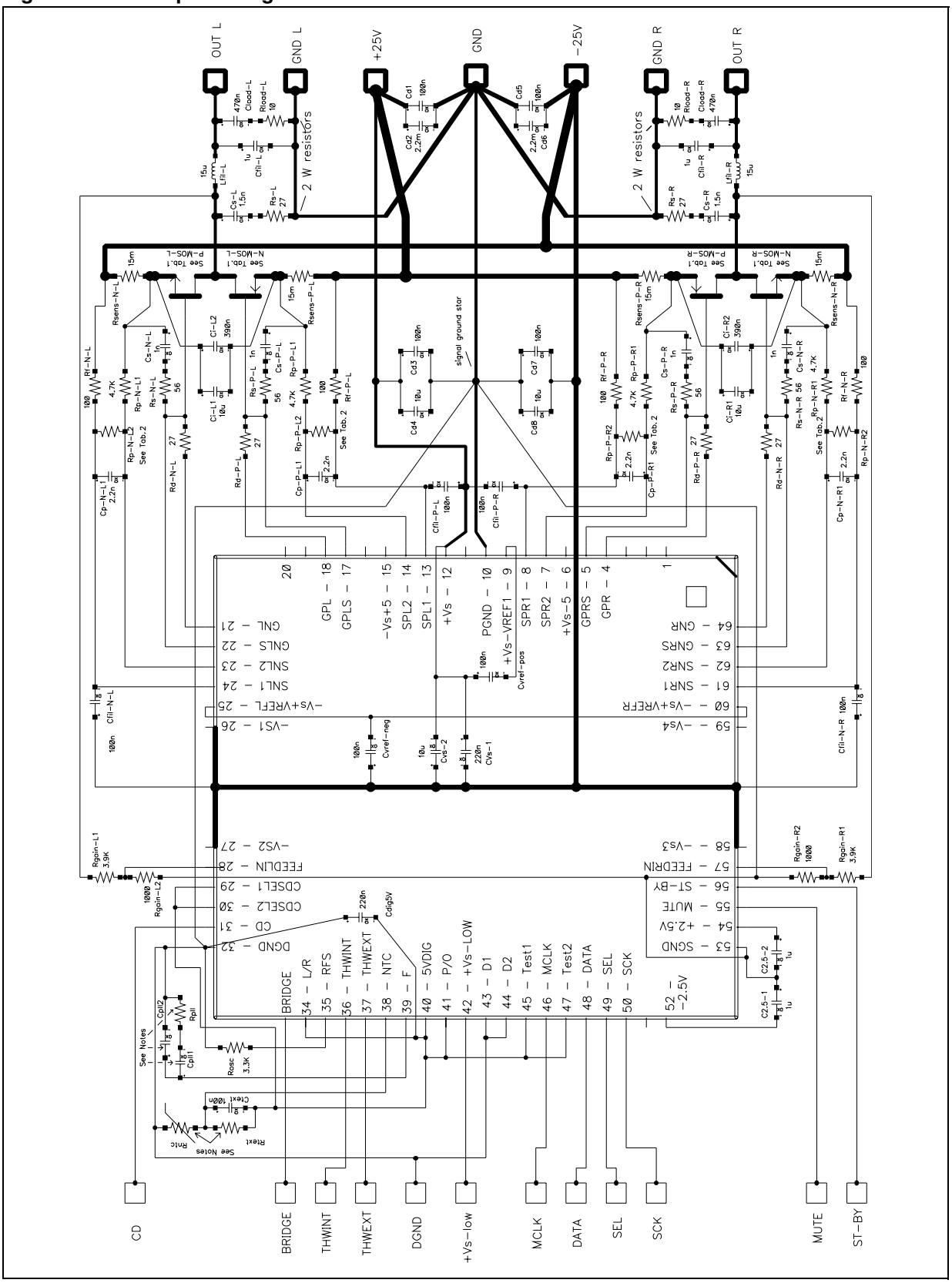
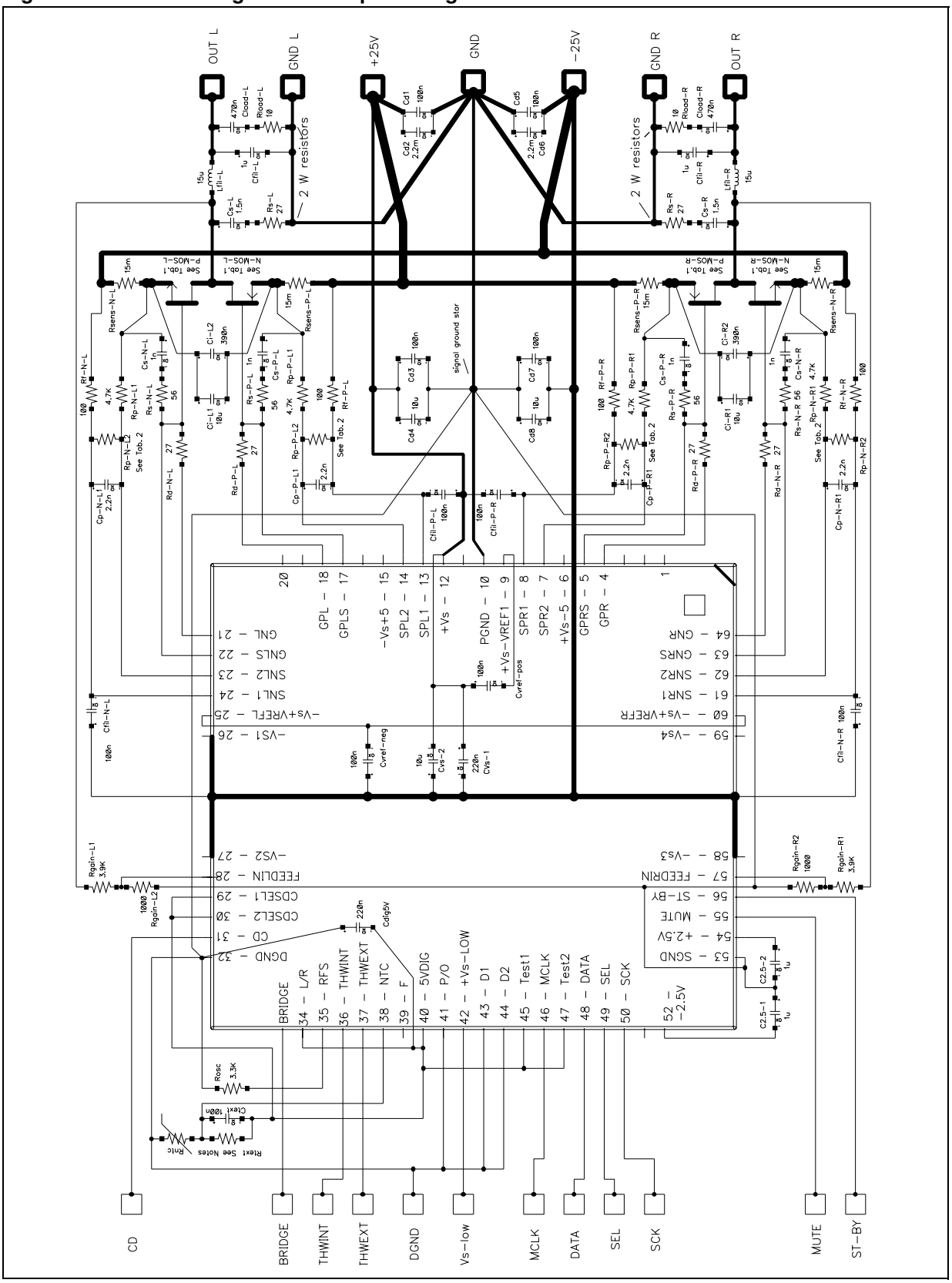


Figure 4. Free running oscillator option diagram



3.4 Notes on the electrical schematic shown in *Figure 3* and *4*

3.4.1 Main characteristics

- 2 channels single-ended or 1 channel bridge PWM amplifier
- Power output: see *Table 5*
- *Figure 3*: PLL option
- *Figure 4*: free running oscillator option
- Output voltage @ input = -6Bfs:
  - *Figure 3*: 10Vrms (single ended) - 20Vrms (bridge)
  - *Figure 4*: 9.5Vrms (single ended) - 19Vrms (bridge)
- Clip detector settled at THD=10%
- No dithering selected

The schematic is depicted showing the suggested structure of the printed circuit board tracks (star points, high current path, components placement).

To avoid malfunctioning due to the parasitic inductance, short connections lengths are recommended.

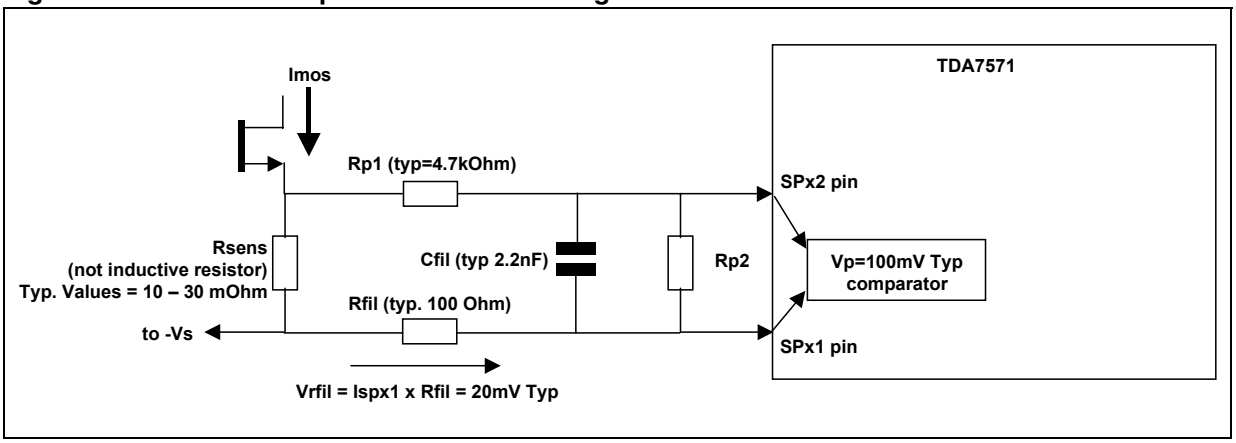
Table 6. Component characteristics

Components (See schematic of *Figure 3* & *3*)	Minimum load: 2 x 4 Ohm single-ended or 8 Ohm bridge (2 x 65W / 1 x 130W) (power supply = ±25V)	Minimum load: 2 x 2 Ohm single-ended or 4Ohm bridge (2 x 125W / 1 x 250W) (power supply = ±25V)
P-MOS-L P-MOS-R	STP12PF06	2 x STP12PF06 in parallel
N-MOS-L N-MOS-R	STP14NF06	2 x STP14NF06 in parallel
Rp-N-L2 RP-P-L2 Rp-N-R2 Rp-P-R2	Not present	4.7K

4 Functions, pins and components description

4.1 Short circuit protection current calculation

Figure 5. Short circuit protection current diagram



$$I_{lim} = \frac{1}{Rsens}\left(\frac{Vpx \cdot (Rp1 + Rp2)}{Rp2} + Vfil\right)$$

$$I_{lim} = \frac{1}{Rsens}(Vpx + Vfil) \quad \leftarrow \text{if Rp2 is not used}$$

4.2 External thermal protection network

The purpose of this function is to sense critical points of the amplifier system, as example the heatsink of the power transistors, avoiding too high temperature.

Through the external thermal warning pin (THWEXT, pin 37), a signal useful to reduce the power dissipation reducing (as example) the output power and/or, in a system provided of regulated power supply, reducing the voltage supply of the amplifier ($\pm V_S$) is present.

Example of external thermal protection circuitry

- Components:
  - type: B57621 C621/100k/+
  - Text = 10K
- Results (simulations):
  - External thermal warning temperature intervention: 90 °C
  - External thermal shut down temperature intervention: 100 °C
  - External thermal shut down hysteresis: 6°C

4.3 Internal thermal protection network

The purpose of this function is to sense the chip temperature. Because of the power dissipation of this device is almost constant (is not dependent by the output power), the system must be designed to avoid chip temperature higher than 140 °C.

The internal thermal protection is intended to avoid dangerous situations due to, as example, damaged power transistors (gate-source shorted) or bad environments conditions.

Through the internal thermal warning pin (THWINT, pin 36), a signal useful to switch-off the system or, at least, reduce the power dissipation reducing (as example) the output power and/or, in a system provided of regulated power supply, reducing the voltage supply of the amplifier (±Vs) is present.

4.4 Feedback

The resistors Rgain-L1, Rgain-L2 for the Left channel and Rgain-R1, Rgain-R2 for the Right channel defines the output AC voltage with a specific input digital data.

In the example, with 3.9Kohm and 1kohm, as shown in the schematic, the output voltage @ input = -6dBFS, is indicated in the Main characteristics description. These values are needed to reach the clipping with 0dBFS input digital data and Vs = ±25V.

If different power supply values are used, different resistors can be used to guarantee the clipping (then the output power), optimizing the signal to noise ratio.

If Vsmax is the maximum power supply at which the amplifier must goes into clipping condition, the value of Rgain-X1 is given by:

$$R_{gain-X1} - \frac{(V_{smax} \cdot R_{gain-X2} - 5.1 \cdot R_{gain-X2})}{5.1}$$

Considering $R_{gain\text{-}X2}$ = 1kohm, the relation become:

$$R_{gain-X1} = \frac{(V_{smax} - 5.1)}{5.1}$$

As example, if V_{smax} = ±20V, R_{gain} - L1 = R_{gain} - R1 = 2.92kohm ~= 3kohm

4.5 Gate driving network

The main purpose of the 27 ohm resistors Rd-N-L, Rd-P-L, Rd-N-R and Rd-P-R are the following:

1. Dumping of the L-C equivalent circuit done by the parasitic inductance and capacitance present in the circuit
2. Reduction of the dv/dt of the Vgs and then reduction of the di/dt of the drain current of the power MOS.

The R-C snubber network done by:

Rs-N-L, Cs-N-L

Rs-P-L, Cs-P-L

Rs-N-R, Cs-N-R

Rs-P-R, Cs-P-R

Are in the direction to increase the dumping (point 1) and reduce the dv/dt (point 2).
The value of these components is also depending on the layout structure. With a reduction of the parasitic inductance present in the P.C. board layout, in the region around the power transistors, the value of these components can be reduced, giving advantage in terms of THD, mainly at mid-high power levels, due to the reduction of the "dead zone".
The minimum suggested value of Rd-x-x is around 10 Ohm, while, is some cases, Rs-x-x and Cs-x-x can be removed.

4.6 PLL

In case of the schematic shown in *Figure 3*, the internal oscillator is locked by a PLL circuit at the Master Clock input frequency (MCLK).
The loop filter of this PLL is externally connected to the pin F (39). It consists in a lag-lead filter (Cpll1, Rpll). The output resistance of the pin F is a 10K (typ) resistor.
The typical suggested values of Cpll1 and Rpll are the following:

Cpll1 = 10Kpf

Rpll = 1Kohm.

In some cases, in a system with few clock interactions and a good MCLK signal, a parallel capacitor Cpll2 of 2.2nF-4.7nF can help to decrease the noise at the pin F.
With the PLL option, the A.C. output amplitude is not dependant by the resistor Rosc, because the voltage across Rosc is defined by the PLL itself, Moreover, the output A.C. voltage is independent also from the clock of the PCM signal (32kHz, 44.1kHz, 48kHz).
Vice versa, if the free running oscillation is selected, the output signal is dependant by the Rosc value and from the input PCM frequency.

4.7 Dither

With the pins D1 (43) and D2 (44) 4 types of digital dithering is achievable:

Table 7. 4 types of digital dithering

	D1	D2	Dithering
1	0	0	Low
2	0	1	Mid-low
3	1	0	Mid-high
4	1	1	High

Because of the recorded signals (music or speech) already contains some amount of noise, the dithering is generally not needed.

For high quality signals, it is suggested do not use the cases 3 and 4, that can be useful only in case of low resolution signals without noise added.

4.8 External connections description

4.8.1 CD, THWEXT, THWINT

These pins, if used, it must be connected to a pull-up resistor (>10kOhm) connected to a supply voltage referred to the receiver device (as example, a µP).

Maximum voltage = 6V.

4.8.2 MUTE

Mute pin

4.8.3 ST-BY - St-By pin.

To avoid pop noise due to multiple ST-BY parasitic pulses, an R-C network must be added (as example 47kOhm, 0.1µF)

4.8.4 +Vs-low -

This pin supply the low voltage circuits. It can be connected to the +Vs or to a reference voltage comprising between 12V to +Vs.

A connection to +Vs through a 100Ohm resistor, together a 1uF capacitor placed from +Vs-low and GND is possible too.

4.8.5 DATA, SEL, SCK

I^2S digital inputs

4.8.6 MCLK

Master clock input. Must be F(MCLK) = 256 x Fs (11289.6kHz in case of Fs = 44.1 kHz)

4.8.7 DGND

Digital ground

4.8.8 BRIDGE and L/R

With this pin, the mode of working of the device (bridge or single-ended) can be selected.

If it is connected to the pin 32 (DGND) the device works in single-ended mode

If it is connected to the pin 40 (5Vdig) the device works in bridge mode.

In case of bridge mode, the pin 34 (L/R) makes the channel selection. If connected to DGND, the Left channel is selected. If connected to 5Vdig, is selected the Right channel.

These pins must be selected with the device in ST-BY condition.

In case of single-ended operation, it is suggested to put the L/R pin at 5V.

4.9 Components with critical placement and type

- Ci-L1, Ci-L2, Ci-R1, Ci-R2 must be placed as near as possible to the sources of the respective power MOS. If 2 power MOS in parallel are needed, can be useful to place a couple of capacitors for each couple of power MOS. These capacitors are needed to absorb the high di/dt current present during the Pchannel/Nchannel and Nchannel/Pchannel transition that can cause high peak voltages on the power supply wiring connection due to their parasitic inductance.
- The capacitors placed between +Vs to GND and to -Vs are distributed along the power lines. With P.C. board with very short connections, some of these capacitors can be avoided (Cvs-1, Cvs-2, Cd3, Cd4, Cd8, Cd7).
- The current sensing resistors Rsens-N-L, Rsens-P-L, Rsens-P-R and Rsens-N-R must be not inductive components, as example, made by a constant an wire.

5 Package information

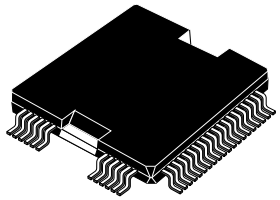
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 6. HiQUAD-64 mechanical data and package dimensions

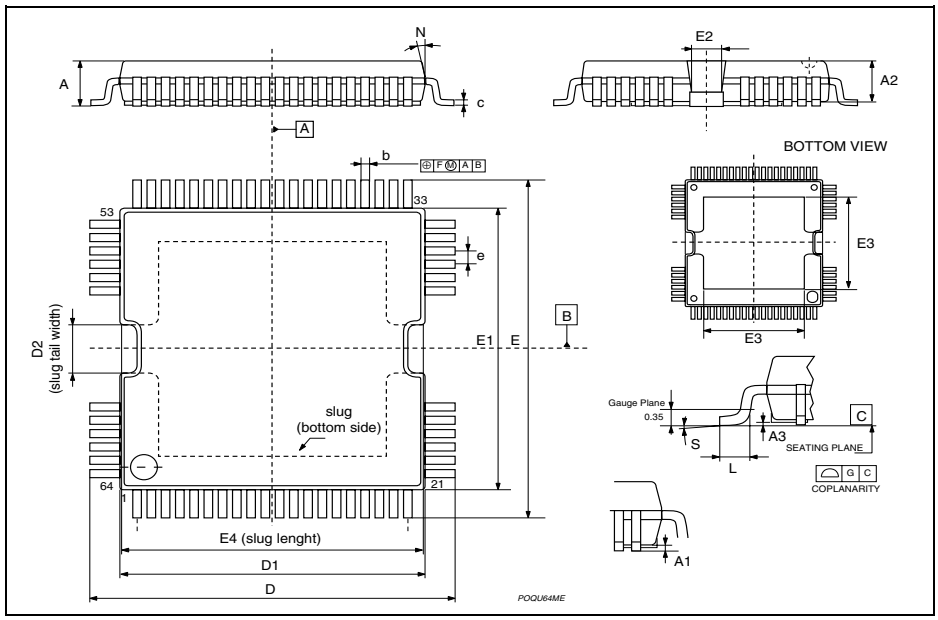
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.15			0.124
A1	0		0.25	0		0.010
A2	2.50		2.90	0.10		0.114
A3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	17.00		17.40	0.669		0.685
D1 (1)	13.90	14.00	14.10	0.547	0.551	0.555
D2	2.65	2.80	2.95	0.104	0.110	0.116
E	17.00		17.40	0.669		0.685
E1 (1)	13.90	14.00	14.10	0.547	0.551	0.555
e		0.65			0.025	
E2	2.35		2.65	0.092		0.104
E3	9.30	9.50	9.70	0.366	0.374	0.382
E4	13.30	13.50	13.70	0.523	0.531	0.539
F		0.10			0.004	
G		0.12			0.005	
L	0.80		1.10	0.031		0.043
N	10°(max.)					
S	0°(min.), 7°(max.)					

(1): "D1" and "E1" do not include mold flash or protusions
- Mold flash or protusions shall not exceed 0.15mm(0.006inch) per side

OUTLINE AND MECHANICAL DATA



HiQUAD-64



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
3-Sep-2007	1	Initial release.

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