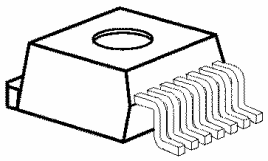
5-V LOW-DROP FIXED VOLTAGE REGULATOR

ILE4271-2

Functional Description

The device is a 5-V low-drop fixed-voltage regulator. The maximum input voltage is 42 V (65 V, ≤400 ms). Up to an input voltage of 26 V and for an output current up to 550 mA it regulates the output voltage within a 2% accuracy. The short circuit protection limits the output current of more than 650 mA.

The IC can be switched off via the inhibit input. An integrated watchdog monitors the connected controller. The device incorporates overvoltage protection and temperature protection that disables the circuit at unpermissibly high temperatures.



P-TO 220-7-180

Features

- Output voltage tolerance ≤± 2%
- Low-drop voltage
- Integrated overtemperature protection
- Reverse polarity protection
- Input voltage up to 42 V
- Overvoltage protection up to 65 V (≤ 400 ms)
- Short-circuit proof
- Suitable for use in automotive electronics
- Wide temperature range
- Adjustable reset and watchdog time

Pin Definitions and Functions

Pin	Symbol	Function
1	I	Input; block to ground directly on the IC with ceramic capacitor.
2	INH	Inhibit
3	RO	Reset Output; the open collector output is connected to the 5 V output via an integrated resistor of 30 kOhm
4	GND	Ground
5	D	Reset Delay; connect a capacitor to ground for delay time adjustment.
6	W	Watchdog Input
7	Q	5-V Output; block to ground with 22 uF capacitor, ESR < 3 Ohm.

Application Description

The IC regulates an input voltage in the range of 5.5 V < V_I < 36 V to V_{Qnom} = 5.0 V. Up to 26 V it produces a regulated output current of more than 550 mA. Above 26 V the save-operating-area protection allows operation up to 36 V with a regulated output current of more than 300 mA. Overvoltage protection limits operation at 42 V. The overvoltage protection hysteresis restores operation if the input voltage has dropped below 36 V. The IC can be switched off via the inhibit input, which causes the quiescent current to drop below 50 uA. A reset signal is generated for an output voltage of VQ < 4.5 V. The watchdog circuit monitors a connected controller. If there is no positive-going edge at the watchdog input within a fixed time, the reset output is set to low. The delay for power-on reset and the maximum permitted watchdog-pulse period can be set externally with a capacitor.

Design Notes for External Components

An input capacitor CI is necessary for compensation of line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx. 1 Ohm. in series with C_I. An output capacitor CQ is necessary for the stability of the regulating circuit. Stability is guaranteed at values of C_Q ≤22 uF and an ESR of <3 Ohm.

Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of a series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

If the output voltage decreases below 4.5 V, an external capacitor CD on pin 4 (D) will be discharged by the reset generator. If the voltage on this capacitor VD drops below VDRL, a reset signal is generated on pin 2 (RO), i.e. reset output is set low. If the output voltage rises above 4.5 V, CD will be charged with constant current. After the power-on-reset time V_D reaches V_{DU} and the reset output will be set high again. The value of the power-on-reset time can be set within a wide range depending on the capacity of C_D. The value of the pull-up resistor at reset output is typically 30 kOhm.

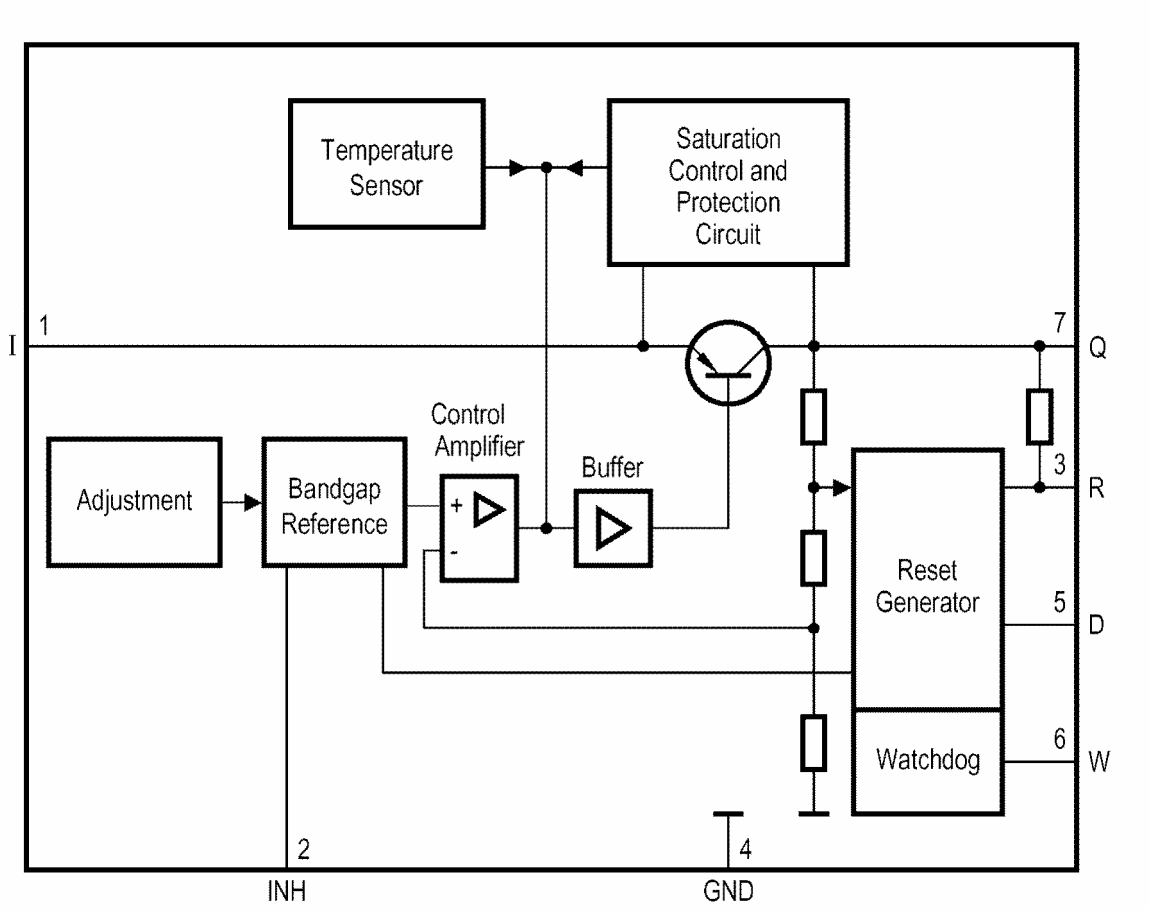
After V_D has reached the voltage V_{DU} and reset was set to high, the watchdog circuit is enabled and discharges C_D with a constant current. If there is no positive-going edge observed at watchdog input, C_D will be discharged down to VDWL. Then reset will be set low and the watchdog circuit will be disabled. C_D will be charged with the current as at power-on reset until V_D reaches V_{DU} and reset will be set high again.

If a watchdog pulse will be observed before C_D is discharged down to V_{DWL}, the watchdog circuit will be enabled and CD will be charged too, but reset will not be set low. After V_D has reached V_{DU}, the periodical behavior starts again.

The IC also incorporates a number of internal circuits for protection against:

- Overload
- Overvoltage
- Overtemperature
- Reverse polarity

Block Diagram



Maximum & Absolute Maximum Ratings

Parameter Symbol	Unit	Maximum Ratings		Absolute Maximum Ratings	
		min.	max.	min.	max.
Junction temperature, T_J	°C	-40	125	-40	150
Storage temperature, T_S	°C	-	-	-50	150
Input voltage, V_I	V	-	-	-	-
		-	-	-	-
Inhibit voltage, U_{INH}	V	6	36	-42	42
		-	-	-	65*
Input current, I_I	A	-	internally limited	-	internally limited
Output voltage, U_Q	V	4,9	5,1	-1	16
Output current, I_Q	mA	-5	internally limited	-5	internally limited
Current on common pin ,I_{GND}	mA	-	-	-0.5	–
Reset voltage, U_R	V	4,9	5,1	-1	16
Reset current, I_R	A	-5	internally limited	-5	internally limited
Output voltage, U_Q	V	-	-	-0.3	7
Output current, I_Q	mA	-	-	-5	5
Output voltage, U_Q	V	-	-	-0.3	7
Output current, I_Q	mA	-	-	-5	5
Thermal resistance junction ambient (P-TO-263-7-1), $R_{th\ ja}$,	°C /W	-	70**	-	70**
Thermal resistance junction case (P-TO-263-7-1), $R_{th\ jc}$	°C/W	-	3**	-	3**

* Time of influence t ≤ 400ms

** Thermal resistance junction ambient for IC with heat dissipater is calculated by formula:

$\mathbf{R_{th\ ja} = R_{th\ jc} + R_{th\ ca}}$ (1)

$R_{th\ jc}$ - thermal resistance junction case, °C /W.

Application circuit and heat dissipater have to provide $T_J \leq 125$ °C.

Maximum power P_{tot},Вт, dissipated by IC for T_A , is calculated by formula:

$\mathbf{P_{tot} = (125 - T_A) / R_{th\ ja}}$ (2)

125 – maximum permitable operating junction temperature, °C.

Optimum reliability and life time are guaranteed if the junction temperature does not exceed 125 °C in operating mode. Operation at up to the maximum junction temperature of 150 °C is possible in principle. Note, however, that operation at the maximum permitted ratings could affect the reliability of the device.

Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input voltage	VI	6	40	V	–
Junction temperature	Tj	– 40	150	°C	–
Thermal Resistance					
Junction ambient	Rthja	–	65	K/W	–
			70	K/W	P-TO263
Junction case	Rthjc	–	3	K/W	–
	Zthjc	–	2	K/W	t ≤1 ms

Characteristics

VI = 13.5 V; – 40 °C ≤Tj ≤125 °C (unless otherwise specified)

Parameter, unit	Symbol	Test Condition	Limit Values		Note
			Min.	Max.	
Output voltage, V	V_Q	6V≤V_I ≤26V; 5mA≤I_Q≤550mA	4.90	5.10	
		26V≤V_I ≤36V; I_Q≤300mA	4.90	5.10	
Output current limiting, mA	I_{Qmax}	V_Q=0B	650		
Current consumption, мкА, $I_q = I_I$	I_q	V_e=0B; I_Q=0mA		50	
Current consumption, mA $I_q = I_I - I_Q$		I_Q=5mA		1,5	
		I_Q=550mA		75	
		I_Q=550mA; V_I=5V		90	
Drop voltage, V	V_{Dr}	I_Q=550mA		0.7	3
Load regulation, mV	$\Delta V_{Q(I)}$	5мА ≤ I_Q ≤ 550mA V_I = 6 V		50	
Supply voltage regulation, mV	$\Delta U_{Q(U)}$	6В≤ U_I ≤ 26V I_Q=5mA		25	

Parameter, unit	Symbol	Test Condition	Limit Values		Note
			Min.	Max.	
Inhibit					
Inhibit ON voltage, V	$V_{INH,on}$	U_Q >4.5V	3,5		
Inhibit OFF voltage, V	$V_{INH,off}$	U_Q <0.8V		0,8	
Inhibit current, uA	I_{INH}	U_{INH}=5V	8	25	
Overvoltage protection					
Напряжение выключения, В	$V_{I, OV}$		40	46	
Watchdog					
Upper timing threshold, V	V_{DU}		1.4	2.3	
Lower watchdog timing threshold, V	V_{DWL}		0.2	0.8	
Discharge current, uA	I_{dis}	U_D=1V	1.5	3.5	
Charge current, uA	I_d	U_D=1V	8	25	
Watchdog period, ms	t_w	C_D=100 nF	40	75	
Watchdog trigger time, ms	t_{wt}	C_D=100 nF	30	66	
Reset Generator					
Switching threshold, V	V_{RT}		4.5	4.8	
Reset high voltage, V	V_{ROH}		4.5	-	
Reset low voltage, V	V_{ROL}	I_R=3mA, V_Q=4.4V	-	400	
Resistance of circuit, kOhm	R	Direct connection to pin Q	18	46	
Lower reset timing threshold, V	V_{DRL}	$V_Q < V_{RT}$	0.2	0.8	
Upper reset timing threshold, V	V_{DU}		1.4	2.3	
Delay time, ms	t_d	C_D = 100 nF	8	18	
Charge current, uA	I_d	V_D = 1.0 V	8	25	

Notes

1 Following capacitances are connected:

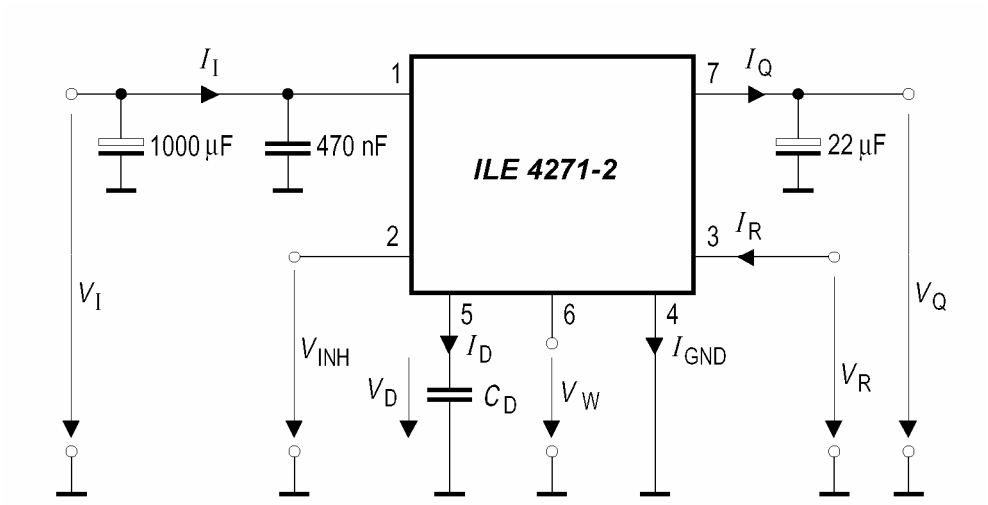
- on input $C1_I$ = 1000 uF(electrolytic), $C2_I$ = 470 nF
- on output C_Q = 22 uF (electrolytic).

2 Measurements of parameters have to carry out with pulse equipment.

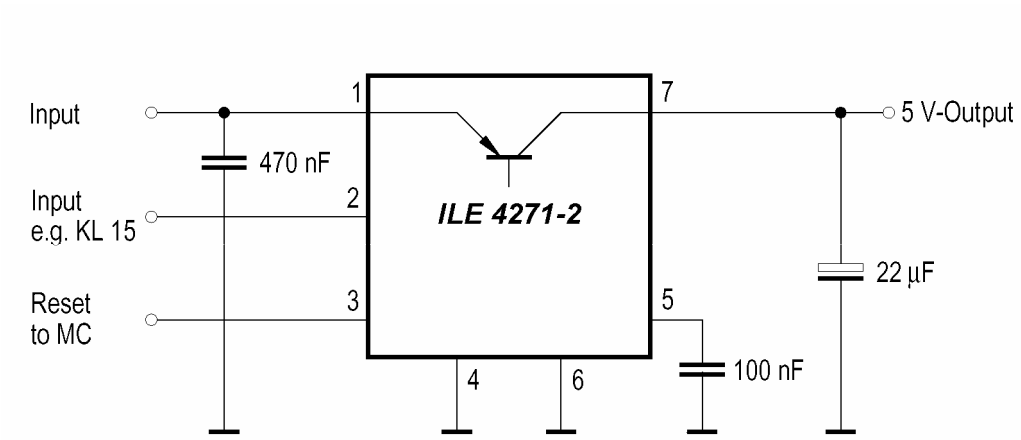
3 Drop voltage V_{Dr}= V_I - V_Q (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)

1)

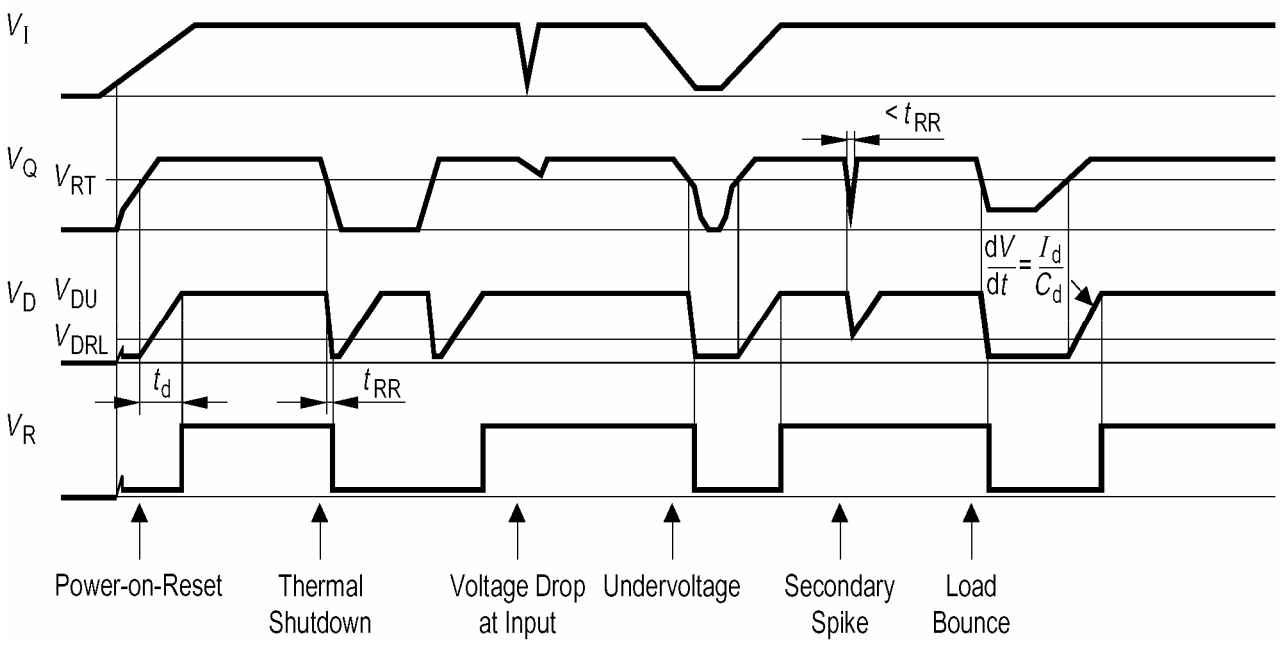
Test Circuit



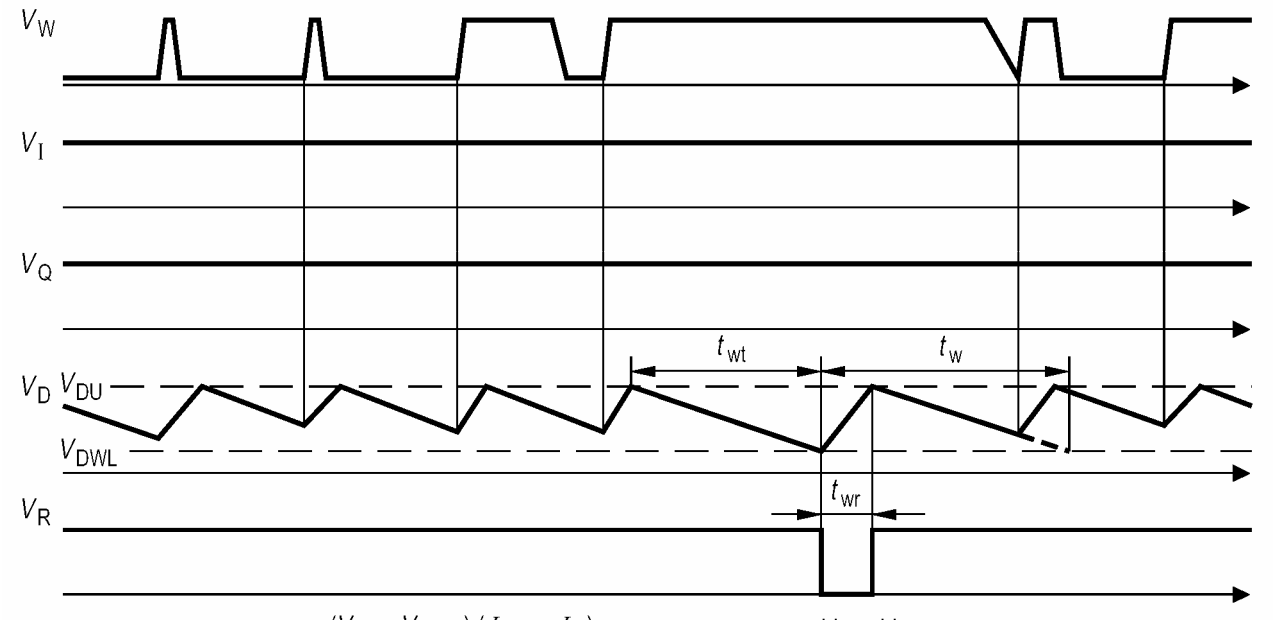
Application Circuit



Time Response



Time Response, Watchdog Behavior



$$t_w = \frac{(V_{DU} - V_{DWL})(I_{dis} + I_d)}{I_d \times I_{dis}} C_D \qquad t_{wr} = \frac{V_{DU} - V_{DWL}}{I_d} C_D = \text{(Watchdog Reset Time)}$$

$$t_{wt} = \frac{V_{DU} - V_{DWL}}{I_{dis}} C_D$$

Package Dimensions

P-TO 220-7-180