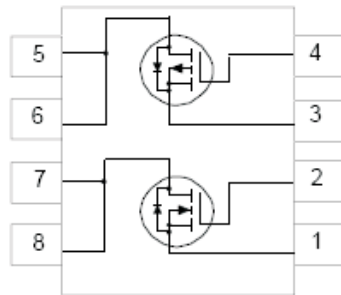
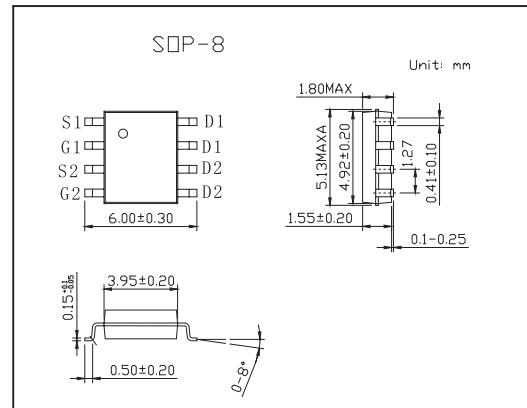


## Dual N & P-Channel Enhancement Mode Field Effect Transistor KDS9952A

### ■ Features

- N-Channel 3.7A, 30V,  $R_{DS(ON)}=0.08W$  @  $V_{GS}=10V$ .  
P-Channel -2.9A, -30V,  $R_{DS(ON)}=0.13W$  @  $V_{GS}=-10V$ .
- High density cell design or extremely low  $R_{DS(ON)}$ .
- High power and current handling capability in a widely used
- surface mount package.  
Dual (N & P-Channel) MOSFET in surface mount package.



### ■ Absolute Maximum Ratings $T_a = 25^\circ C$

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain to Source Voltage	$V_{DSS}$	30	-30	V
Gate to Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Drain Current Continuous (Note 1a)	$I_D$	$\pm 3.7$	$\pm 2.9$	A
Drain Current Pulsed		$\pm 15$	$\pm 10$	A
Power Dissipation for Dual Operation	$P_D$	2		W
Power Dissipation for Single Operation (Note 1a)	$P_D$	1.6		
(Note 1b)		1		
(Note 1c)		0.9		
Operating and Storage Temperature	$T_J, T_{STG}$	-55 to 150		$^\circ C$
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40		$^\circ C/W$
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78		$^\circ C/W$

## KDS9952A

## ■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditons	Type	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	N-Ch	30			V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	P-Ch	-30			
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V	N-Ch			2	μA
		V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C				25	
		V <sub>DS</sub> = -24 V, V <sub>GS</sub> = 0 V	P-Ch			-2	
		V <sub>DS</sub> = -24 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C				-25	
Gate-Body Leakage, Forward	I <sub>GSSF</sub>	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V	ALL			100	nA
Gate-Body Leakage, Reverse	I <sub>GSSR</sub>	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V	ALL			-100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	1	1.7	2.8	V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA, T <sub>J</sub> = 125°C		0.7	1.2	2.2	
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-1	-1.6	-2.8	
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA, T <sub>J</sub> = 125°C		-0.85	-1.25	-2.5	
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.0 A	N-Ch		0.06	0.08	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.0 A, T <sub>J</sub> = 125°C			0.08	0.13	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.5 A			0.08	0.11	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.5 A, T <sub>J</sub> = 125°C			0.11	0.18	
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1.0 A	P-Ch		0.11	0.13	
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1.0 A, T <sub>J</sub> = 125°C			0.15	0.21	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -0.5 A			0.17	0.2	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -0.5 A, T <sub>J</sub> = 125°C			0.24	0.32	
On-State Drain Current	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 5 V	N-Ch	15			A
		V <sub>GS</sub> = -10 V, V <sub>DS</sub> = -5 V	P-Ch	-10			
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.7 A	N-Ch		6		S
		V <sub>DS</sub> = -15 V, I <sub>D</sub> = -2.9 A	P-Ch		4		
Input Capacitance	C <sub>iss</sub>	N-Channel V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	N-Ch		320		pF
			P-Ch		350		
Output Capacitance	C <sub>oss</sub>	P-Channel	N-Ch		225		pF
			P-Ch		260		
Reverse Transfer Capacitance	C <sub>rss</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	N-Ch		85		pF
			P-Ch		100		
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 10 V, I <sub>D</sub> = 1 A	N-Ch		10	15	ns
			P-Ch		9	40	
Turn-On Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω (Note 2)	N-Ch		13	20	ns
			P-Ch		21	40	
Turn-Off Delay Time	t <sub>d(off)</sub>	P-Channel V <sub>DD</sub> = -10 V, I <sub>D</sub> = -1 A	N-Ch		21	50	ns
			P-Ch		21	90	
Turn-Off Fall Time	t <sub>f</sub>	V <sub>GS</sub> = -10 V, R <sub>GEN</sub> = 6 Ω (Note 2)	N-Ch		5	50	ns
			P-Ch		8	50	
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.7 A, V <sub>GS</sub> = 10 V	N-Ch		9.5	27	nC
			P-Ch		10	25	
Gate-Source Charge	Q <sub>gs</sub>	P-Channel	N-Ch		1.5		nC
			P-Ch		1.6		
Gate-Drain Charge	Q <sub>gd</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -2.9 A, V <sub>GS</sub> = -10 V	N-Ch		3.3		nC
			P-Ch		3.4		

## KDS9952A

## ■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Type	Min	Typ	Max	Unit
Maximum Continuous Drain-Source Diode Forward Current	Is		N-Ch			1.2	A
			P-Ch			-1.2	
Drain-Source Diode Forward Voltage	VSD	VGS = 0 V, Is = 1.25 A (Note 2)	N-Ch		0.8	1.3	V
		VGS = 0 V, Is = -1.25 A (Note 2)	P-Ch		-0.8	-1.3	
Reverse Recovery Time	trr	VGS=0 V, IF=1.25 A, dIF/dt=100A/μs	N-Ch			75	ns
		VGS=0 V, IF=-1.25 A, dIF/dt=100A/μs	P-Ch			100	

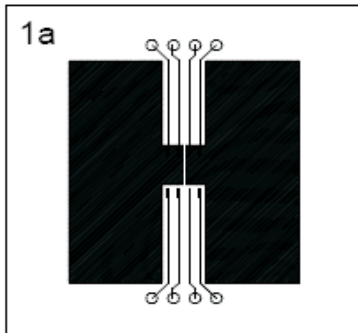
## Notes:

1.  $R_{\theta j-c}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta j-c}$  is guaranteed design while  $R_{\theta j-a}$  is determined by the user's board design.

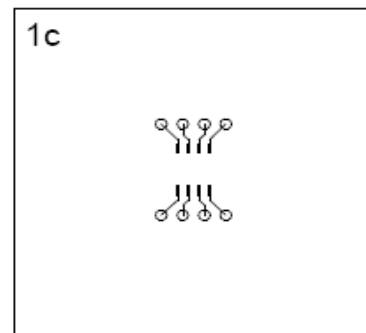
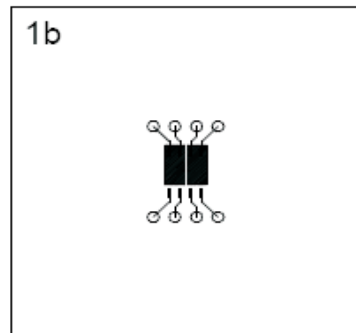
$$P_D(t) = \frac{T_j - T_a}{R_{\theta j-c}} = \frac{T_j - T_a}{R_{\theta j-c} + R_{\theta c-a}(t)} = I_D^2(t) \times R_{DS(on)} \theta_{rj}$$

Typical  $R_{\theta j-c}$  for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 78°C/W when mounted on a 0.5 in<sup>2</sup> pad of 2oz copper.
- b. 125°C/W when mounted on a 0.02 in<sup>2</sup> pad of 2oz copper.
- c. 135°C/W when mounted on a 0.003 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper



2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.