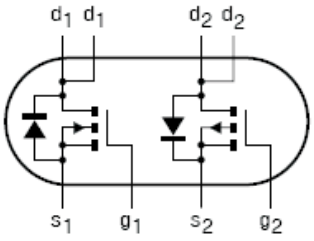
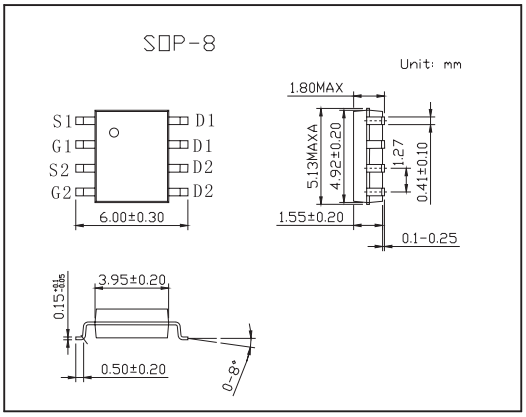
Complementary enhancement mode MOS transistors KHC21025

■ Features

- High-speed switching
- No secondary breakdown
- Very low on-resistance.





■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain to Source Voltage	V_{DSS}	30	-30	V
Gate to Source Voltage	V_{GS}	±20	±20	V
Drain Current Ts ≤ 80℃	I_D	3.5	-2.3	A
peak drain current *1	I_{DM}	14	-10	A
total power dissipation Ts = 80℃; *2	P_{tot}	2		W
Tamb = 25 ℃; * 3		2		
Tamb = 25℃; * 4		1		
Tamb = 25 ℃; *5		1.3		
storage temperature	T_{stg}	-65 to 150		℃
operating junction temperature	T_j	150		℃
source current (DC) Ts ≤ 80 ℃	I_S	1.5	-1.25	A
peak pulsed source current *1	I_{SM}	6	-5	A
thermal resistance from junction to soldering point	$R_{th\ j\text{-}s}$	35		K/W

*1 Pulse width and duty cycle limited by maximum junction temperature.

*2 Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.

*3 Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.

*4 Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

*5 Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

KHC21025

■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Type	Min	Typ	Max	Unit
drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0; I_D = 10 mA	N-Ch	30			V
		V_{GS} = 0; I_D = -10 mA	P-Ch	-30			V
gate-source threshold voltage	V_{GSth}	V_{GS} = V_{DS}; I_D = 1 mA	N-Ch	1		2.8	V
		V_{GS} = V_{DS}; I_D = -1 mA	P-Ch	-1		-2.8	V
drain-source leakage current	I_{DSS}	V_{GS} = 0; V_{DS} = 24 V	N-Ch			100	nA
		V_{GS} = 0; V_{DS} = -24 V	P-Ch			-100	nA
gate leakage current	I_{GSS}	V_{GS} = ±20 V; V_{DS} = 0	N-Ch			±100	nA
			P-Ch			±100	nA
on-state drain current	I_{Don}	V_{GS} = 10 V; V_{DS} = 1 V	N-Ch	3.5			A
		V_{GS} = 4.5 V; V_{DS} = 5 V		2			A
		V_{GS} = -10 V; V_{DS} = -1 V	P-Ch	-2.3			A
		V_{GS} = -4.5 V; V_{DS} = -5 V		-1			A
drain-source on-state resistance	R_{DSon}	V_{GS} = 4.5 V; I_D = 1 A	N-Ch		0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2.2 A			0.08	0.1	Ω
		V_{GS} = -4.5 V; I_D = - 0.5 A	P-Ch		0.33	0.4	Ω
		V_{GS} = -10 V; I_D = -1 A			0.22	0.25	Ω
forward transfer admittance	$\|y_{fs}\|$	V_{DS} = 20 V; I_D = 2.2 A	N-Ch	2	4.5		S
		V_{DS} = -20 V; I_D = -1 A	P-Ch	1	2		S
input capacitance	C_{iss}	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	N-Ch		250		pF
		V_{GS} = 0; V_{DS} = -20 V; f = 1 MHz	P-Ch		250		pF
output capacitance	C_{oss}	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	N-Ch		140		pF
		V_{GS} = 0; V_{DS} = -20 V; f = 1 MHz	P-Ch		140		pF
reverse transfer capacitance	C_{rss}	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	N-Ch		50		pF
		V_{GS} = 0; V_{DS} = -20 V; f = 1 MHz	P-Ch		50		pF
total gate charge	Q_G	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	N-Ch		10	30	nC
		V_{GS} = -10 V; V_{DS} = -15 V; I_D = -2.3 A	P-Ch		10	25	nC
gate-source charge	Q_{GS}	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	N-Ch		1		nC
		V_{GS} = -10 V; V_{DS} = -15 V; I_D = -2.3 A	P-Ch		1		nC
gate-drain charge	Q_{GD}	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	N-Ch		2.5		nC
		V_{GS} = -10 V; V_{DS} = -15 V; I_D = -2.3 A	P-Ch		3		nC
turn-on time	t_{on}	V_{GS} =0 to 10 V; V_{DD}=20V;I_D=1A;R_L=20 Ω	N-Ch		15	40	ns
		V_{GS}=0 to -10V;V_{DD}=-20V;I_D=-1 A;R_L=20 Ω	P-Ch		20	80	ns
turn-off time	t_{off}	V_{GS}=10 to 0 V;V_{DD}=20V;I_D=1A;R_L=20 Ω	N-Ch		25	140	ns
		V_{GS}=-10 to 0 V;V_{DD}=-20V;I_D=-1 A;R_L=20 Ω	P-Ch		50	140	ns
source-drain diode forward voltage	V_{SD}	V_{GD} = 0; I_S = 1.25 A	N-Ch			1.2	V
		V_{GD} = 0; I_S = -1.25 A	P-Ch			-1.6	V
reverse recovery time	t_{rr}	I_S = 1.25 A; di/dt = 100 A/μs	N-Ch		35	100	ns
		I_S = -1.25 A; di/dt = 100 A/μs	P-Ch		150	200	ns