Freescale Semiconductor

Technical Data

RF Power Field Effect Transistor

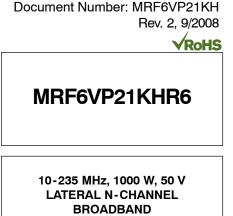
N-Channel Enhancement-Mode Lateral MOSFET

Designed primarily for pulsed wideband applications with frequencies up to 235 MHz. Device is unmatched and is suitable for use in industrial, medical and scientific applications.

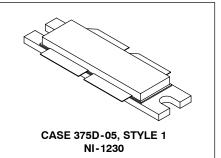
- Typical Pulsed Performance at 225 MHz: V_{DD} = 50 Volts, I_{DQ} = 150 mA, P_{out} = 1000 Watts Peak (200 W Avg.), Pulse Width = 100 μsec, Duty Cycle = 20% Power Gain — 24 dB
 - Drain Efficiency 67.5%
- Capable of Handling 10:1 VSWR, @ 50 Vdc, 225 MHz, 1000 Watts Peak Power

Features

- Qualified Up to a Maximum of 50 V_{DD} Operation
- Integrated ESD Protection
- Excellent Thermal Stability
- Designed for Push-Pull Operation
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- RoHS Compliant
- In Tape and Reel. R6 Suffix = 150 Units per 56 mm, 13 inch Reel.



RF POWER MOSFET



PART IS PUSH-PULL

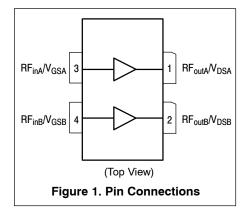


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	-0.5, +110	Vdc
Gate-Source Voltage	V _{GS}	-6, +10	Vdc
Storage Temperature Range	T _{stg}	- 65 to +150	°C
Case Operating Temperature	T _C	150	°C
Operating Junction Temperature	TJ	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value ^(1,2)	Unit
Thermal Resistance, Junction to Case			
Case Temperature 80°C, 1000 W Pulsed, 100 μsec Pulse Width, 20% Duty Cycle	$R_{\theta JC}$	0.03	°C/W

1. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

 Refer to AN1955, Thermal Measurement Methodology of RF Power Amplifiers. Go to <u>http://www.freescale.com/rf</u>. Select Documentation/Application Notes - AN1955.



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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Тур	Мах	Unit
Off Characteristics ⁽¹⁾	I				
Gate-Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}		_	20	μAdc
Drain-Source Breakdown Voltage (I _D = 300 mA, V _{GS} = 0 Vdc)	V _{(BR)DSS}	110			Vdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 50 Vdc, V _{GS} = 0 Vdc)	I _{DSS}			100	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)	I _{DSS}			5	mA
On Characteristics					*
Gate Threshold Voltage ⁽¹⁾ ($V_{DS} = 10 \text{ Vdc}, I_D = 1600 \mu \text{Adc}$)	V _{GS(th)}	1	1.68	3	Vdc
Gate Quiescent Voltage ⁽²⁾ (V_{DD} = 50 Vdc, I _D = 150 mAdc, Measured in Functional Test)	V _{GS(Q)}	1.5	2.2	3.5	Vdc
Drain-Source On-Voltage ⁽¹⁾ (V _{GS} = 10 Vdc, I _D = 4 Adc)	V _{DS(on)}	_	0.28		Vdc
Dynamic Characteristics ⁽¹⁾			L.	I	1
Reverse Transfer Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C _{rss}		3.3		pF
Output Capacitance (V _{DS} = 50 Vdc \pm 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	147	—	pF
Input Capacitance (V _{DS} = 50 Vdc, V _{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C _{iss}	_	506		pF

100 µsec Pulse Width, 20% Duty Cycle

Power Gain	G _{ps}	22	24	26	dB
Drain Efficiency	η _D	65	67.5	—	%
Input Return Loss	IRL	—	-15	-9	dB

Each side of device measured separately.
 Measurement made with device in push-pull configuration.

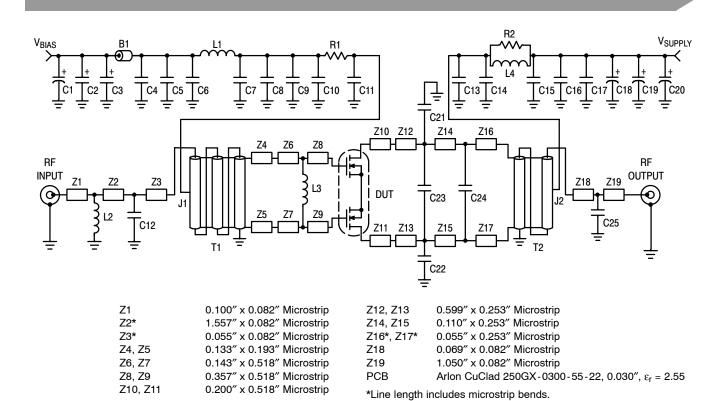
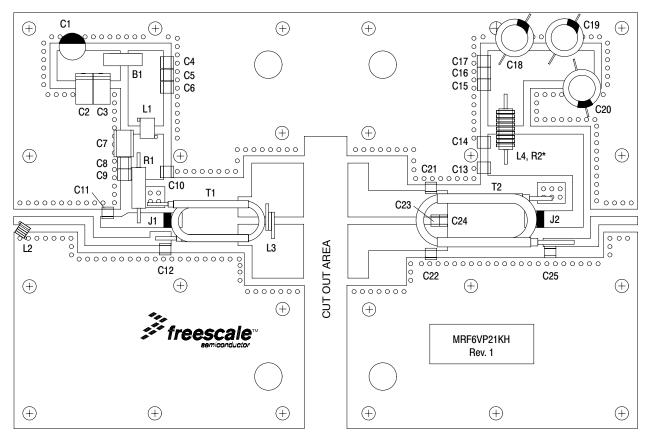


Figure 2	. MRF6VP21KHR6	Test Circuit	Schematic
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Part	Description	Part Number	Manufacturer
B1	95 Ω, 100 MHz Long Ferrite Bead	2743021447	Fair-Rite
C1	47 μF, 50 V Electrolytic Capacitor	lytic Capacitor 476KXM050M	
C2	22 μF, 35 V Tantalum Capacitor	T491X226K035AT	Kemet
C3	10 μF, 35 V Tantalum Capacitor	T491D106K035AT	Kemet
C4, C9, C17	10K pF Chip Capacitors	ATC200B103KT50XT	ATC
C5, C16	20K pF Chip Capacitors	ATC200B203KT50XT	ATC
C6, C15	0.1 μF, 50 V Chip Capacitors	CDR33BX104AKYS	Kemet
C7	2.2 μF, 50 V Chip Capacitor	C1825C225J5RAC	Kemet
C8	0.22 μF, 100 V Chip Capacitor	C1825C223K1GAC	Kemet
C10, C11, C13, C14	1000 pF Chip Capacitors	ATC100B102JT50XT	ATC
C12, C21, C22	27 pF Chip Capacitors	ATC100B270JT500XT	ATC
C18, C19, C20	470 μF, 63 V Electrolytic Capacitors	EKME630ELL471MK25S	Multicomp
C23, C24	68 pF Chip Capacitors	ATC100B680JT500XT	ATC
C25	4.7 pF Chip Capacitor	ATC100B4R7JT500XT	ATC
J1, J2	Jumpers from PCB to T1 and T2	Copper Foil	
L1	82 nH Inductor	1812SMS-82NJC	CoilCraft
L2	8 nH Inductor	A03TKLC	CoilCraft
L3	1 Turn Inductor, Red Coil	GA3092-AL	CoilCraft
L4*	10 Turn #18AWG Inductor, Handwound	Copper Wire	
R1	1 KΩ, 1/4 W Axial Leaded Resistor	CMF601000R0FKEK	Vishay
R2	20 Ω, 3 W Chip Resistor	CPF320R000FKE14	Vishay
T1	Balun	TUI-9	Comm Concepts
T2	Balun	TUO-4	Comm Concepts

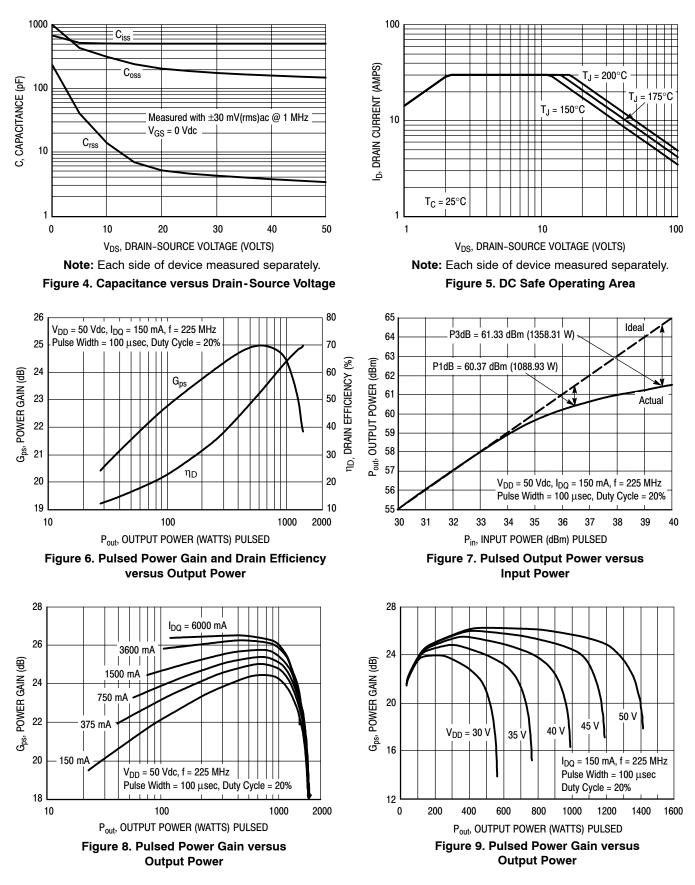
*L4 is wrapped around R2.



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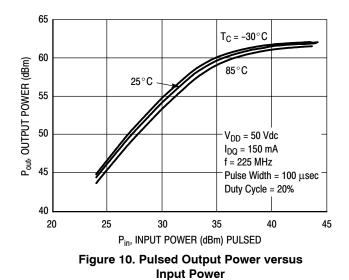
Figure 3. MRF6VP21KHR6 Test Circuit Component Layout

TYPICAL CHARACTERISTICS



MRF6VP21KHR6

TYPICAL CHARACTERISTICS



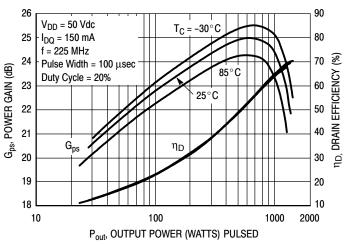


Figure 11. Pulsed Power Gain and Drain Efficiency versus Output Power

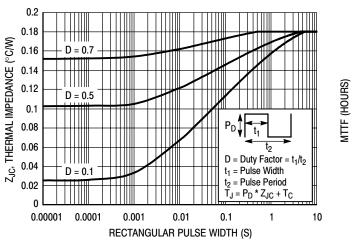
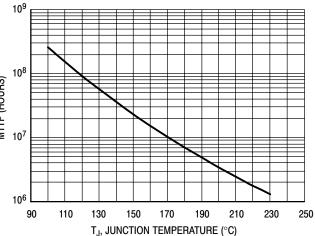


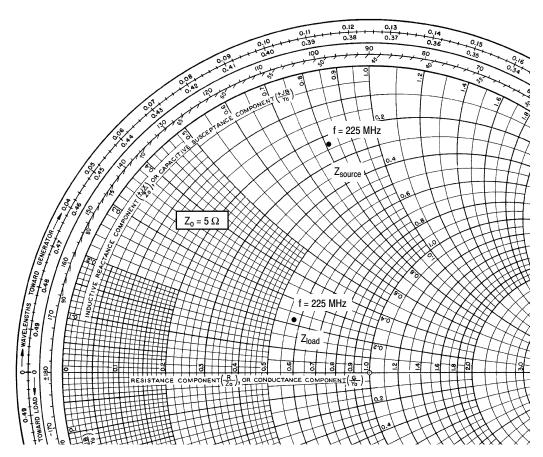
Figure 12. Maximum Transient Thermal Impedance



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 50 Vdc, P_{out} = 1000 W Peak, Pulse Width = 100 μ sec, Duty Cycle = 20%, and η_D = 67.5%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 13. MTTF versus Junction Temperature



V_{DD} = 50 Vdc, I_{DQ} = 150 mA, P_{out} = 1000 W Peak

f MHz	Z _{source} Ω	Z_{load}
225	1.16 + j4.06	2.86 + j1.10

 Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

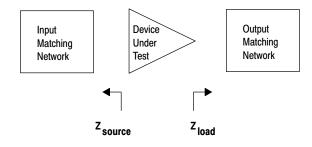
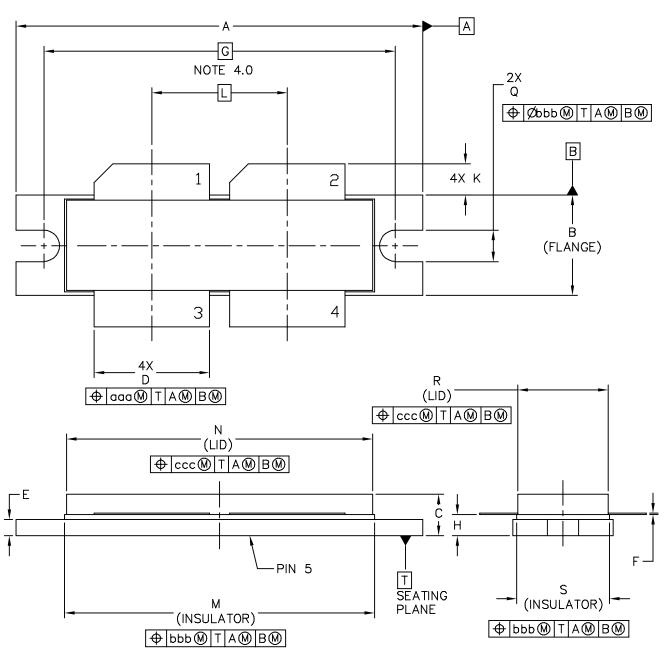


Figure 14. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



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NI-1230	CASE NUM	IBER: 375D-05	31 MAR 2005
	STANDARI	D: NON-JEDEC	

MRF6VP21KHR6

NOTES:

- 1.0 INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- 2. O CONTROLLING DIMENSION: INCH
- 3.0 DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.
- 4.0 RECOMMENDED BOLT CENTER DIMENSION OF 1.52 (38.61) BASED ON M3 SCREW.

STYLE 1: PIN 1 - DRAIN 2 - DRAIN 3 - GATE 4 - GATE 5 - SOURCE

	IN	INCH MI		LIMETER			INCH	М	ILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX	
A	1.615	1.625	41.02	41.28	Ν	1.218	1.242	30.9	4 31.55	
В	.395	.405	10.03	10.29	Q	.120	.130	3.05	5 3.3	
С	.150	.200	3.81	5.08	R	.355	.365	9.0	1 9.27	
D	.455	.465	11.56	11.81	S	.365	.375	9.2	7 9.53	
E	.062	.066	1.57	1.68						
F	.004	.007	0.1	0.18						
G	1.400	BSC	35	5.56 BSC	aaa		.013		0.33	
н	.082	.090	2.08	2.29	ьрр		.010		0.25	
К	.117	.137	2.97	3.48	ccc		.020		0.51	
L	.540	BSC	13	5.72 BSC						
М	1.219	1.241	30.96	31.52						
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TITLE:					DOCUMENT NO: 98ASB16977C REV: E			REV: E		
	NI-1230			CASE NUMBER: 375D-05 31 MAR 2			31 MAR 2005			
					STANDARD: NON-JEDEC					

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

• AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

• EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Jan. 2008	Initial Release of Data Sheet
1	Apr. 2008	 Corrected description and part number for the R1 resistor and updated R2 resistor to latest RoHS compliant part number in Table 5, Test Circuit Component Designations and Values, and updated the footnote to read "L4" versus "L3", p. 3. Added Fig. 12, Maximum Transient Thermal Impedance, p. 6
2	Sept. 2008	 Added Note to Fig. 4, Capacitance versus Drain-Source Voltage, to denote that each side of device is measured separately, p. 5 Updated Fig. 5, DC Safe Operating Area, to clarify that measurement is on a per-side basis, p. 5 Corrected Fig. 13, MTTF versus Junction Temperature, to reflect the correct die size and increased the MTTF factor accordingly, p. 6

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