

## FEATURES

- **LOW THERMAL RESISTANCE** — 1.4°C/W
- **CURRENT FOLDOVER PROTECTION** — NEW
- **HIGH TEMPERATURE VERSION** — PA12H
- **EXCELLENT LINEARITY** — Class A/B Output
- **WIDE SUPPLY RANGE** — ±10V to ±50V
- **HIGH OUTPUT CURRENT** — Up to ±15A Peak

## APPLICATIONS

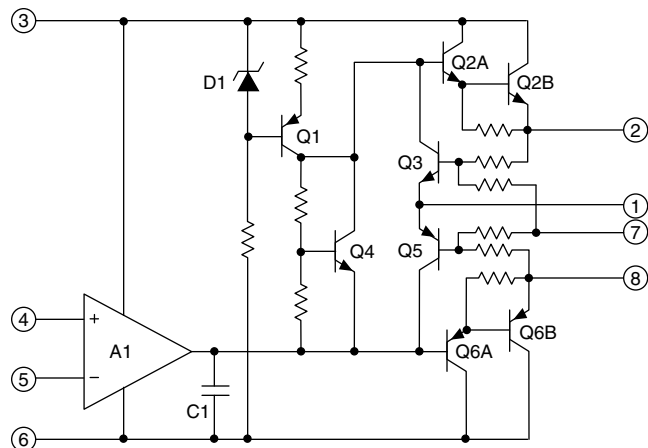
- **MOTOR, VALVE AND ACTUATOR CONTROL**
- **MAGNETIC DEFLECTION CIRCUITS UP TO 10A**
- **POWER TRANSDUCERS UP TO 100kHz**
- **TEMPERATURE CONTROL UP TO 360W**
- **PROGRAMMABLE POWER SUPPLIES UP TO 90V**
- **AUDIO AMPLIFIERS UP TO 120W RMS**

## DESCRIPTION

The PA12 is a state of the art high voltage, very high output current operational amplifier designed to drive resistive, inductive and capacitive loads. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. For continuous operation under load, a heatsink of proper rating is recommended. The PA12 is not recommended for gains below -3 (inverting) or +4 (non-inverting).

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

## EQUIVALENT SCHEMATIC



**8-PIN TO-3  
PACKAGE STYLE CE**

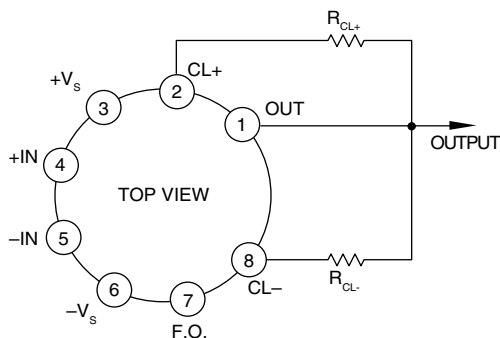
## POWER RATING

Not all vendors use the same method to rate the power handling capability of a Power Op Amp. APEX rates the internal dissipation, which is consistent with rating methods used by transistor manufacturers and gives conservative results. Rating delivered power is highly application dependent and therefore can be misleading. For example, the 125W internal dissipation rating of the PA12 could be expressed as an output rating of 250W for audio (sine wave) or as 440W if using a single ended DC load. Please note that all vendors rate maximum power using an infinite heatsink.

## THERMAL STABILITY

APEX has eliminated the tendency of class A/B output stages toward thermal runaway and thus has vastly increased amplifier reliability. This feature, not found in most other Power Op Amps, was pioneered by APEX in 1981 using thermistors which assure a negative temperature coefficient in the quiescent current. The reliability benefits of this added circuitry far outweigh the slight increase in component count.

## EXTERNAL CONNECTIONS



# PA12 • PA12A

ABSOLUTE MAXIMUM RATINGS  
SPECIFICATIONS



Product Innovation From



## ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, +Vs to -Vs	100V
OUTPUT CURRENT, within SOA	15A
POWER DISSIPATION, internal	125W
INPUT VOLTAGE, differential	±37V
INPUT VOLTAGE, common mode	±Vs
TEMPERATURE, pin solder -10s	300°C
TEMPERATURE, junction <sup>1</sup>	200°C
TEMPERATURE RANGE, storage	-65 to +150°C
OPERATING TEMPERATURE RANGE, case	-55 to +125°C

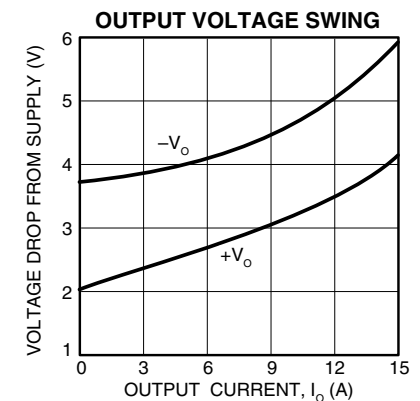
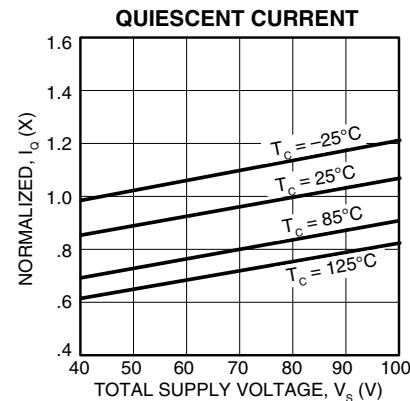
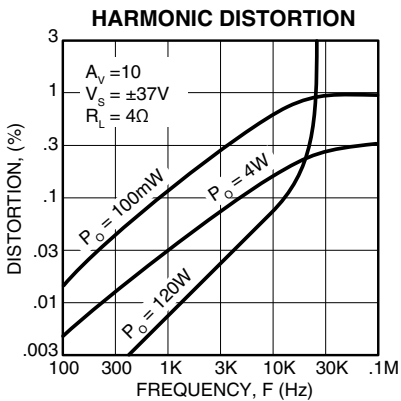
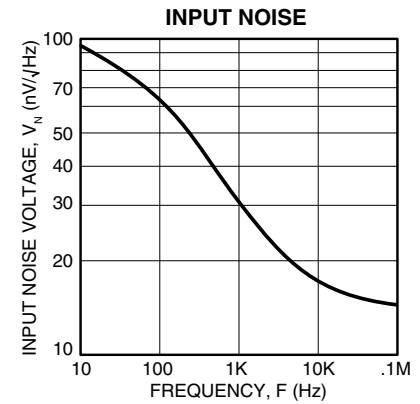
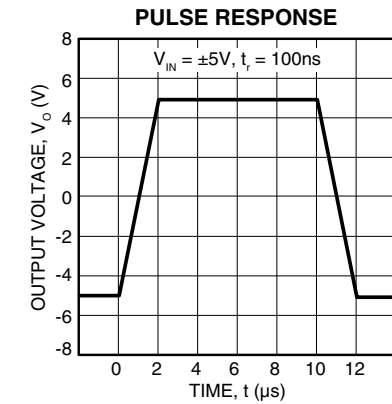
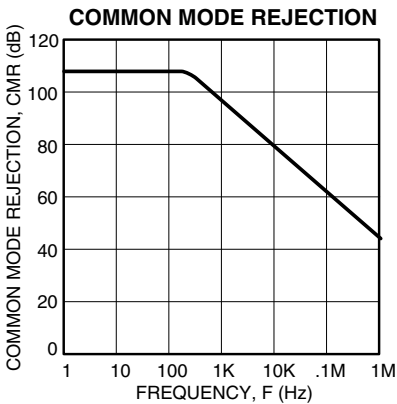
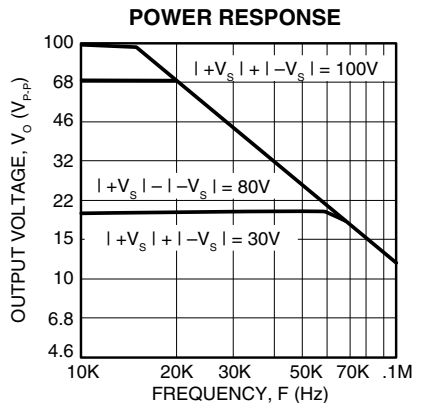
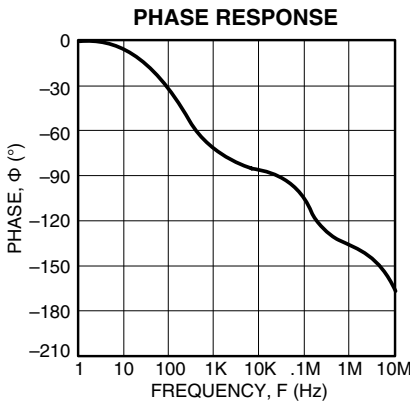
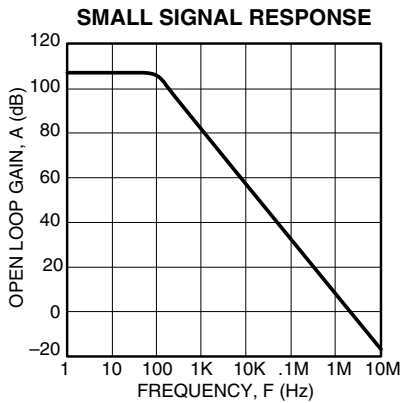
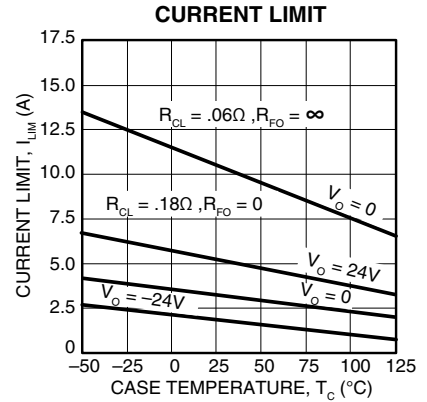
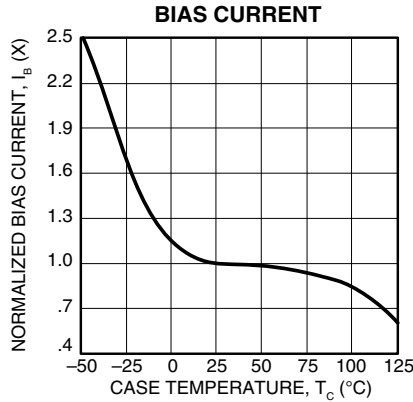
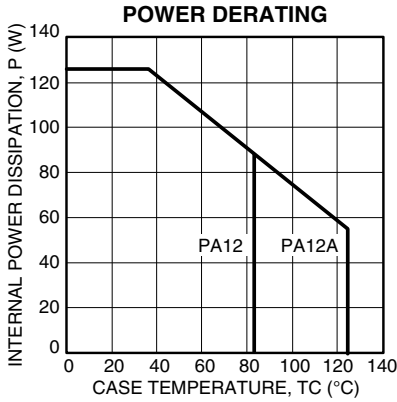
## SPECIFICATIONS

PARAMETER	TEST CONDITIONS <sup>2,5</sup>	PA12			PA12A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT</b>								
OFFSET VOLTAGE, initial	T <sub>c</sub> = 25°C		±2	±6		±1	±4	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	±40	μV/°C
OFFSET VOLTAGE, vs. supply	T <sub>c</sub> = 25°C		±30	±200		*	*	μV/V
OFFSET VOLTAGE, vs. power	T <sub>c</sub> = 25°C		±20			*		μV/W
BIAS CURRENT, initial	T <sub>c</sub> = 25°C		±12	±30		10	20	nA
BIAS CURRENT, vs. temperature	Full temperature range		±50	±500		*	*	pA/°C
BIAS CURRENT, vs. supply	T <sub>c</sub> = 25°C		±10			*		pA/V
OFFSET CURRENT, initial	T <sub>c</sub> = 25°C		±12	±30		±5	±20	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	T <sub>c</sub> = 25°C		200			*		MΩ
INPUT CAPACITANCE	T <sub>c</sub> = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE <sup>3</sup>	Full temperature range	±Vs -5	±Vs -3		*	*		V
COMMON MODE REJECTION, DC	Full temp. range, V <sub>CM</sub> = ±Vs -6V	74	100		*	*		dB
<b>GAIN</b>								
OPEN LOOP GAIN at 10Hz	T <sub>c</sub> = 25°C, 1KΩ load		110			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 8Ω load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T <sub>c</sub> = 25°C, 8Ω load		4			*		MHz
POWER BANDWIDTH	T <sub>c</sub> = 25°C, 8Ω load	13	20		*	*		kHz
PHASE MARGIN, A <sub>v</sub> = +4	Full temp. range, 8Ω load		20			*		°
<b>OUTPUT</b>								
VOLTAGE SWING <sup>3</sup>	T <sub>c</sub> = 25°C, PA12 = 10A, PA12A = 15A	±Vs -6			*			V
VOLTAGE SWING <sup>3</sup>	T <sub>c</sub> = 25°C, I <sub>o</sub> = 5A	±Vs -5			*			V
VOLTAGE SWING <sup>3</sup>	Full temp. range, I <sub>o</sub> = 80mA	±Vs -5			*			V
CURRENT, peak	T <sub>c</sub> = 25°C	10			15			A
SETTLING TIME to .1%	T <sub>c</sub> = 25°C, 2V step		2			*		μs
SLEW RATE	T <sub>c</sub> = 25°C	2.5	4		*	*		V/μs
CAPACITIVE LOAD	Full temperature range, A <sub>v</sub> = 4			1.5			*	nF
CAPACITIVE LOAD	Full temperature range, A <sub>v</sub> > 10			SOA			*	
<b>POWER SUPPLY</b>								
VOLTAGE	Full temperature range	±10	±40	±45	*	*	±50	V
CURRENT, quiescent	T <sub>c</sub> = 25°C		25	50		*	*	mA
<b>THERMAL</b>								
RESISTANCE, AC, junction to case <sup>4</sup>	T <sub>c</sub> = -55 to +125°C, F > 60Hz		.8	.9		*	*	°C/W
RESISTANCE, DC, junction to case	T <sub>c</sub> = -55 to +125°C		1.25	1.4		*	*	°C/W
RESISTANCE, junction to air	T <sub>c</sub> = -55 to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	-25		+85	-55		+125	°C

- NOTES: \* The specification of PA12A is identical to the specification for PA12 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
  2. The power supply voltage for all tests is ±40, unless otherwise noted as a test condition.
  3. +Vs and -Vs denote the positive and negative supply rail respectively. Total Vs is measured from +Vs to -Vs.
  4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
  5. Full temperature range specifications are guaranteed but not 100% tested.

### CAUTION

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



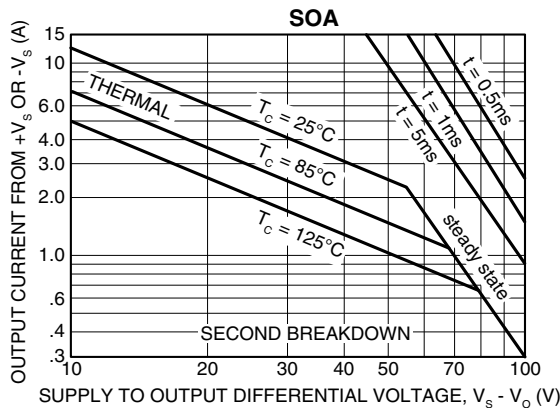
## GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit [www.apexmicrotech.com](http://www.apexmicrotech.com) for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

## SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Capacitive and dynamic\* inductive loads up to the following maximum are safe with the current limits set as specified.

±V <sub>s</sub>	CAPACITIVE LOAD		INDUCTIVE LOAD	
	I <sub>LIM</sub> = 5A	I <sub>LIM</sub> = 10A	I <sub>LIM</sub> = 5A	I <sub>LIM</sub> = 10A
50V	200µF	125µF	5mH	2.0mH
40V	500µF	350µF	15mH	3.0mH
35V	2.0mF	850µF	50mH	5.0mH
30V	7.0mF	2.5mF	150mH	10mH
25V	25mF	10mF	500mH	20mH
20V	60mF	20mF	1,000mH	30mH
15V	150mF	60mF	2,500mH	50mH

\*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I<sub>LIM</sub> = 15A or 25V below the supply rail with I<sub>LIM</sub> = 5A while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive

load and short circuits to the supply rail or common if the current limits are set as follows at T<sub>c</sub> = 25°C:

±V <sub>s</sub>	SHORT TO ±V <sub>s</sub> C, L, OR EMF LOAD	SHORT TO COMMON
50V	.30A	2.4A
40V	.58A	2.9A
35V	.87A	3.7A
30V	1.5A	4.1A
25V	2.4A	4.9A
20V	2.9A	6.3A
15V	4.2A	8.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

## CURRENT LIMITING

Refer to Application Note 9, "Current Limiting", for details of both fixed and foldover current limit operation. Visit the Apex web site at [www.apexmicrotech.com](http://www.apexmicrotech.com) for a copy of the Power Design spreadsheet (Excel) which plots current limits vs. steady state SOA. Beware that current limit should be thought of as a +/-20% function initially and varies about 2:1 over the range of -55°C to 125°C.

For fixed current limit, leave pin 7 open and use equations 1 and 2.

$$R_{CL} = 0.65/I_{CL} \quad (1)$$

$$I_{CL} = 0.65/R_{CL} \quad (2)$$

Where:

I<sub>CL</sub> is the current limit in amperes.

R<sub>CL</sub> is the current limit resistor in ohms.

For certain applications, foldover current limit adds a slope to the current limit which allows more power to be delivered to the load without violating the SOA. For maximum foldover slope, ground pin 7 and use equations 3 and 4.

$$I_{CL} = \frac{0.65 + (V_o * 0.014)}{R_{CL}} \quad (3)$$

$$R_{CL} = \frac{0.65 + (V_o * 0.014)}{I_{CL}} \quad (4)$$

Where:

V<sub>o</sub> is the output voltage in volts.

Most designers start with either equation 1 to set R<sub>CL</sub> for the desired current at 0v out, or with equation 4 to set R<sub>CL</sub> at the maximum output voltage. Equation 3 should then be used to plot the resulting foldover limits on the SOA graph. If equation 3 results in a negative current limit, foldover slope must be reduced. This can happen when the output voltage is the opposite polarity of the supply conducting the current.

In applications where a reduced foldover slope is desired, this can be achieved by adding a resistor (R<sub>FO</sub>) between pin 7 and ground. Use equations 4 and 5 with this new resistor in the circuit.

$$I_{CL} = \frac{0.65 + \frac{V_o * 0.14}{10.14 + R_{FO}}}{R_{CL}} \quad (5)$$

$$R_{CL} = \frac{0.65 + \frac{V_o * 0.14}{10.14 + R_{FO}}}{I_{CL}} \quad (6)$$

Where:

R<sub>FO</sub> is in K ohms.

Copyright © 2007 Cirrus Logic, Inc.  
All rights reserved  
Printed in the USA

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided 'as is' without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied upon is current and complete. All products are sold subject to the terms and conditions of sales supplied at the time of order acknowledgement, including those pertaining to warranty, indemnification, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and, by furnishing this information, Cirrus grants no license, express or implied, under any patents. Mask work rights, copyrights, trademarks, trade secrets, or other intellectual property rights. No part of this publication may be copied, reproduced, stored in a retrieval system, or transmitted, in any form or by any means (electronic, mechanical, photographic, or otherwise) unless distributed in its entirety with all copyright notices attached. No part of this publication may be used as a basis for manufacture or sale of any items without the prior

written consent of Cirrus. Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("critical applications"). Cirrus products are not designed, authorized, or warranted to be suitable for use in products surgically implanted into the body, automotive safety or security devices, life-support products or other critical applications, inclusion of Cirrus products in such applications is understood to be fully at the customer's risk and Cirrus disclaims and makes no warranty of merchantability and fitness for particular purpose, with regard to any Cirrus product that is used in such a manner. If the customer uses or permits the use of Cirrus products in critical products in critical applications, customer agrees, by such use, to fully indemnify Cirrus, its officers, directors, employees, distributors and other agents from any and all liability, including attorneys' fees and costs that may result from or arise in connection with these uses.

Cirrus Logic, Cirrus, the Cirrus Logic logo designs, Apex, and Apex Precision Power are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.

CIRRUS LOGIC, INC. • 5980 N SHANNON ROAD, TUCSON, AZ 85741 USA • TELEPHONE (520) 690-8600  
APPLICATIONS SUPPORT (800) 546-2739 • FAX (520) 888-3329 • EMAIL [support@cirrus.com](mailto:support@cirrus.com)  
ORDERS (520) 690-8601 • FAX (520) 690-7749 • EMAIL [teamsales@cirrus.com](mailto:teamsales@cirrus.com)