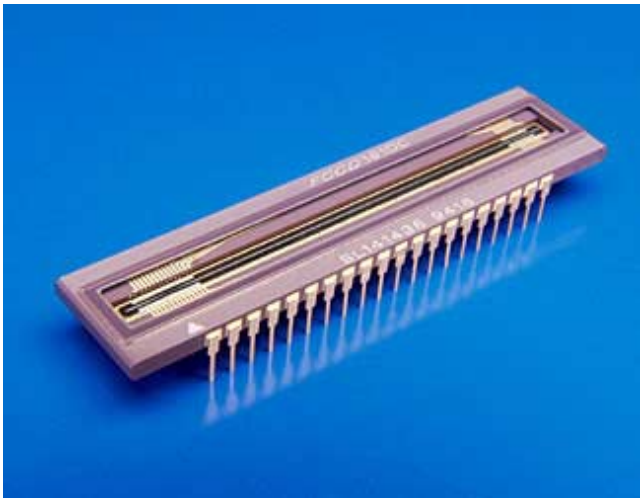
CCD 191
6000 Element
Linear Image Sensor

FEATURES

- **6000 x 1 photosite array**
- **10 µm x 10µm photosites on 10µm pitch**
- **Anti-blooming and integration control**
- **Enhanced spectral response (particularly in the blue region)**
- **Excellent low-light-level performance**
- **Low dark signal**
- **Very high responsivity**
- **High speed operation**
- **Dynamic range typical: 15000:1**
- **Over 3 V peak-to-peak outputs**
- **Special selection available - consult factory**
- **AR coated window**



GENERAL DESCRIPTION

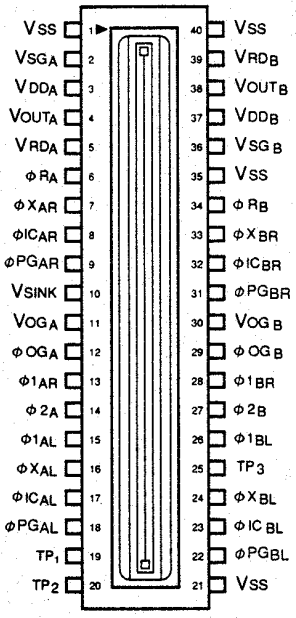
The CCD191 is a 6000 element line image sensor designed for scanning applications which require very high resolution, high sensitivity and very wide dynamic range. Incorporation of on-chip anti-blooming and integration controls allow the CCD191 to be extremely useful in industrial measurement and control environments, or in environments where lighting conditions are difficult to control.

The CCD191 is a third generation device having an overall improved performance compared with first and second generation devices, including enhanced blue response and excellent low light level performance. The photoelement size is 10µm (0.39 mils) x 10µm (0.39 mils) on 10µm (0.39 mils) centers. The device is manufactured using Fairchild Imaging's advanced charge-coupled device n-channel isoplanar buried-channel technology.

PIN NAME	DESCRIPTION
$V_{SG\ (A,B)}$	Amp Signal Grounds
V_{OUT_A}	Output Amp—A Source
Φ_{R_A}	Reset Gate—A
V_{RD_A}	Reset Drain—A
$\Phi_{OG(A,B)}$	Output Clock Gates
V_{OG_A}	Output DC Gate—A
$\Phi_{X\ (AR,AL,BR,BL)}$	Transfer Clocks (A & B sides, left & right)*
Φ_{2A}, Φ_{2B} Φ_{1A}, Φ_{1B}	Transport Clocks (A & B)
$\Phi_{IC\ (AR,AL,BR,BL)}$	Integration Control (A & B sides, left & right)*
$\Phi_{PG\ (AR,AL,BR,BL)}$	Photogates (A & B sides, left & right)*
TP1, TP2, TP3	Test Points
V_{SINK}	Anti Blooming Sink
V_{OG_B}	Output DC Gate—B
V_{RD_B}	Reset Drain—B
Φ_{R_B}	Reset Gate—B
V_{OUT_B}	Output Amp—B Source
$V_{DD(A,B)}$	Output Amp Drains
V_{SS}	Substrate

NOTE: Left & right pins must be connected together. Example: ϕPG_{AR} and ϕPG_{AL}

PIN DIAGRAM



Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500

FUNCTIONAL DESCRIPTION

The CCD191 consists of the following functional elements illustrated in the Block Diagram and Circuit Diagram.

Photosites — A row of 6000 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Two Transfer Gate — Gate structures adjacent to the row of image sensor elements. The charge packets accumulated in the photosites are transferred in parallel via the transfer gates (ϕX) to the transport shift registers whenever the transfer gate voltages go high. Alternate charge packets are transferred to the A and B transport registers.

Two Analog Shift Registers — The transport shift registers are used to move the light generated charge packets delivered by the transfer gates. (ϕ1A, ϕ1B, ϕ2A, ϕ2B) serially to the charge detector/amplifier. The parallel layout of the last elements of the two transport registers provides for simultaneous delivery of charge packets at the output amplifiers.

A Gated Charge Detector/Amplifier — Charge packets are transported to a precharge capacitor whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the input gate of the two-stage NMOS amplifiers producing a signal at the output "VOUT" pin. Before each charge packet is sensed, a reset clock (ϕRA, ϕRB) recharges the input node capacitor to a fixed voltage (VRDA, VRDB)

Integration and Anti-Blooming Controls — In many applications the dynamic range in parts of the image is larger than the dynamic range of the CCD, which may cause more electrons to be generated in the photosite area than can be stored in the CCD shift register. This is particularly common in industrial inspection and satellite applications. The excess electrons generated by bright illumination tend to "bloom" or "spill over" to neighboring pixels along the shift register, thus "smearing" the information. This smearing can be eliminated using two methods:

Anti-Blooming Operation:

A DC voltage applied to the integration control gate (approximately 1 to 3 volts) will cause excess charge generated in the photosites to be diverted to the anti-blooming sink (VSINK) instead of to the shift registers. This acts as a "clipping circuit" for the CCD output.

Integration Control Operation:

Variable integration times which are less than the CCD exposure time may be attained by supplying a clock to the integration control gate. Clocking ϕIC reduces the integration time from tEXPOSURE to tINT. Greater than 10:1 reduction in average photosite signal can be achieved with integration control.

The integration-control and anti-blooming features can be implemented simultaneously. This is done by setting the ϕIC, clock-low level to approximately 1 to 3 volts.

DEFINITION OF TERM

Charge-Coupled Device — A Charge-coupled device is a semiconductor device in which finite isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Prescan Reference — Video output level generated from shift register cells which provides a reference voltage equivalent to device operation in the dark. This permits use of external DC restoration circuitry.

Dynamic Range — The saturation exposure divided by the RMS temporal noise equivalent exposure. Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times RMS noise.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal to the RMS noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosites integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-uniformity — The difference of the response levels of the most and the least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements.

Dark Signal — The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and highly sensitive to temperature.

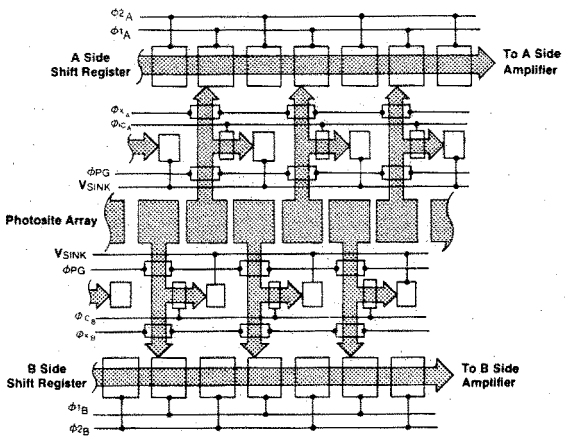
Saturation Output Voltage — The maximum usable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Integration Time — The time interval between the falling edge of any two successive transfer pulses (ϕX). The integration is the time allowed for the photosites to collect charge.

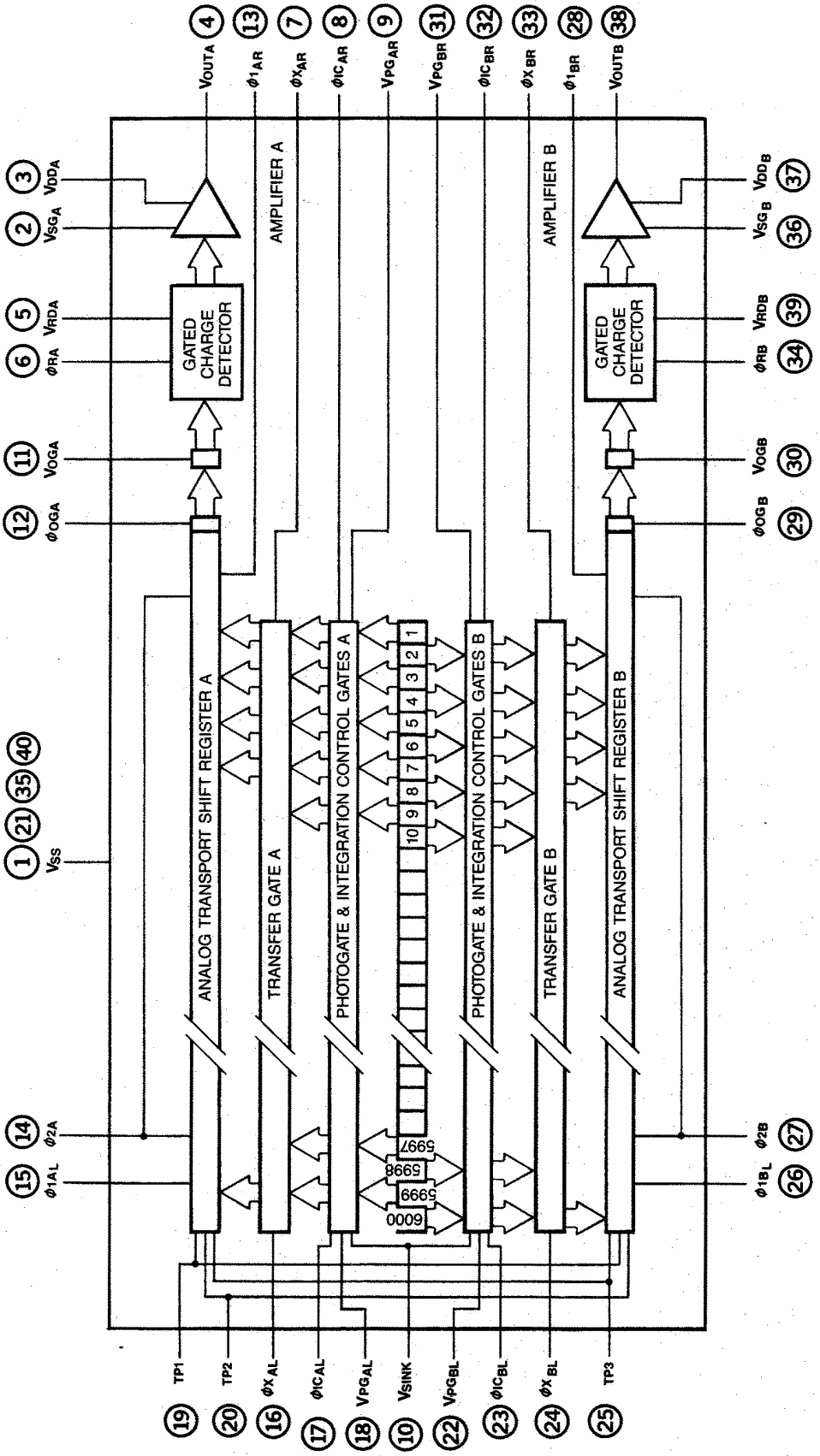
Exposure Time - The time interval between the falling edge of the two transfer pulses (ϕX) shown in the timing diagram. The exposure time is the time between transfers of signal charge from the photosites into the transport registers.

Pixel - A picture element (photosite).

CCD191 CIRCUIT DIAGRAM



CCD191 BLOCK DIAGRAM



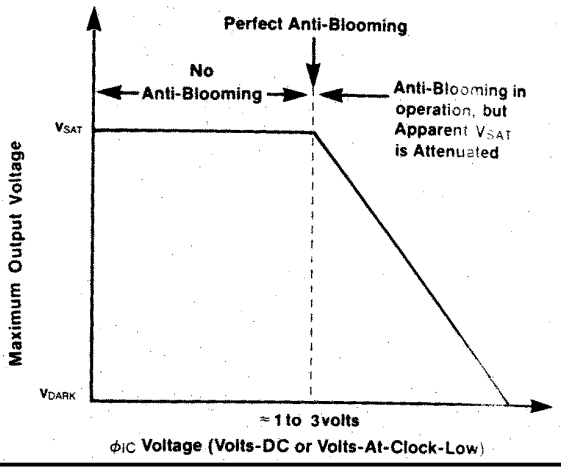
Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500

ABSOLUTE MAXIMUM RATINGS
(above which useful life may be impaired)

Storage Temperature		−25°C to +125°C
Operating Temperature		−25°C to +70°C
CCD 191: Pins 2, 36		0V
	Pins 1, 21, 40, 35	−3.0V to 0V
	Pins 4, 38	See Caution Note
	All other pins	−0.3V to +18V

CAUTION NOTE:
These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $V_{OUT_{A+B}}$ to V_{SS} or V_{DD} during operation of the devices. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

MAXIMUM OUTPUT VOLTAGE VS ϕIC VOLTAGE



DC CHARACTERISTICS: T_P = 25°C (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITION
		MIN	TYP	MAX		
V_{DD}	Output Amplifier Drain Supply Voltage	16.5	17.0	17.5	V	
$V_{RD\ (A+B)}$	Output Reset Drain Supply Voltages	16.5	17.0	17.5	V	
V_{SINK}	Anti-Blooming Sink Voltage	16.5	17.0	17.5	V	
V_{PG}	Photogate Bias Voltage	1.5	2.0	2.5	V	Note 11
$V_{OG\ (A+B)}$	Output DC Gate Voltages	5.5	6.0	6.5	V	
TP_1, TP_2		0.0	0.3	0.5	V	
TP_3		16.5	17.0	17.5	V	
V_{SG}	Amplifier Signal Ground	0.0	0.3	0.5	V	
V_{SS}	Substrate Bias	−2.0	−1.0	0.0	V	Note 2
I_{DD}	Output Amplifier Drain Supply Current	6.0	10.0	15.0	mA	

CLOCK CHARACTERISTICS: T_P = 25°C (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITION
		MIN	TYP	MAX		
$V\phi_{X\ HIGH}$	Transfer Clock HIGH	14.5	15.0	15.5	V	Note 3
$V\phi_{1\ HIGH\ (A+B)}$ $V\phi_{2\ HIGH\ (A+B)}$	Transport Clock HIGH	7.5	8.0	8.5	V	Note 3
$V\phi_{R\ HIGH\ (A+B)}$ $V\phi_{OG\ HIGH\ (A+B)}$	Reset Clock HIGH	14.5	15.0	15.5	V	Note 3
$V\phi_{IC\ HIGH}$	Integration Control Clock HIGH		10.0		V	Note 3
$V\phi_{IC\ LOW}$	Integration Control Clock LOW		2.0		V	Note 2, 3
$V\phi_{X\ LOW}$	Transfer Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi_{1\ LOW\ (A+B)}$	Transport Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi_{2\ LOW\ (A+B)}$	Transport Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi_{R\ LOW\ (A+B)}$	Reset Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V\phi_{OG\ LOW\ (A+B)}$	Output Clock Gate LOW	0.0	0.3	0.7	V	Note 2,3
f_{data} max	Maximum Output Data Rate	2.0	5.0		MHz	Note 6

Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500

AC CHARACTERISTICS: T_P = 25°C, (Note 1), f_{data} = 2.0MHz, t_{int} = 10ms, Light Source = 2854°K + 2.0mm thick Schott BG-38 and OCLI WBHM Filters (Note 4).

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITION
		MIN	TYP	MAX		
DR	Dynamic Range (P-P Noise)		3000:1			
	(RMS Noise)		15000:1			
NEE	RMS Noise Equivalent Exposure		0.00003		μJ/cm²	
SE	Saturation Exposure		0.50		μJ/cm²	
CTE	Charge Transfer Efficiency	0.99999	0.999999			Note 6
V_O	Output DC Level	6.0	10.0	12.0	V	
Z	Output Impedance		1		kΩ	
P	On-Chip Power Dissipation Amplifiers		170	250	mW	
N	Peak-to-Peak Temporal Noise		1.0		mV	

PERFORMANCE CHARACTERISTICS: T_P = 25°C (Note 1, 7), f_{data} = 2.0MHz, t_{int} = 10ms, Light Source = 2854°K + 2.0mm thick Schott BG-38 and OCLI WBHM filters (Note 4).

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITION
		MIN	TYP	MAX		
PRNU*	Photoresponse Non-Uniformity:					
	Peak-to-Peak		90	240	mV	
	Peak-to-Peak without single pixel and Positive and Negative Pulses		60		mV	
	Single-pixel Positive Pulses		55		mV	
	Single-pixel Negative Pulses		55		mV	
M Video	Video Mismatch		75	225	mV	Note 7
M DC	DC Mismatch		0.5	2.0	V	Note 8
DS	Dark Signal:					Notes 9
	DC Component		2	5	mV	
	Low Frequency Component		2	5	mV	
SPDSNU	Single Pixel DS Non-Uniformity		2	5	mV	Note 10
R	Responsivity	4.0	6.0	12.0	V/μJ/cm²	
V_{SAT}	Saturation Output Voltage	1.5	3.0	4.5	V	

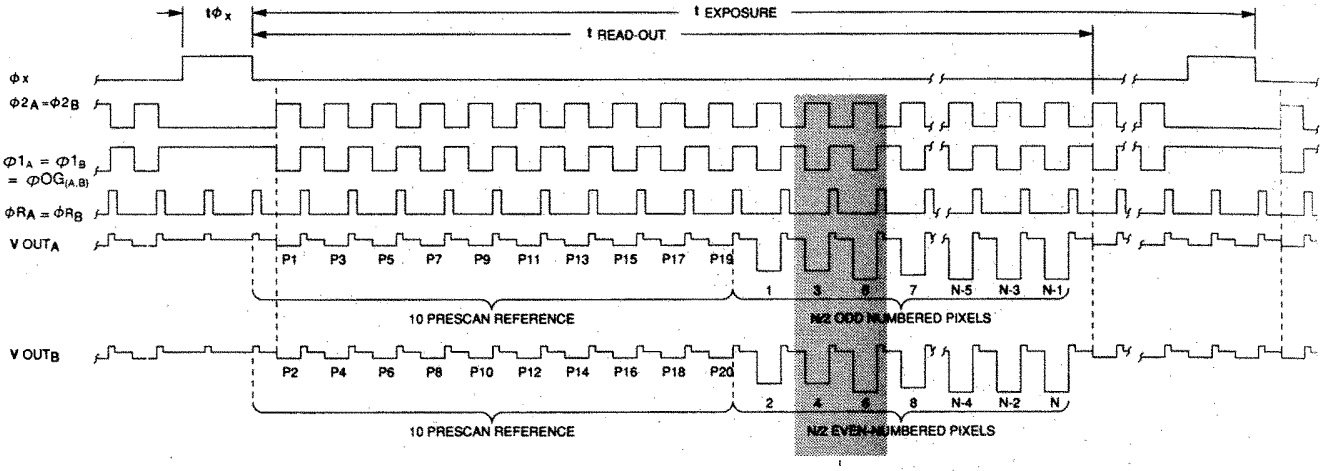
*All PRNU measurements are taken at approximately 80% of V_{SAT} using an f/5.0 lens and exclude the output from the first and last elements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate the PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU. These characteristics are based on 1200 mV output (80% of minimum V_{SAT}).

NOTES:

1. T_P is defined as the package temperature measured on a copper block in good thermal contact with the entire backside of the package.
2. Negative transients on any clock pin going below 0.0 volts may cause charge injection, which results in an increase in apparent DS. Adjusting V_{SS} to a more negative voltage than the clock low voltages will reduce charge injection, if present.
3. $C\phi_{XA} = C\phi_{XB} = C\phi_{ICA} = C\phi_{ICB}$ = 450pF, $C\phi_{1A} = C\phi_{1B} = C\phi_{2A} = C\phi_{2B}$ = 800pF $C\phi_{RA} = C\phi_{RB} = C\phi_{OGA} = C\phi_{OGB}$ = 5pF
4. OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror.
5. The minimum clock frequency is limited by increases in dark signal.
6. CTE is the measurement for a one-stage transfer.
7. Video mismatch is the difference in AC amplitudes between V_{OUT} A and V_{OUT} B under uniform illumination. It can be eliminated by attenuation/amplification of one of the video inputs.
8. DC mismatch is the difference in DC output level V_O between V_{OUT} A and V_{OUT} B.
9. Dark signal component approximately doubles for every 5 to 15°C in T_P.
10. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 5 to 15°C increase in T_P.
11. The HIGH level of the Photogate Clock can actually be as high as 16V. However, increasing the high level of this clock may also increase the photosite dark signal.
12. Metal back plate electrically tied to V_{SS}.
13. See "Anti-Blooming" and "Integration Control" under "Functional Description" for additional information; also see Application Note "Anti-blooming and Integration Control."

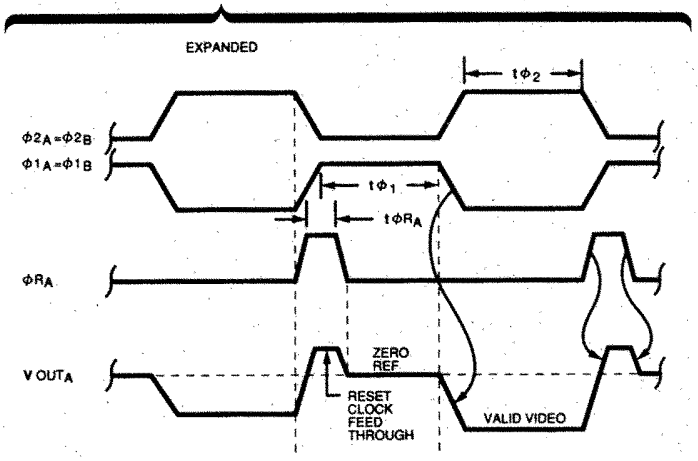
Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500

TIMING DIAGRAM

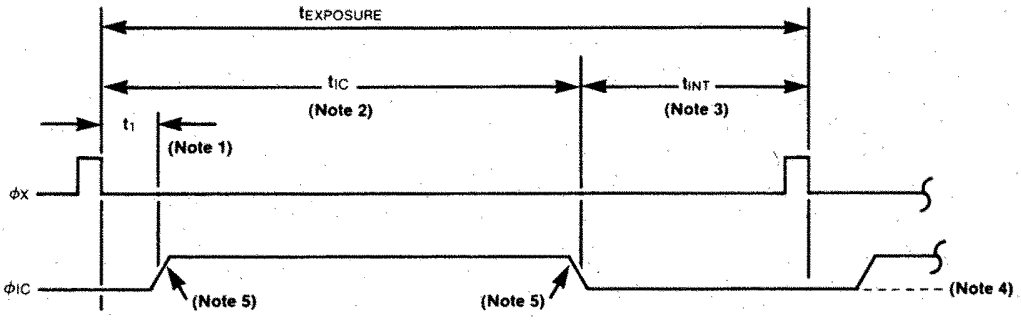


NOTES:

1. Timing requirements for ϕ_1 and ϕ_2:
   a. 50 ± 10% duty cycle, ~180° out of phase (See 1b).
   b. Φ_{OG} and Φ_2 clocks must cross at ≥4V on the falling edge of Φ_2. (Both Φ_{OG} and Φ_2 must not be <4V simultaneously.)
   c. $(0.1 \cdot t\phi_2) \leq (t_{rise} = t_{fall}) < (0.4 \cdot t\phi_2)$
2. Timing requirements for ϕR_A and ϕR_{2B}:
   a. $20ns \leq (t_{rise} = t_{fall}) < (0.3 \cdot t\phi_R)$
   b. $30ns < (t\phi R_A = t\phi R_B) < t\phi_2$
   c. t_{fall} time of ϕR_A must not overlap t_{rise} of ϕR_A
   d. t_{fall} time of ϕR_B must not overlap t_{rise} of ϕR_B
3. Integration Control Clock (ϕIC) has been omitted from these timing diagrams for clarity. See "Integration Control Timing" diagram
4. Timing requirements for ϕ_X:
   a. $t\phi_X \geq 0.1\mu s$
   b. t_{rise} and t_{fall} times of ϕ_X must not overlap t_{rise} or t_{fall} times of ϕ_1 or ϕ_2.



INTEGRATION CONTROL TIMING DIAGRAM



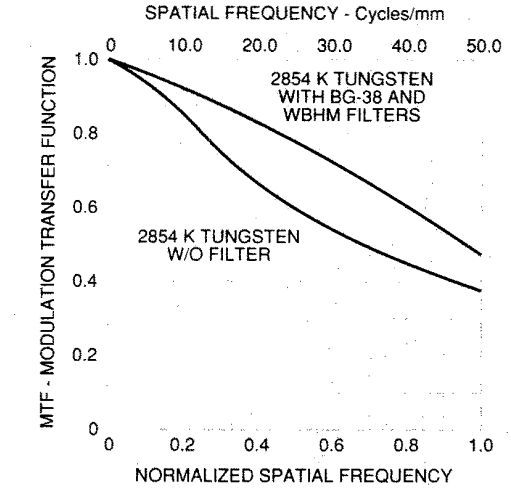
NOTES:

1. $t_1 > (t_{fall}$ of $\phi X)$.
2. All charge generated in photosites during t_{IC} is dumped in V_{SINK}.
3. All charge generated in photosites < Q_{SAT} during t_{INT} is transferred into the shift registers during ϕX clock-high period. Photosite charge > Q_{SAT} (shift reg.) generated during t_{INT} goes into V_{SINK} if anti-blooming voltage is optimized.
4. ϕIC clock-low ≈ 1 to 3 volts will give best anti-blooming operation.
5. ϕIC t_{rise} & $t_{fall} > 4\mu s$ to minimize clock coupling of ϕIC, into V_{OUT}.
6. To eliminate integration control, but retain anti-blooming $\phi IC \approx +2$ VDC.
7. To eliminate both integration control and anti-blooming, ϕIC = 0VDC or V_{SS} (-1 V).
8. To use integration control without anti-blooming, use ϕIC clock-low = 0.0 to 0.7 volts and ϕIC clock-high = same range as ϕX clock-high voltage.

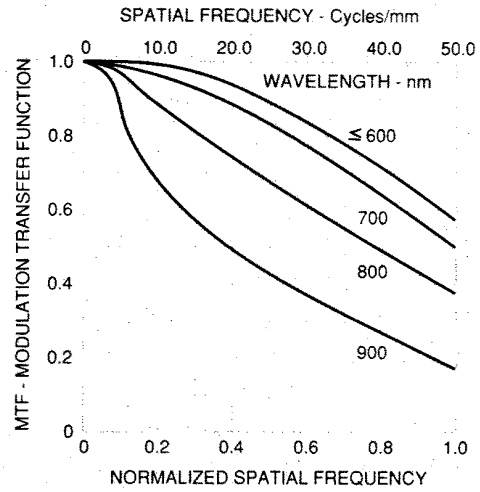
Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500

TYPICAL PERFORMANCE CURVES

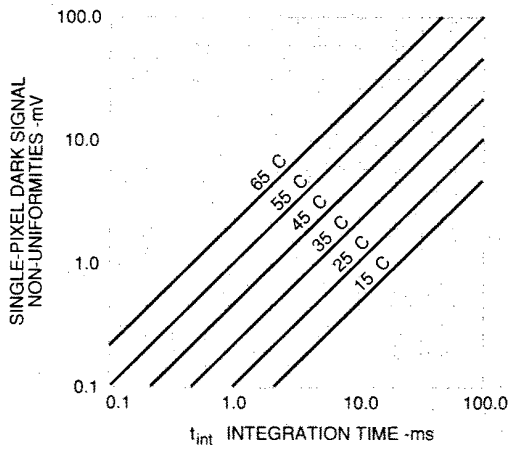
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



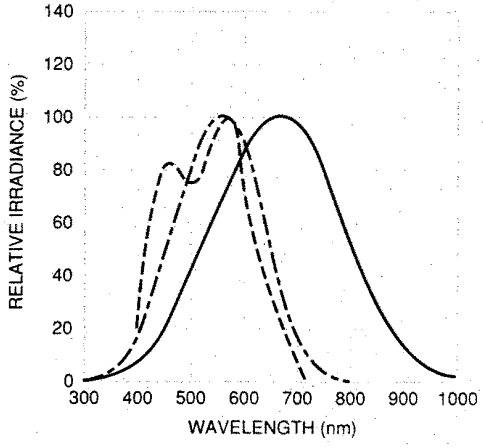
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME

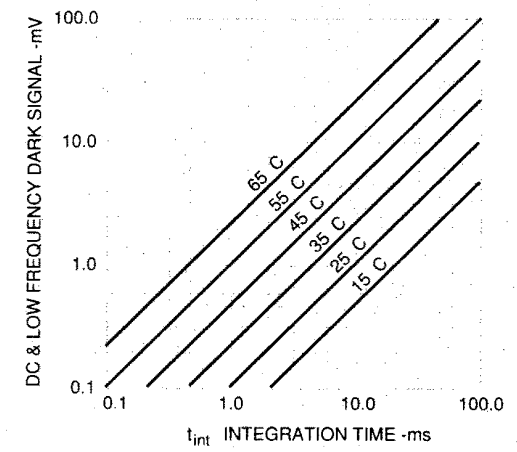


*** RELATIVE RADIANT FLUX VS WAVELENGTH**

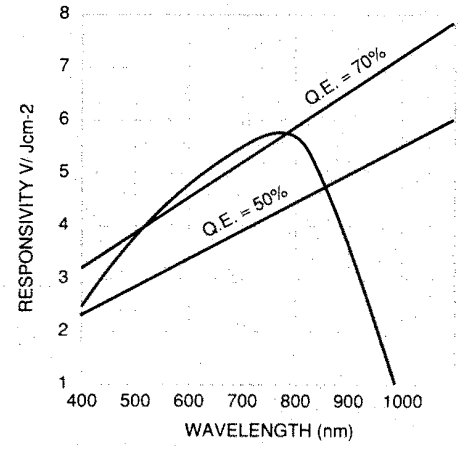


— — — TYPICAL "DAYLIGHT FLUORESCENT" BULB
— - — - 2854 K LIGHT SOURCE + WBM + 2.0 mm THICK BG-38
——— 2854 K LIGHT SOURCE + 3.0 mm THICK 1-75

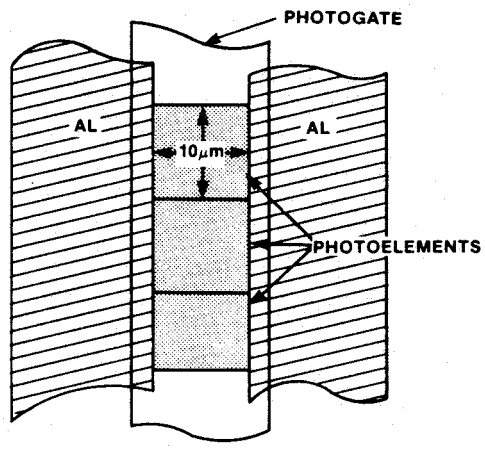
DC AND LOW-FREQUENCY DARK SIGNAL, VS INTEGRATION TIME



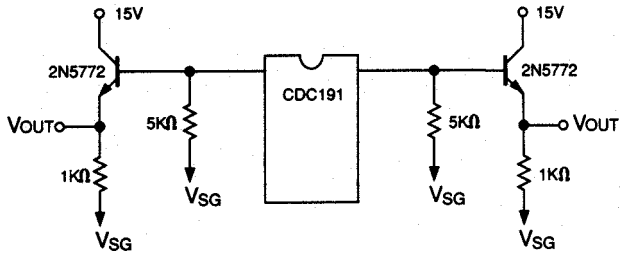
TYPICAL SPECTRAL RESPONSE



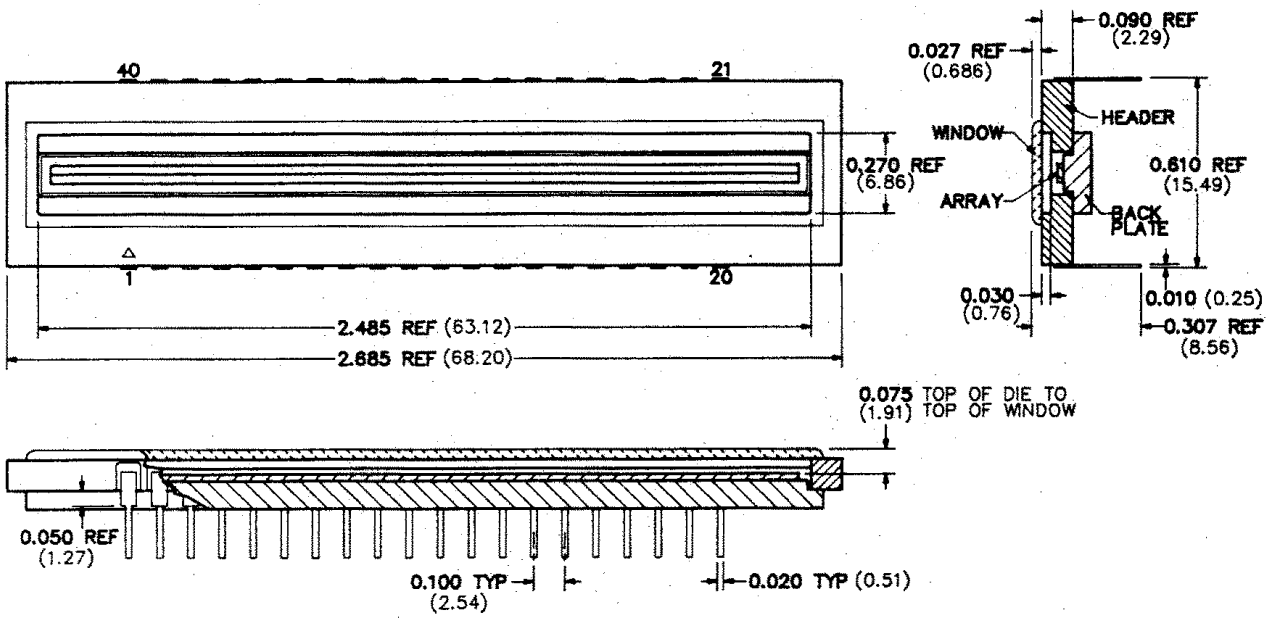
PHOTOELEMENT DIMENSIONS



TEST LOAD CONFIGURATIONS



CCD191 PACKAGE OUTLINE



DEVICE CARE AND OPERATION

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with deionized water. Allow the glass to dry, preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal dc and low frequency components approximately double for every 5º C temperature increase and single-pixel dark signal non-uniformities approximately double for every 8º C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION

Order CCD191DC where “D” stands for a ceramic package and “C” for commercial temperature range.

Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, CA 95035 • (800)325-6975 • (408) 433-2500