HD74LS195A

4-bit Parallel-Access Shift Register

REJ03D0457–0300
Rev.3.00
Jul.15.2005

This 4-bit register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift / load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

- Parallel (broadside) load
- Shift (in the direction Q_A toward Q_D)

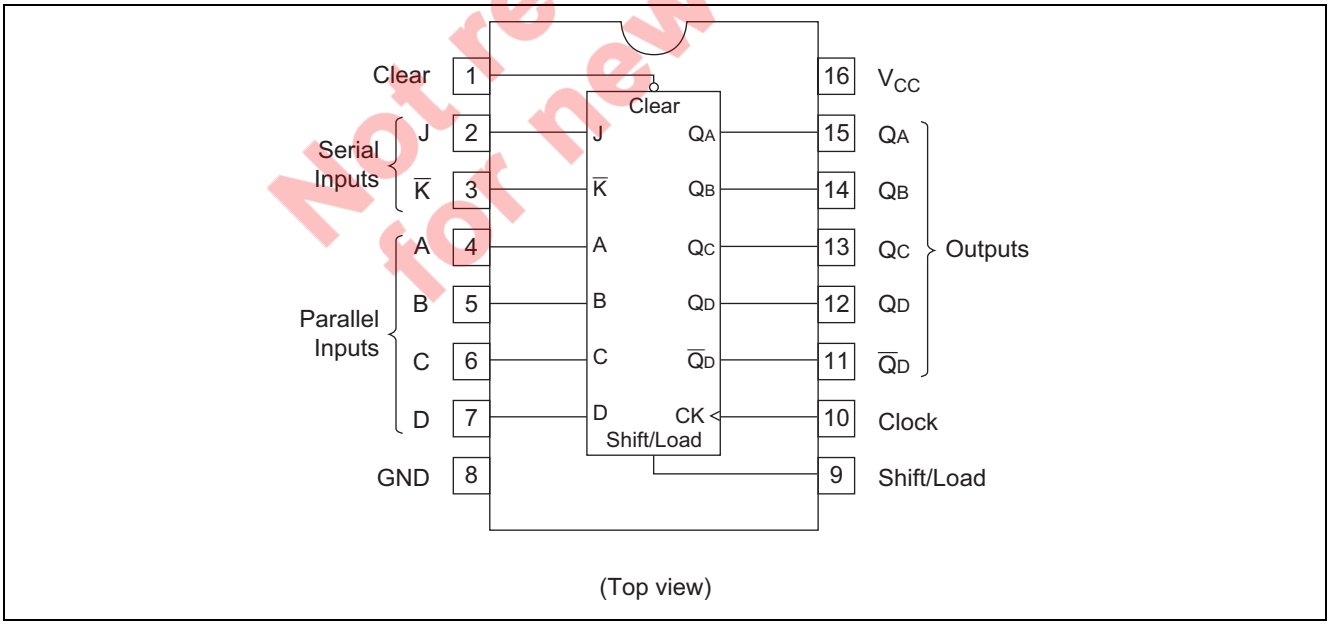
Parallel loading is accomplished by applying the four bits of data and taking the shift / load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shifting is accomplished synchronously when the shift / load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS195AFPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Pin Arrangement



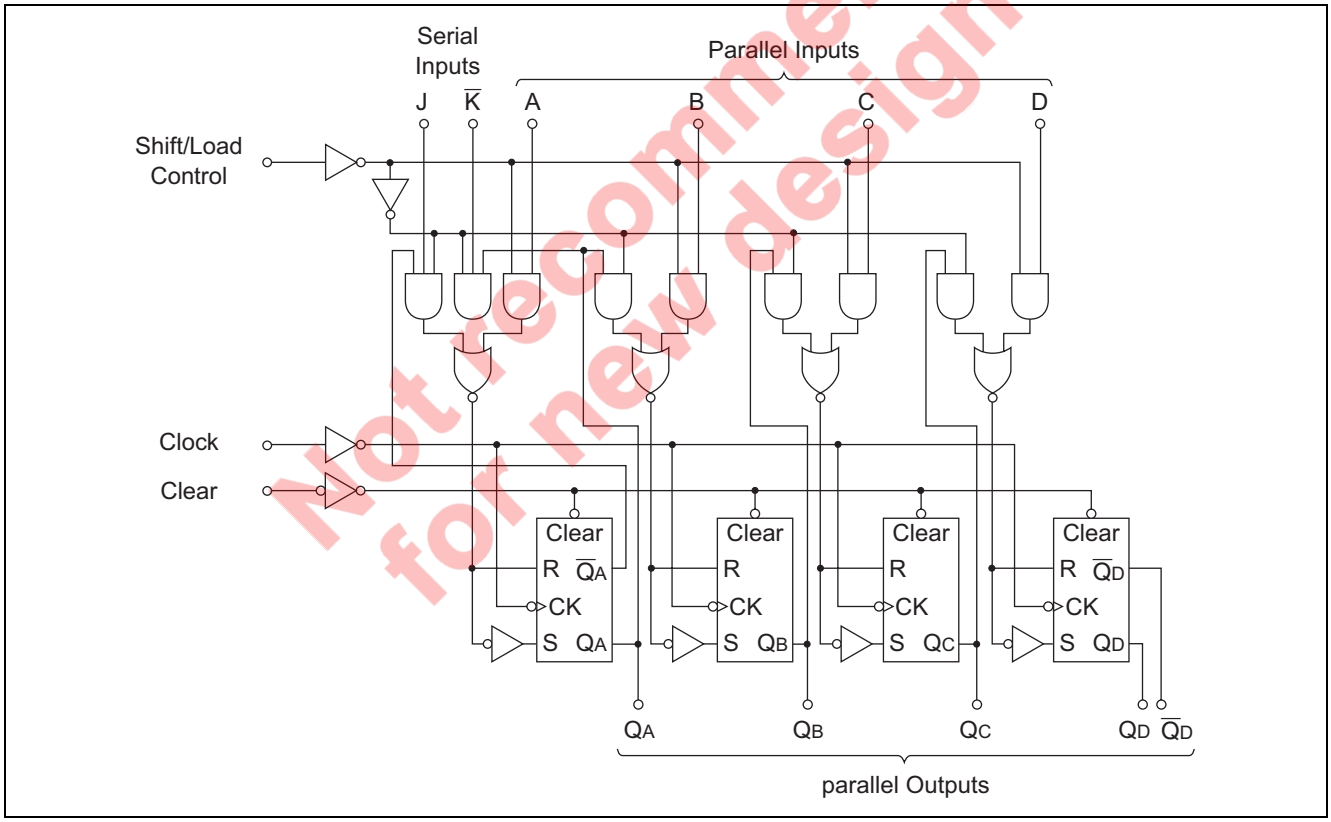
(Top view)

Function Table

Inputs									Outputs				
Clear	Shift / Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Notes: 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. a to d; the level of steady-state input at inputs A, B, C, or D, respectively
4. Q_{A0} to Q_{D0}; the level of Q_A, Q_B, Q_C, or Q_D, respectively before the indicated steady-state input conditions were established.
5. Q_{An} to Q_{Cn}; the level of Q_A, Q_B, Q_C, respectively before the most-recent ↑ transition of the clock.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	µA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	–20	25	75	°C
Clock frequency		f_{clock}	0	—	30	MHz
Clock pulse width		$t_{w\,(CK)}$	16	—	—	ns
Clear pulse width		$t_{su\,(CLR)}$	12	—	—	ns
Setup time	Shift / load	t_{su}	25	—	—	ns
	Serial and parallel data		15	—	—	ns
	Clear inactive-state		25	—	—	ns
Release time		$t_{release}$	—	—	5	ns
Hold time		t_h	0	—	—	ns

Electrical Characteristics

(Ta = –20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA; V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
		—	—	0.5		I_{OL} = 8 mA
Input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
Short-circuit output current	I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current**	I_{CC}	—	14	21	mA	V_{CC} = 5.25 V
Input clamp voltage	V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

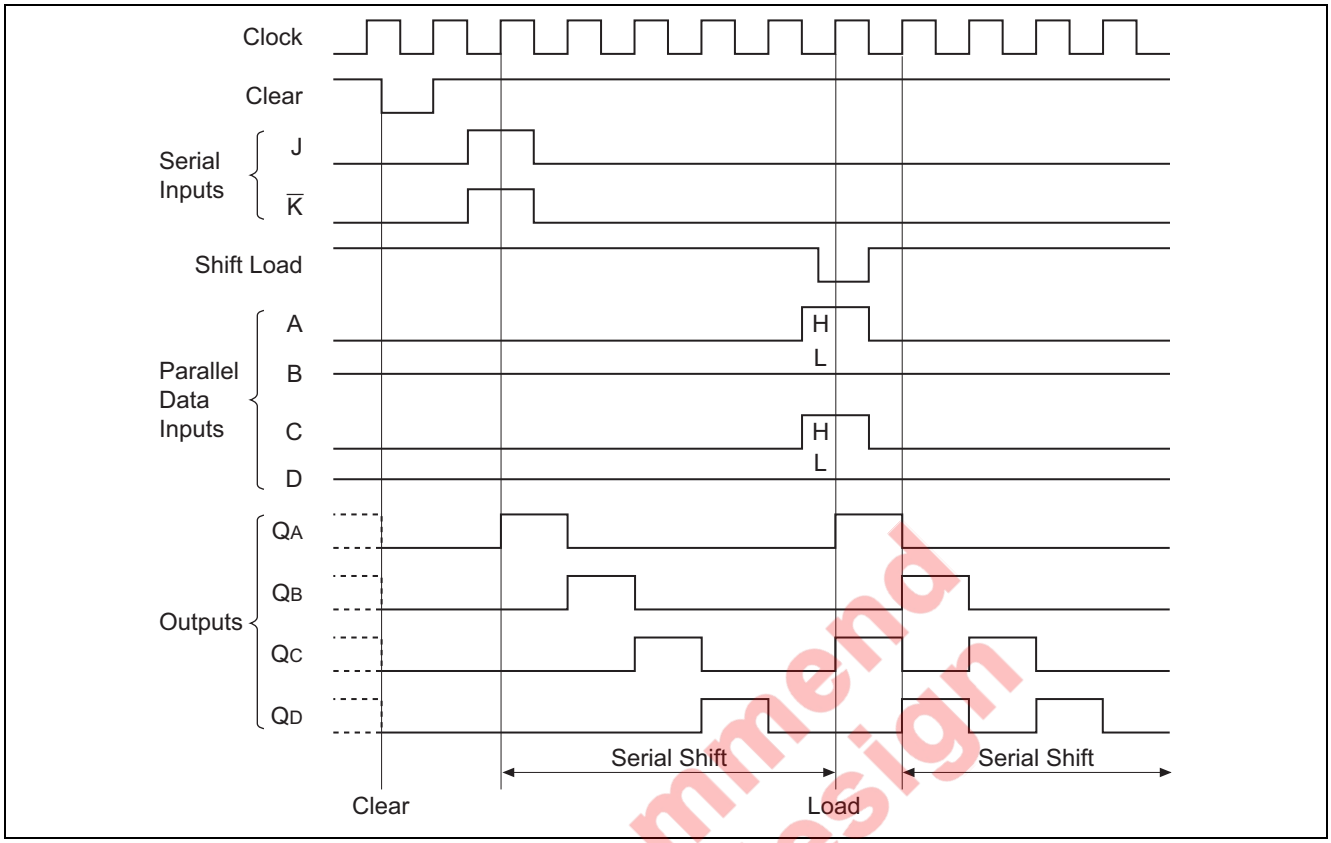
** With all outputs open, shift / load grounded, and 4.5 V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

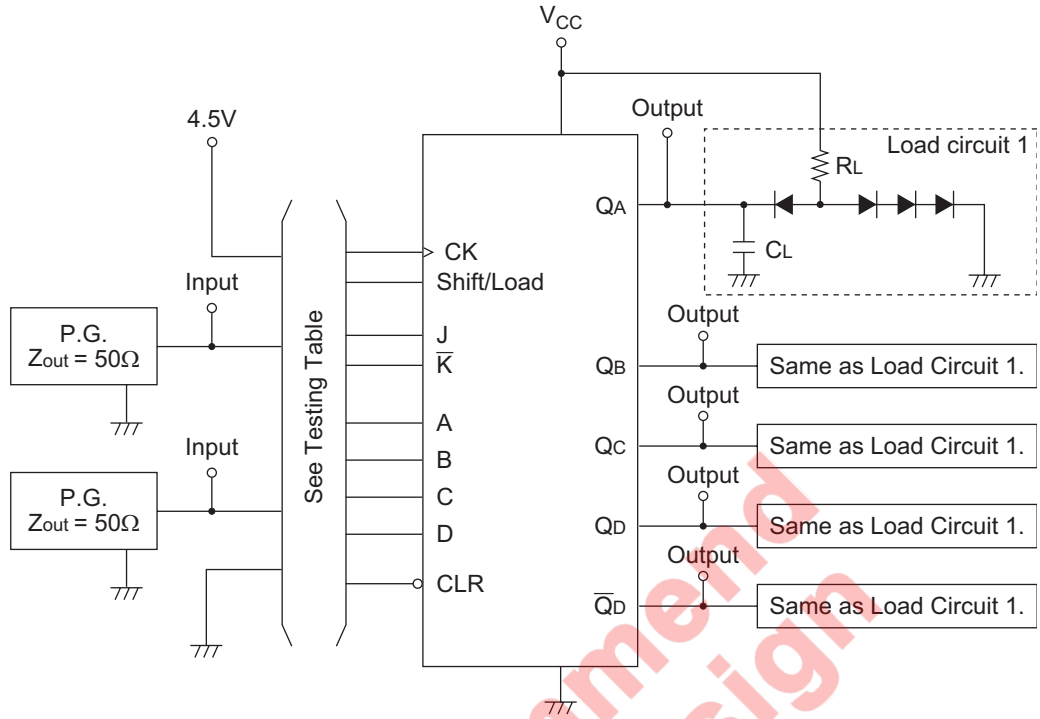
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}	Clock	Q_A to Q_D	30	39	—	MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PHL}	Clear	Q_A to Q_D	—	19	30	ns	
	t_{PLH}	Clock	Q_A to Q_D	—	14	22	ns	
	t_{PHL}		$\overline{Q}_D$	—	17	26	ns	

Count Sequence



Testing Method

Test Circuit



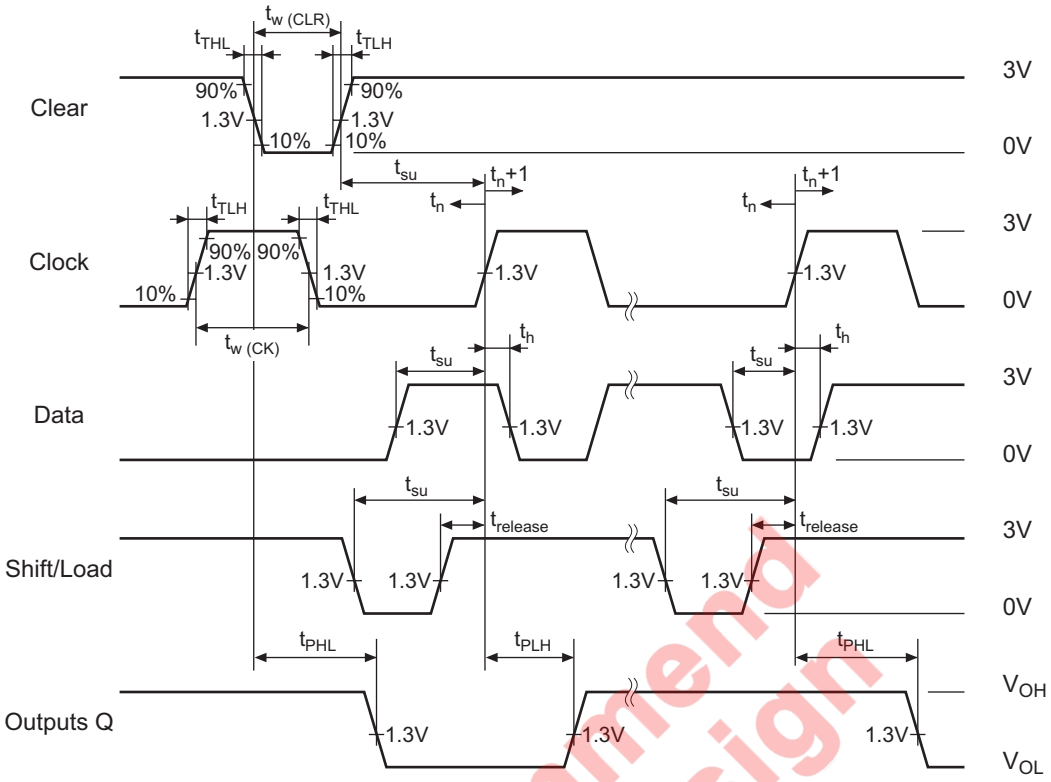
Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

Testing Table

Item	From input to output	Inputs								
		CLR	Shift / Load	J	$\overline{K}$	CK	A	B	C	D
f_{max}		4.5V	4.5V	4.5V	GND	IN	4.5V	4.5V	4.5V	4.5V
t_{PLH} t_{PHL}	Clear→ Q_A to Q_D	IN	GND	4.5V	4.5V	IN	4.5V	4.5V	4.5V	4.5V
	Clock→ Q_A to Q_D, $\overline{Q}_D$	4.5V	4.5V	4.5V	GND	IN	4.5V	4.5V	4.5V	4.5V
		4.5V	GND	4.5V	4.5V	IN	IN	IN	IN	IN

Item	From input to output	Outputs				
		Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
f_{max}		OUT	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	Clear→ Q_A to Q_D	OUT	OUT	OUT	OUT	—
	Clock→ Q_A to Q_D, $\overline{Q}_D$	OUT	OUT	OUT	OUT	OUT
		OUT	OUT	OUT	OUT	OUT

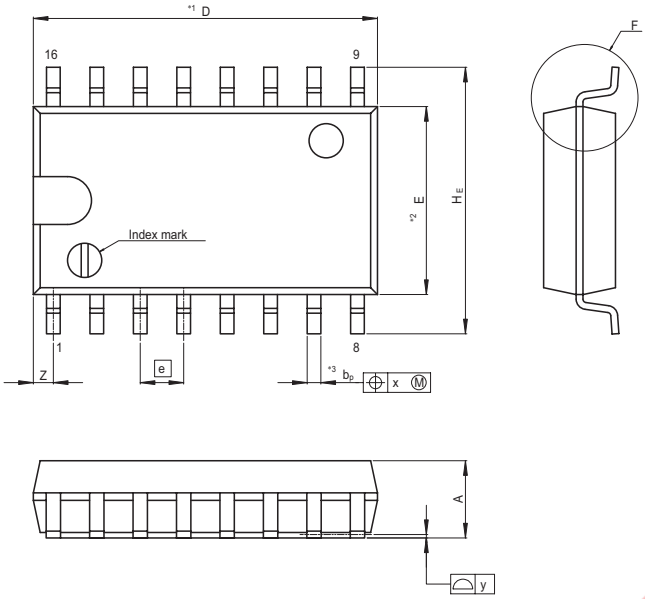
Waveform



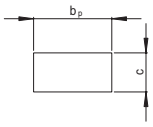
Notes:
1. Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle 50%
2. A clear pulse is applied prior to each test.
3. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.
4. J and $\overline{K}$ inputs are tested the same as data A, B, C, and D inputs except that shift / load input remains high.
5. t_n; bit time beroer clocking transition.
6. t_{n+1}; bit time after one clocking transition.
7. t_{n+4}; bit time after four clocking transition.

Package Dimensions

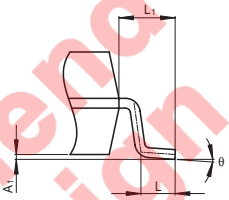
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A_2	——	——	——
A_1	0.00	0.10	0.20
A	——	——	2.20
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.15	0.20	0.25
c_1	——	——	——
θ	0°	——	8°
H_E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.80
L	0.50	0.70	0.90
L_1	——	1.15	——

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