

HD74LS75

Quadruple Bistable Latches

REJ03D0416-0300 Rev.3.00 May 10, 2006

The HD74LS75 is ideally suited for use as temporary storage for binary information between processing units and input / output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high. This device features complementary Q and \overline{Q} outputs from a 4-bit latch.

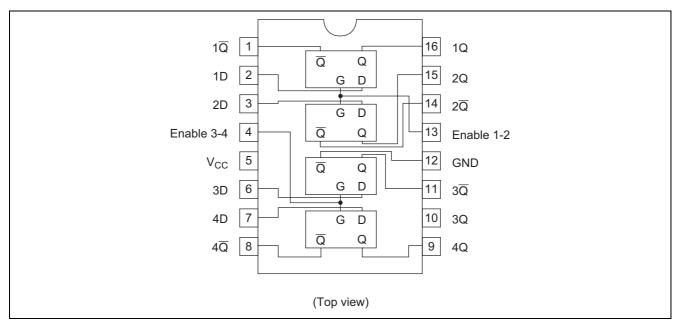
Features

Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS75P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	Р	_
HD74LS75FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement

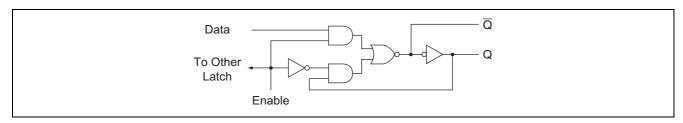


Function Table

Inp	uts	Outputs			
D	G	Q	Q		
L	Н	L	Н		
Н	Н	Н	L		
X	L	Q_0	$\overline{\overline{Q}}_0$		

H; high level, L; low level, X; irrelevant

Circuit Schematic (1/4)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P _T	400	mW
Storage temperature	Tstg	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Тур	Max	Unit
Supply voltage	Vcc	4.75	5.00	5.25	V
Output current	I _{OH}	_	_	-400	μΑ
Output current	I _{OL}	_	_	8	mA
Operating temperature	Topr	-20	25	75	°C
Pulse width	tw	20	_	_	ns
Setup time	tsu	15	_	_	ns
Hold time	th	5	_	_	ns

Q₀; level of Q before the indicated steady-state input conditions were established.

 $[\]overline{Q}_0$; complement of Q_0 or level of \overline{Q}_0 before the indicated steady-state input conditions were established.

Electrical Characteristics

 $(Ta = -20 \text{ to } +75 \text{ }^{\circ}\text{C})$

Item		Symbol	min.	typ.*	max.	Unit	Condition		
Input voltage		V_{IH}	2.0	_	_	V			
Input voltag	je	V_{IL}	_	_	0.8	V			
		V _{OH}	2.7	_	_	V	$V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V},$ $I_{OH} = -400 \mu\text{A}$		
Output volta	age	V _{OL}	_	_	0.4	V	$I_{OL} = 4 \text{ mA}$ $V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V},$		
			_	_	0.5	V	$I_{OL} = 8 \text{ mA}$ $V_{IL} = 0.8 \text{ V}$		
	D input	1	_	_	20	μΑ	V _{CC} = 5.25 V, V _I = 2.7 V		
	G input	I _{IH}	_	_	80		VCC = 3.23 V, VI = 2.7 V		
Input	nput D input		_	_	-0.4	mA	V _{CC} = 5.25 V, V _I = 0.4 V		
current G input		l _{IL}	_	_	-1.6	IIIA	V _{CC} = 5.25 v, v ₁ = 0.4 v		
	D input	ı	_	_	0.1	mA	V _{CC} = 5.25 V, V _I = 7 V		
G input		l _l	_	_	0.4	IIIA	VCC = 3.23 V, V = 7 V		
Short-circui current	t output	los	-20	_	-100	mA	V _{CC} = 5.25 V		
Supply current**		Icc	_	6.3	12	mA	V _{CC} = 5.25 V		
Input clamp voltage		V _{IK}	_	_	-1.5	V	$V_{CC} = 4.75 \text{ V}, I_{IN} = -18 \text{ mA}$		

Notes: $^*V_{CC} = 5 \text{ V}$, $Ta = 25^{\circ}C$

Switching Characteristics

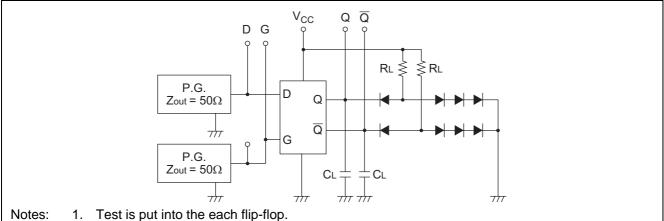
 $(V_{CC} = 5 \text{ V}, \text{Ta} = 25^{\circ}\text{C})$

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
	t _{PLH}	D	Q		15	27	ns	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega$
	t _{PHL}				9	17		
Propagation delay time	t _{PLH}	D	Q		12	20		
	t _{PHL}				7	15		
	t _{PLH}	G	Q	_	15	27	ns	
	t _{PHL}			_	14	25		
	t _{PLH}	G	Q	_	16	30	ns	
	t _{PHL}			_	7	15		

 $^{^{\}star\star}$ I_{CC} is measured with all outputs open and all inputs grounded.

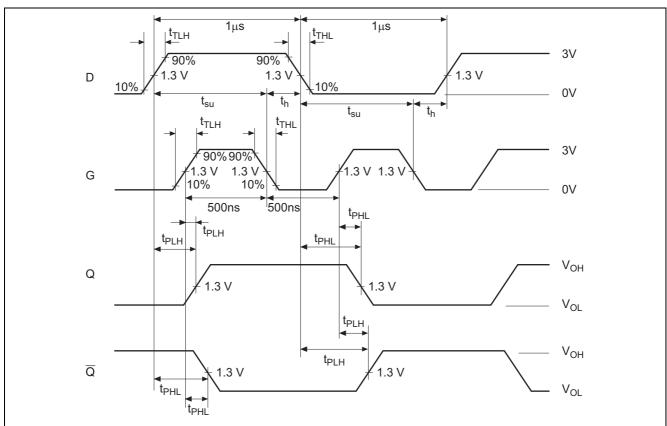
Testing Method

Test Circuit



- Test is put into the each flip-flop.
- C_L includes probe and jig capacitance.
- 3. All diodes are 1S2074(H).

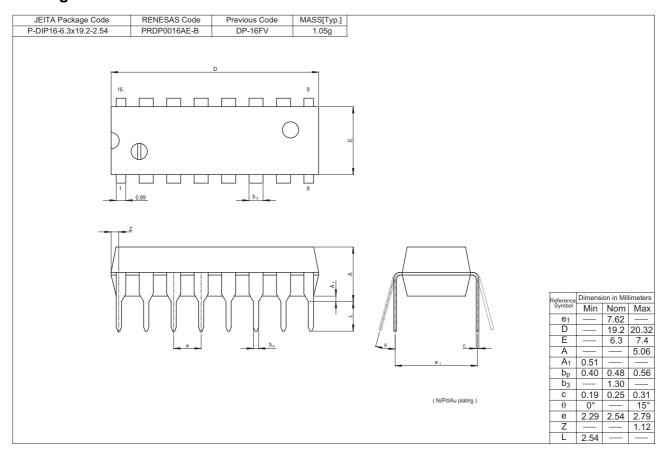
Waveform

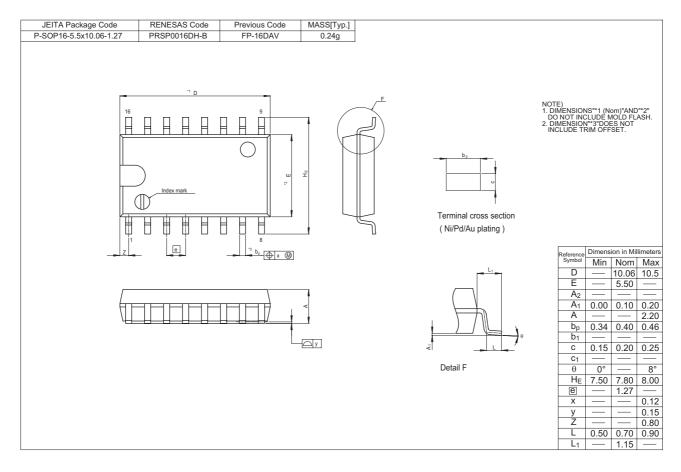


Notes:

- 1. Input pulse; D input: PRR = 500 kHz, G input; PRR = 1 MHz, $t_{THL} \leq 10$ ns, $t_{TLH} \leq 10$ ns.
- When measuring propugation delay times from the D input, the corresponding G input must be held high.

Package Dimensions





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