

# HD74LV2G74A

## Single D-type Flip Flops with Preset and Clear

REJ03D0097-0500  
 (Previous: ADE-205-346D)  
 Rev.5.00  
 Apr 07, 2006

### Description

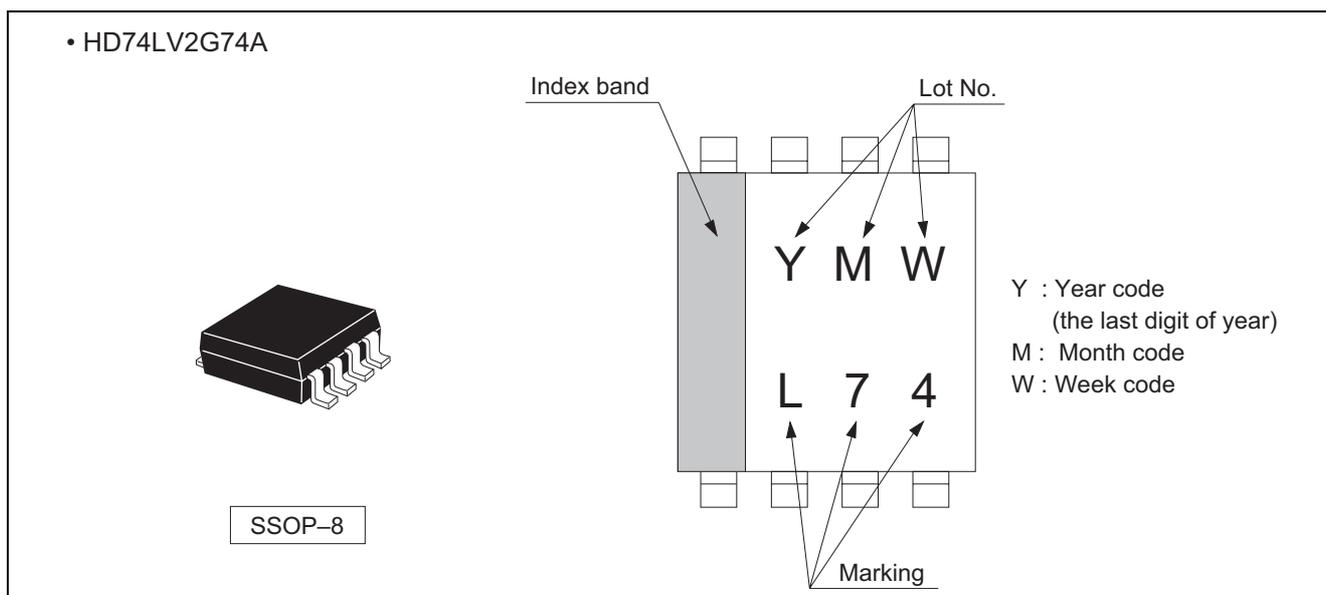
The HD74LV2G74A has independent data, preset, clear, and clock inputs  $Q$  and  $\bar{Q}$  outputs in an 8 pin package. The input data is transferred to the output at the rising edge of clock pulse CLK. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

### Features

- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- Electrical characteristics equivalent to the HD74LV74A  
 Supply voltage range : 1.65 to 5.5 V  
 Operating temperature range : -40 to +85°C
- All inputs  $V_{IH}$  (Max.) = 5.5 V (@  $V_{CC}$  = 0 V to 5.5 V)  
 All outputs  $V_O$  (Max.) = 5.5 V (@  $V_{CC}$  = 0 V)
- Output current  $\pm 6$  mA (@  $V_{CC}$  = 3.0 V to 3.6 V),  $\pm 12$  mA (@  $V_{CC}$  = 4.5 V to 5.5 V)
- All the logical input has hysteresis voltage for the slow transition.
- Ordering Information

Part Name	Package Type	Package Code (Previous code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV2G74AUSE	SSOP-8 pin	PVSP0008KA-A (TTP-8DBV)	US	E (3,000 pcs / Reel)

### Outline and Article Indication



### Function Table

Inputs				Outputs	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>*1</sup>	H <sup>*1</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	↓	X	Q <sub>0</sub>	$\overline{\text{Q}}_0$

H : High level

L : Low level

X : Immaterial

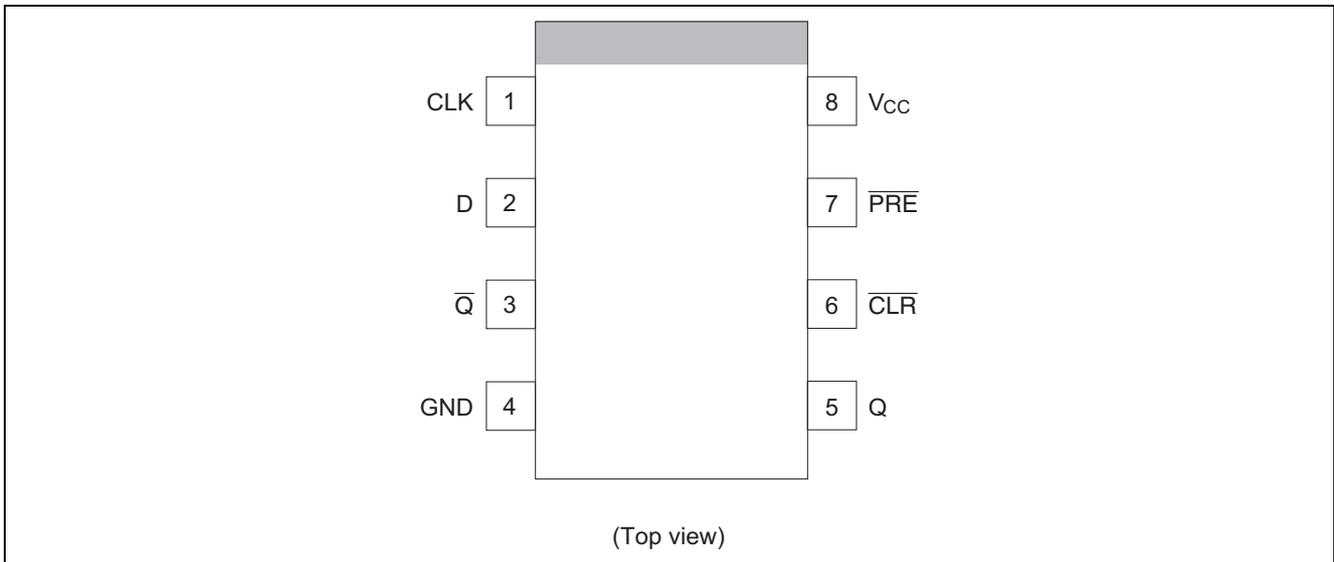
↑ : Low to high transition

↓ : High to low transition

Q<sub>0</sub> : The level of Q immediately before the input conditions shown in the above table are determined.

Note : 1. Q and  $\overline{\text{Q}}$  will remain high as long as preset and clear are low, but Q and  $\overline{\text{Q}}$  are unpredictable, if preset and clear go high simultaneously.

### Pin Arrangement



### Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V	
Input voltage range <sup>*1</sup>	$V_I$	-0.5 to 7.0	V	
Output voltage range <sup>*1, 2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$	V	Output : H or L
		-0.5 to 7.0		$V_{CC}$ : OFF
Input clamp current	$I_{IK}$	-20	mA	$V_I < 0$
Output clamp current	$I_{OK}$	$\pm 50$	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	$\pm 25$	mA	$V_O = 0$ to $V_{CC}$
Continuous current through $V_{CC}$ or GND	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) <sup>*3</sup>	$P_T$	200	mW	
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

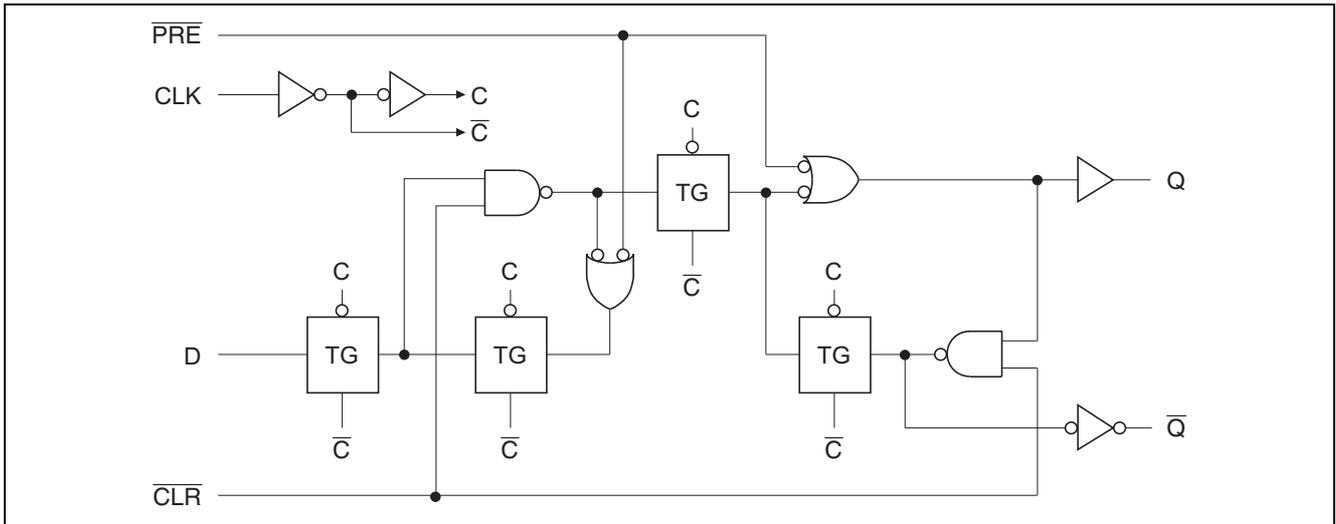
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150 $^\circ\text{C}$ .

### Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	$V_{CC}$	1.65	5.5	V	
Input voltage range	$V_I$	0	5.5	V	
Output voltage range	$V_O$	0	$V_{CC}$	V	
Output current	$I_{OL}$	—	1	mA	$V_{CC} = 1.65$ to $1.95$ V
		—	2		$V_{CC} = 2.3$ to $2.7$ V
		—	6		$V_{CC} = 3.0$ to $3.6$ V
		—	12		$V_{CC} = 4.5$ to $5.5$ V
	$I_{OH}$	—	-1		$V_{CC} = 1.65$ to $1.95$ V
		—	-2		$V_{CC} = 2.3$ to $2.7$ V
		—	-6		$V_{CC} = 3.0$ to $3.6$ V
		—	-12		$V_{CC} = 4.5$ to $5.5$ V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	300	ns / V	$V_{CC} = 1.65$ to $1.95$ V
		0	200		$V_{CC} = 2.3$ to $2.7$ V
		0	100		$V_{CC} = 3.0$ to $3.6$ V
		0	20		$V_{CC} = 4.5$ to $5.5$ V
Operating free-air temperature	$T_a$	-40	85	$^\circ\text{C}$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V <sub>CC</sub> (V) *	Min	Typ	Max	Unit	Test condition
Input voltage	V <sub>IH</sub>	1.65 to 1.95	V <sub>CC</sub> ×0.75	—	—	V	
		2.3 to 2.7	V <sub>CC</sub> ×0.7	—	—		
		3.0 to 3.6	V <sub>CC</sub> ×0.7	—	—		
		4.5 to 5.5	V <sub>CC</sub> ×0.7	—	—		
	V <sub>IL</sub>	1.65 to 1.95	—	—	V <sub>CC</sub> ×0.25		
		2.3 to 2.7	—	—	V <sub>CC</sub> ×0.3		
		3.0 to 3.6	—	—	V <sub>CC</sub> ×0.3		
		4.5 to 5.5	—	—	V <sub>CC</sub> ×0.3		
Hysteresis voltage	V <sub>H</sub>	1.8	—	0.25	—	V	V <sub>T+</sub> - V <sub>T-</sub>
		2.5	—	0.30	—		
		3.3	—	0.35	—		
		5.0	—	0.45	—		
Output voltage	V <sub>OH</sub>	Min to Max	V <sub>CC</sub> -0.1	—	—	V	I <sub>OH</sub> = -50 μA
		1.65	1.4	—	—		I <sub>OH</sub> = -1 mA
		2.3	2.0	—	—		I <sub>OH</sub> = -2 mA
		3.0	2.48	—	—		I <sub>OH</sub> = -6 mA
		4.5	3.8	—	—		I <sub>OH</sub> = -12 mA
	V <sub>OL</sub>	Min to Max	—	—	0.1		I <sub>OL</sub> = 50 μA
		1.65	—	—	0.3		I <sub>OL</sub> = 1 mA
		2.3	—	—	0.4		I <sub>OL</sub> = 2 mA
		3.0	—	—	0.44		I <sub>OL</sub> = 6 mA
		4.5	—	—	0.55		I <sub>OL</sub> = 12 mA
Input current	I <sub>IN</sub>	0 to 5.5	—	—	±1	μA	V <sub>IN</sub> = 5.5 V or GND
Quiescent supply current	I <sub>CC</sub>	5.5	—	—	10	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0
Output leakage current	I <sub>OFF</sub>	0	—	—	5	μA	V <sub>IN</sub> or V <sub>O</sub> = 0 to 5.5 V
Input capacitance	C <sub>IN</sub>	3.3	—	2.5	—	pF	V <sub>IN</sub> = V <sub>CC</sub> or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

V<sub>CC</sub> = 1.8 ± 0.15 V

Item	Symbol	T <sub>a</sub> = 25°C			T <sub>a</sub> = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f <sub>max</sub>	30	60	—	20	—	MHz	C <sub>L</sub> = 15 pF		
		20	40	—	15	—		C <sub>L</sub> = 50 pF		
Propagation delay time	t <sub>PLH</sub>	—	16.3	27.0	1.0	29.0	ns	C <sub>L</sub> = 15 pF	PRE/CLR	Q or Q̄
	t <sub>PHL</sub>	—	17.9	29.0	1.0	32.0			CLK	
			—	21.6	34.0	1.0	36.5	C <sub>L</sub> = 50 pF	PRE/CLR	Q or Q̄
									CLK	
Setup time	t <sub>su</sub>	13.0	—	—	14.0	—	ns		D	
		9.0	—	—	9.0	—			PRE or CLR inactive	
Hold time	t <sub>h</sub>	0.5	—	—	0.5	—	ns			
Pulse width	t <sub>w</sub>	12.0	—	—	13.0	—	ns		PRE or CLR "L"	
		12.0	—	—	13.0	—			CLK "H" or "L"	

V<sub>CC</sub> = 2.5 ± 0.2 V

Item	Symbol	T <sub>a</sub> = 25°C			T <sub>a</sub> = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f <sub>max</sub>	50	100	—	40	—	MHz	C <sub>L</sub> = 15 pF		
		30	70	—	25	—		C <sub>L</sub> = 50 pF		
Propagation delay time	t <sub>PLH</sub>	—	9.8	14.8	1.0	17.0	ns	C <sub>L</sub> = 15 pF	PRE/CLR	Q or Q̄
	t <sub>PHL</sub>	—	11.1	16.4	1.0	19.0			CLK	
			—	13.0	17.4	1.0	20.0	C <sub>L</sub> = 50 pF	PRE/CLR	Q or Q̄
									CLK	
Setup time	t <sub>su</sub>	8.0	—	—	9.0	—	ns		D	
		7.0	—	—	7.0	—			PRE or CLR inactive	
Hold time	t <sub>h</sub>	0.5	—	—	0.5	—	ns			
Pulse width	t <sub>w</sub>	8.0	—	—	9.0	—	ns		PRE or CLR "L"	
		8.0	—	—	9.0	—			CLK "H" or "L"	

V<sub>CC</sub> = 3.3 ± 0.3 V

Item	Symbol	T <sub>a</sub> = 25°C			T <sub>a</sub> = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f <sub>max</sub>	80	140	—	70	—	MHz	C <sub>L</sub> = 15 pF		
		50	90	—	45	—		C <sub>L</sub> = 50 pF		
Propagation delay time	t <sub>PLH</sub>	—	6.9	12.3	1.0	14.5	ns	C <sub>L</sub> = 15 pF	PRE/CLR	Q or Q̄
	t <sub>PHL</sub>	—	7.9	11.9	1.0	14.0			CLK	
			—	9.2	15.8	1.0	18.0	C <sub>L</sub> = 50 pF	PRE/CLR	Q or Q̄
									CLK	
Setup time	t <sub>su</sub>	6.0	—	—	7.0	—	ns		D	
		5.0	—	—	5.0	—			PRE or CLR inactive	
Hold time	t <sub>h</sub>	0.5	—	—	0.5	—	ns			
Pulse width	t <sub>w</sub>	6.0	—	—	7.0	—	ns		PRE or CLR "L"	
		6.0	—	—	7.0	—			CLK "H" or "L"	

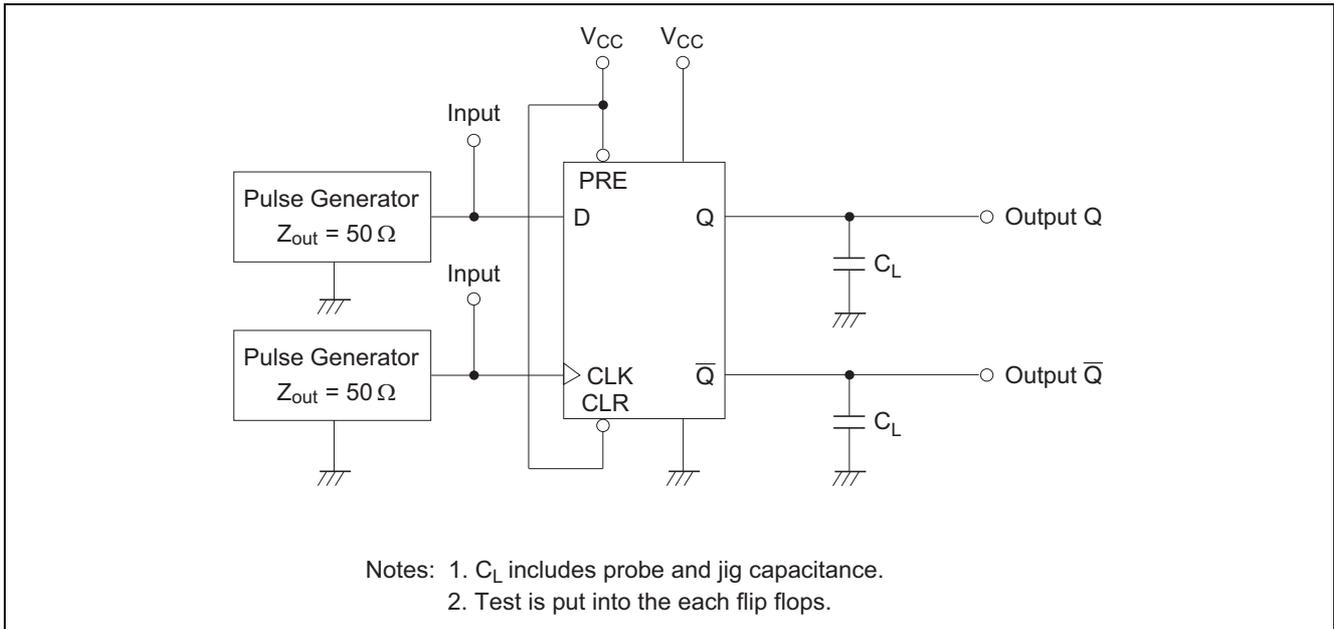
Item	Symbol	T <sub>a</sub> = 25°C			T <sub>a</sub> = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)	
		Min	Typ	Max	Min	Max					
Maximum clock frequency	f <sub>max</sub>	130	180	—	110	—	MHz	C <sub>L</sub> = 15 pF			
		90	140	—	75	—		C <sub>L</sub> = 50 pF			
Propagation delay time	t <sub>PLH</sub>	—	5.0	7.7	1.0	9.0	ns	C <sub>L</sub> = 15 pF	PRE/CLR	Q or Q̄	
	t <sub>PHL</sub>	—	5.6	7.3	1.0	8.5			CLK		
			—	6.6	9.7	1.0		11.0	C <sub>L</sub> = 50 pF	PRE/CLR	Q or Q̄
										CLK	
Setup time	t <sub>su</sub>	5.0	—	—	5.0	—	ns		D		
		3.0	—	—	3.0	—			PRE or CLR inactive		
Hold time	t <sub>h</sub>	0.5	—	—	0.5	—	ns				
Pulse width	t <sub>w</sub>	5.0	—	—	5.0	—	ns		PRE or CLR "L"		
		5.0	—	—	5.0	—			CLK "H" or "L"		

**Operating Characteristics**

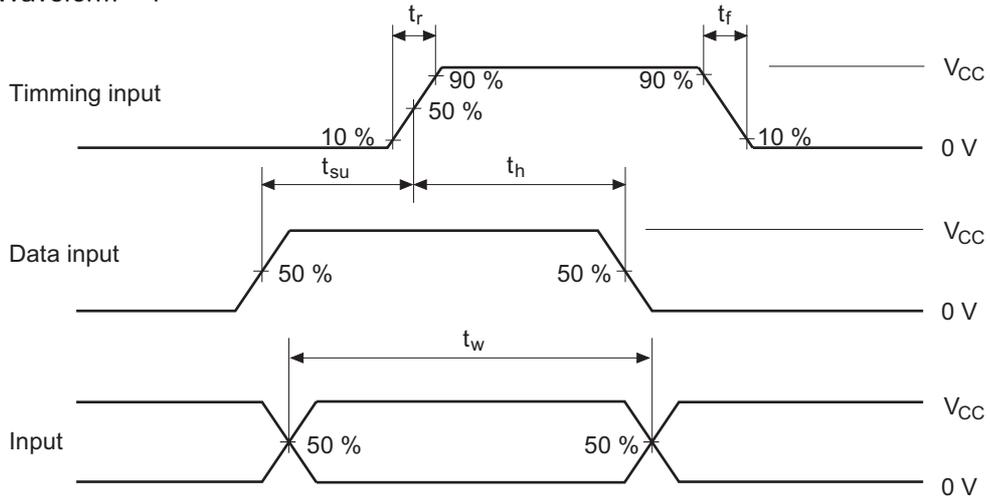
C<sub>L</sub> = 50 pF

Item	Symbol	V <sub>CC</sub> (V)	T <sub>a</sub> = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C <sub>PD</sub>	3.3	—	13.0	—	pF	f = 10 MHz
		5.0	—	14.0	—		

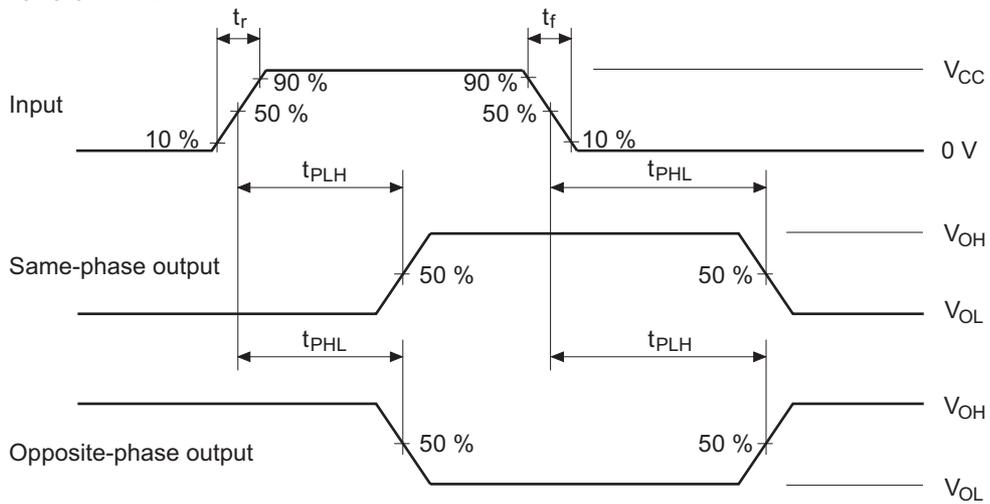
**Test Circuit**



• Waveform – 1



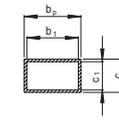
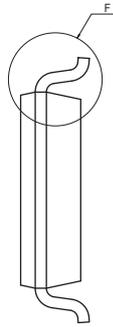
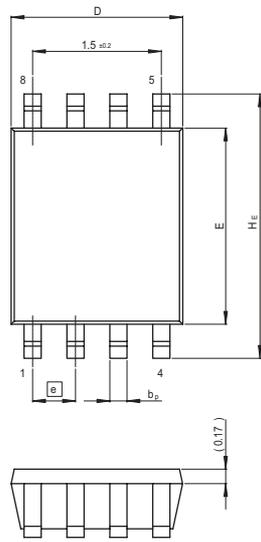
• Waveform – 2



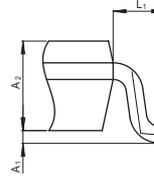
- Notes: 1. Input waveform : PRR  $\leq$  1 MHz,  $Z_o = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.  
 2. The output are measured one at a time with one transition per measurement.

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-VSSOP8-2.3x2-0.50	PVSP0008KA-A	TTP-8DB/TTP-8DBV	0.010g



Terminal cross section



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	1.8	2.0	2.2
E	2.2	2.3	2.4
A <sub>2</sub>	0.6	0.7	0.8
A <sub>1</sub>	0	—	0.1
A	—	—	—
b <sub>p</sub>	0.15	0.22	0.3
b <sub>1</sub>	—	0.20	—
c	0.08	0.13	0.23
c <sub>1</sub>	—	0.11	—
θ	—	—	—
H <sub>E</sub>	2.8	3.1	3.4
ⓐ	—	(0.5)	—
x	—	—	—
y	—	—	—
Z	—	—	—
L	—	—	—
L <sub>1</sub>	—	(0.4)	—

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