



## PA4867

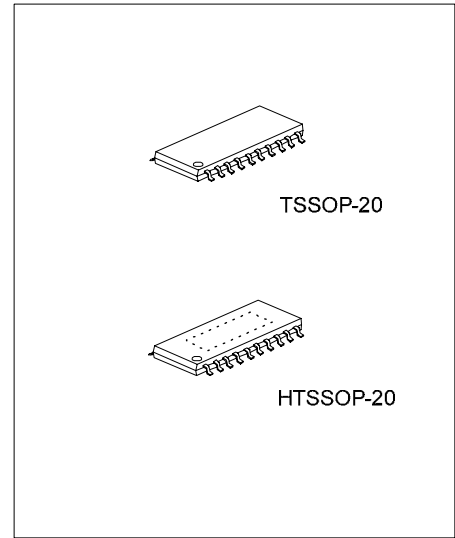
CMOS IC

### DUAL 2.1W AUDIO AMPLIFIER PLUS STEREO HEADPHONE FUNCTION

#### DESCRIPTION

The UTC **PA4867** is a stereo audio power amplifier capable of delivering typically 2.1W to a 4Ω load or 2.4W to a 3Ω load each channel with less than 1.0% THD+N using a 5V power supply. UTC **PA4867** has a new circuit topology which can eliminate headphone output coupling capacitors. And an internal input MUX allows two sets of stereo inputs to the amplifier.

The UTC **PA4867** has integrated depop circuitry that virtually eliminates transients that cause noise in the speakers during power up and when using the shutdown modes.



\*Pb-free plating product number: PA4867L

#### FEATURES

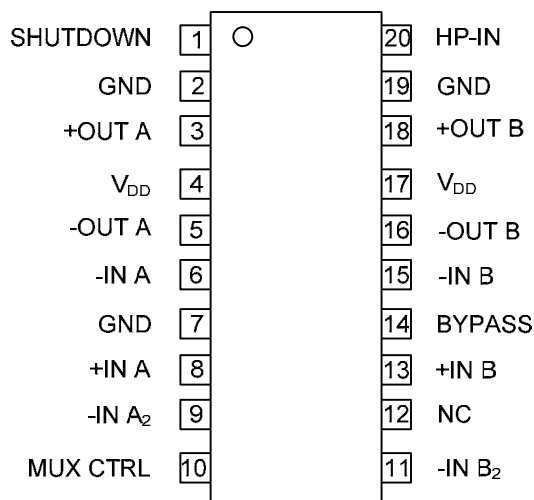
- \* Operating voltage range  $V_{DD}=2V\sim 5.5V$
- \* Output power:
  - 2.4W(typ.)@5V into 3Ω with 1% THD+N max (1kHz)
  - 2.1W(typ.)@5V into 4Ω with 1% THD+N max (1kHz)
- \* Eliminates SE-mode output coupling capacitors
- \* Shutdown mode available
- \* click and pop reduction circuitry
- \* Unity-gain stable
- \* Thermal-shutdown Protection
- \* Input MUX control
- \* SE/BTL mode available

#### ORDERING INFORMATION

Order Number		Package	Packing
Normal	Lead Free Plating		
PA4867-N20-R	PA4867L-N20-R	HTSSOP-20	Tape Reel
PA4867-N20-T	PA4867L-N20-T	HTSSOP-20	Tube
PA4867-P20-R	PA4867L-P20-R	TSSOP-20	Tape Reel
PA4867-P20-T	PA4867L-P20-T	TSSOP-20	Tube

<p>PA4867L-N20-T</p> <p>(1)Packing Type (2)Package Type (3)Lead Plating</p>	<p>(1) R: Tape Reel, T: Tube (2) N20: HTSSOP-20, P20: TSSOP-20 (3) L: Lead Free Plating, Blank: Pb/Sn</p>
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### ■ PIN CONFIGURATION



### ■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	PIN DESCRIPTION
1	SHUTDOWN	I	Entire IC into the shutdown mode when this pin connected to the $V_{DD}$
2, 7, 19	GND		Ground
3	+OUTA	O	Channel A + output in BTL mode, high impedance in SE mode
4, 17	$V_{DD}$		Supply voltage
5	-OUTA	O	Channel A - output in BTL mode, + output in SE mode
6	-INA	I	Inverting input of channel A
8	+INA	I	Non-inverting input of channel A, connected to BYPASS pin inside the IC
9	-INA <sub>2</sub>	I	Inverting input of channel A <sub>2</sub>
10	MUX CTRL		
11	-INB <sub>2</sub>	I	Inverting input of channel B <sub>2</sub>
12	NC		No Connection
13	+INB	I	Non-inverting input of channel B, connected to BYPASS pin inside the IC
14	BYPASS		Internal mid-supply bias reference bypassing
15	-INB	I	Inverting input of channel B
16	-OUTB	O	Channel B - output in BTL mode, + output in SE mode
18	+OUTB	O	Channel B + output in BTL mode, high impedance in SE mode
20	HP-IN	I	Output mode select, connected to the $V_{DD}$ for SE mode or GND for BTL mode

## ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage		6.0	V
Input Voltage		-0.3 ~ V <sub>DD</sub> +0.3	V
Power Dissipation	P <sub>D</sub>	Internally Limited	
Junction Temperature	T <sub>J</sub>	150	
Operating Temperature	T <sub>OPR</sub>	-40 ~ +85	
Storage Temperature	T <sub>STG</sub>	-65 ~ +150	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ ELECTRICAL CHARACTERISTICS

The following specifications apply for V<sub>DD</sub>= 5V unless otherwise specified. Limits apply for T<sub>A</sub>= 25 .

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>FOR ENTIRE IC</b>						
Supply Voltage	V <sub>DD</sub>		2		5.5	V
Quiescent Power Supply Current	I <sub>DD</sub>	V <sub>IN</sub> =0V, I <sub>OUT</sub> =0A, HP-IN=0V		7.5	15	mA
		V <sub>IN</sub> =0V, I <sub>OUT</sub> =0A, HP-IN=4V		3.0	6	mA
Shutdown Current	I <sub>SD</sub>	V <sub>DD</sub> applied to the SHUTDOWN pin		0.7	2	μA
<b>FOR BRIDGED-MODE OPERATION</b>						
Output Offset Voltage	V <sub>O(OFF)</sub>	V <sub>IN</sub> =0V		5	50	mV
Output Power	P <sub>OUT</sub>	THD=1%, f=1kHz	R <sub>L</sub> = 3Ω		2.2	W
			R <sub>L</sub> = 4Ω		1.9	W
			R <sub>L</sub> = 8Ω	1.0	1.1	W
		THD+N=10%, f=1kHz	R <sub>L</sub> = 3Ω		3.0	W
			R <sub>L</sub> = 4Ω		2.6	W
			R <sub>L</sub> = 8Ω		1.5	W
		THD+N=1%, f=1kHz, R <sub>L</sub> =32Ω		0.34		W
Total Harmonic Distortion+Noise	THD+N	20Hz ≤ f ≤ 20kHz, R <sub>L</sub> =4Ω, P <sub>OUT</sub> =2W		0.3		%
		A <sub>VD</sub> =2, R <sub>L</sub> =8Ω, P <sub>OUT</sub> =1W		0.3		%
Power Supply Rejection Ratio	PSRR	V <sub>DD</sub> =5V, V <sub>RIPPLE</sub> =200mV <sub>RMS</sub> , R <sub>L</sub> =8Ω, C <sub>B</sub> =2.2μF		67		dB
Channel Separation	X <sub>TALK</sub>	f=1kHz, C <sub>B</sub> =2.2μF		80		dB
Signal To Noise Ratio	SNR	V <sub>DD</sub> =5V, P <sub>OUT</sub> =1.1W, R <sub>L</sub> =8Ω		97		dB
<b>FOR SINGLE-ENDED OPERATION</b>						
Output Offset Voltage	V <sub>O(OFF)</sub>	V <sub>IN</sub> =0V		5	50	mV
Output Power	P <sub>OUT</sub>	THD = 0.5%, f = 1kHz, R <sub>L</sub> = 32Ω	75	85		mW
		THD+N = 1%, f = 1kHz, R <sub>L</sub> = 8Ω		180		
		THD+N = 1%, f = 1kHz, R <sub>L</sub> = 16Ω		165		mW
		THD+N = 1%, f = 1kHz, R <sub>L</sub> = 32Ω		88		
		THD+N = 10%, f = 1kHz, R <sub>L</sub> = 16Ω		208		mW
		THD+N = 10%, f = 1kHz, R <sub>L</sub> = 32Ω		114		
Output Voltage Swing	V <sub>OUT</sub>	THD = 0.05%, R <sub>L</sub> = 5kΩ		1		V <sub>P-P</sub>
Total Harmonic Distortion+Noise	THD+N	A <sub>V</sub> =-1, P <sub>OUT</sub> =75mW 20Hz ≤ f ≤ 20kHz, R <sub>L</sub> =32Ω		0.2		%
Power Supply Rejection Ratio	PSRR	C <sub>B</sub> =1.0μF, V <sub>RIPPLE</sub> =200mV <sub>RMS</sub> f=1kHz		52		dB
Channel Separation	X <sub>TALK</sub>	f=1kHz, C <sub>B</sub> =2.2μF		60		dB
Signal To Noise Ratio	SNR	V <sub>DD</sub> =5V, P <sub>OUT</sub> =340mW, R <sub>L</sub> =8Ω		95		dB

■ TYPICAL APPLICATION CIRCUIT

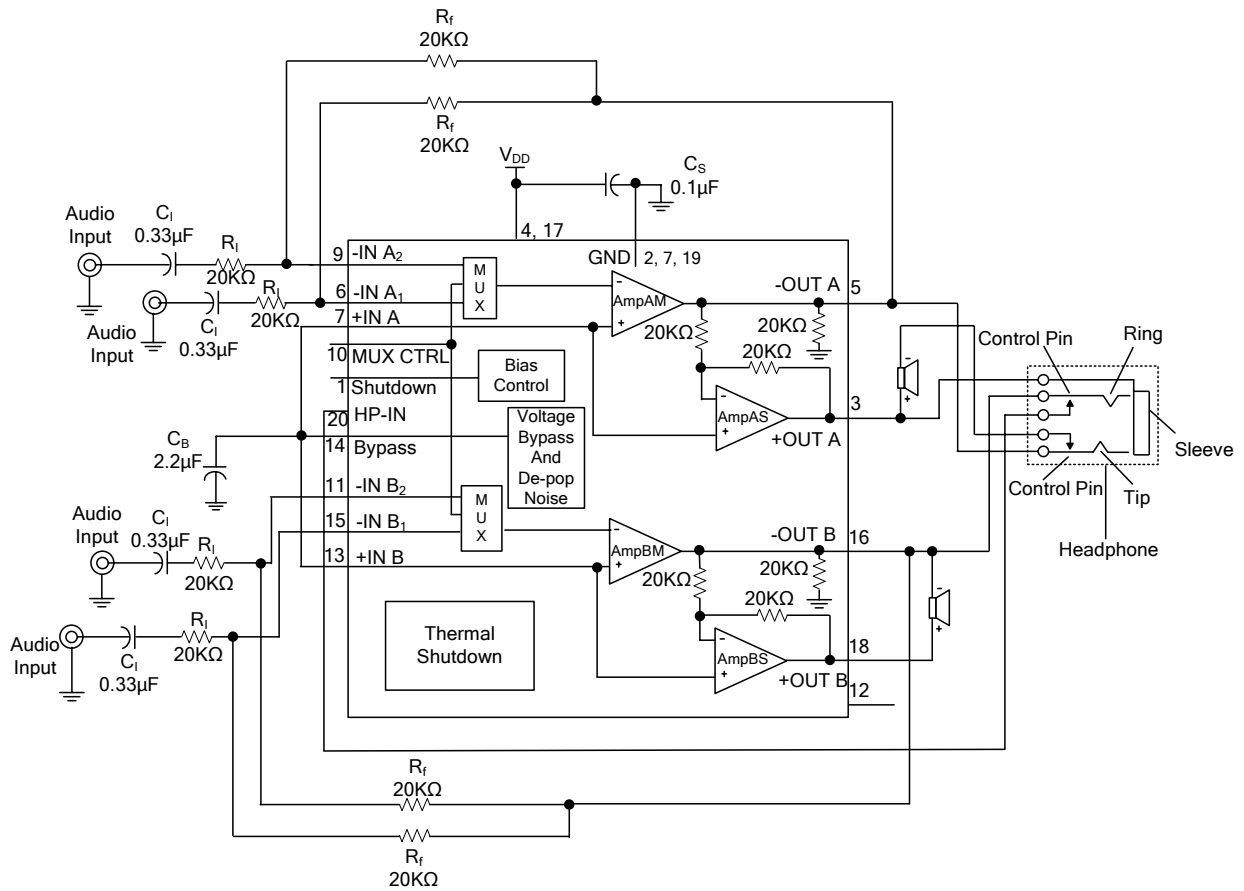
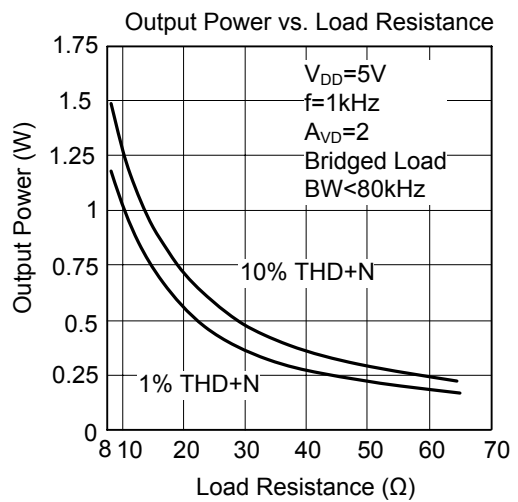
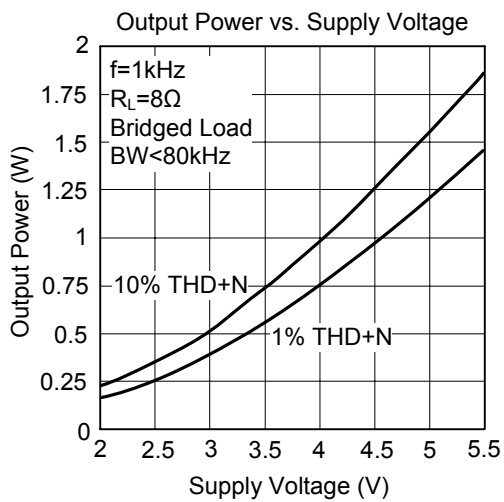
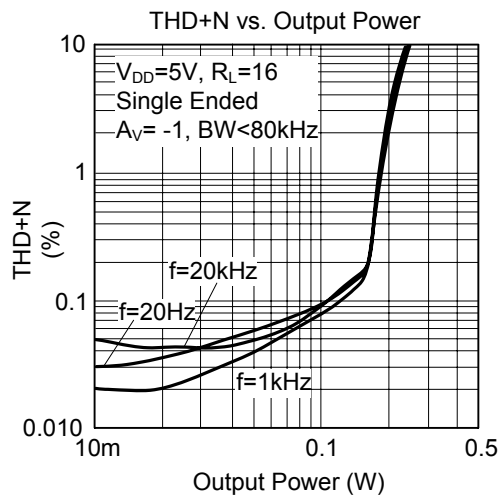
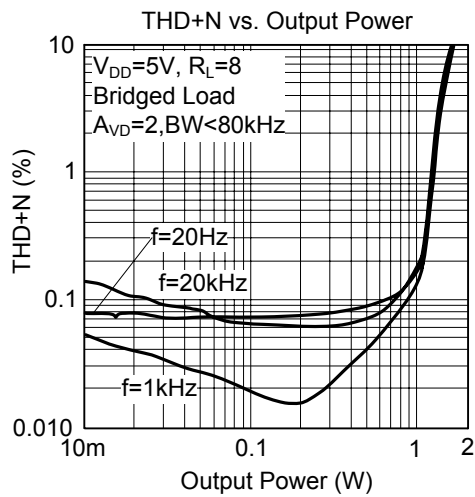
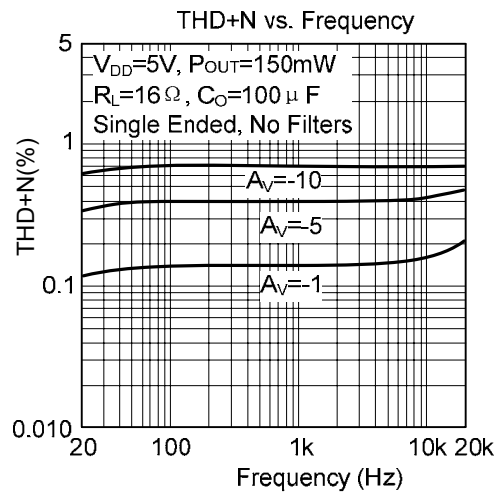
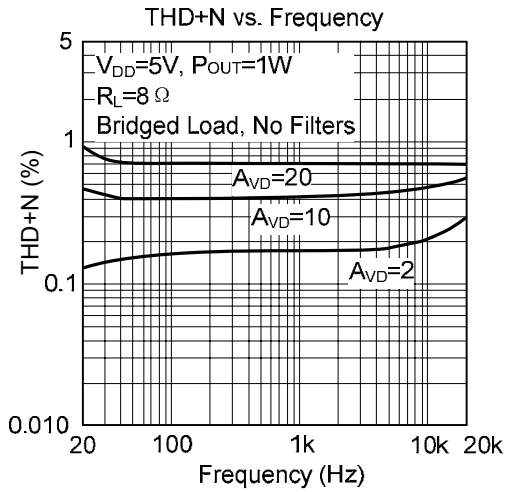
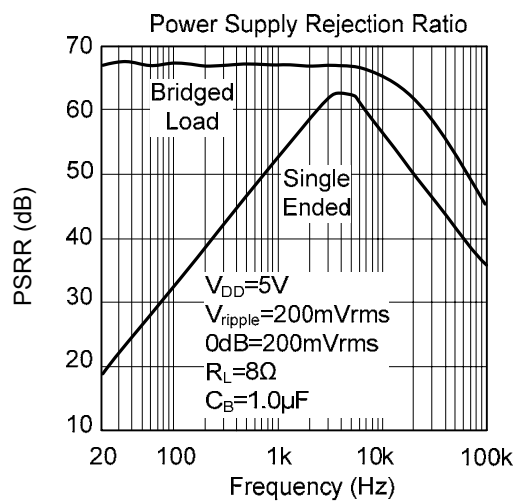
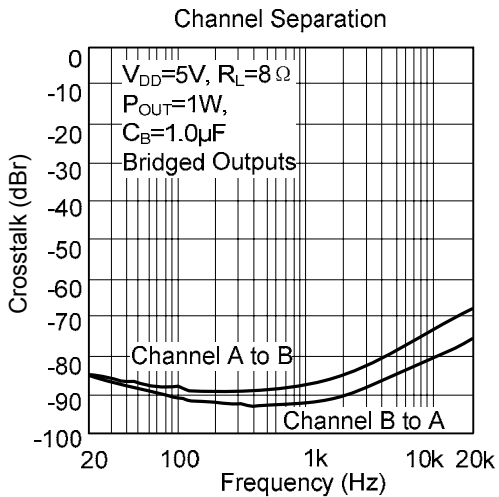
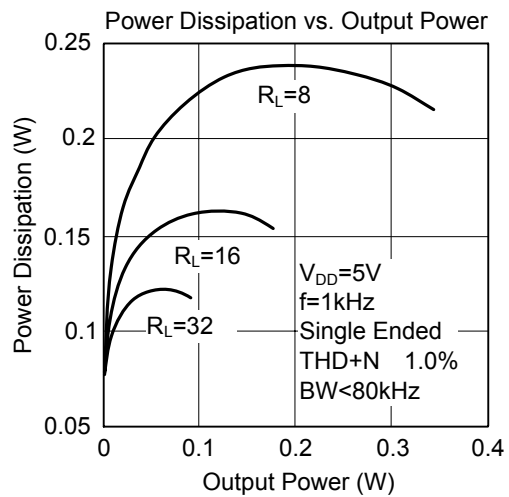
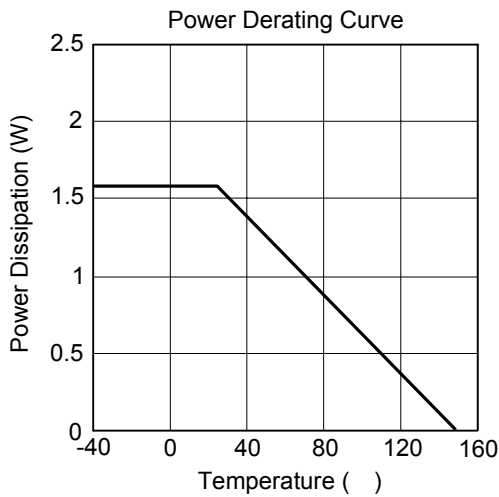
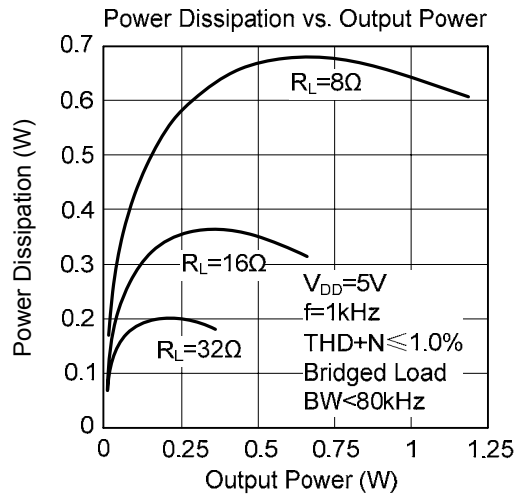
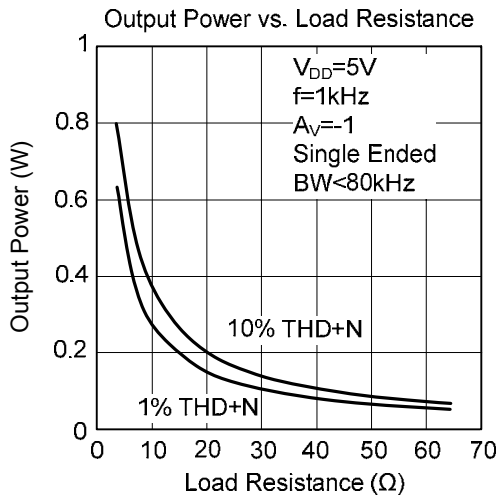


Figure 1. Typical Audio Amplifier Application Circuit

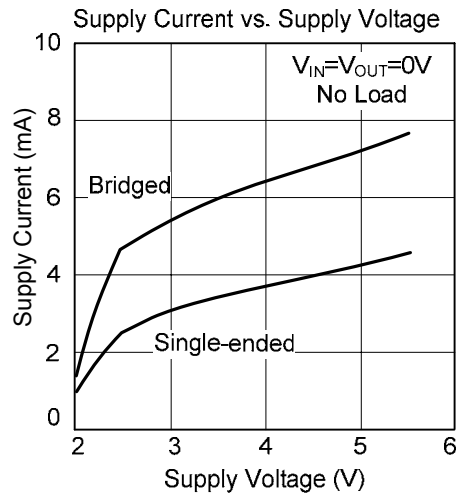
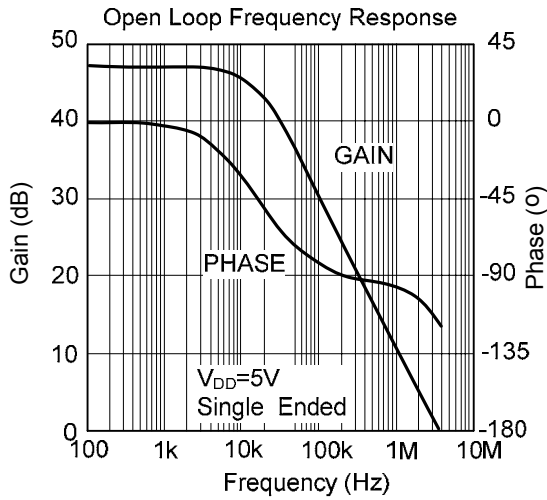
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS(Cont.)



■ TYPICAL CHARACTERISTICS(Cont.)



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