

R8830I
Brief Sheet
16-BIT RISC MICROCONTROLLER

1. Features

I CPU Core

- RDC's proprietary RISC architecture
- Five-stage pipeline
- CPU Clock speed: 20 / 25 / 33 MHz
- Supports CPU ID
- Supports 32 PIO pins

I Bus interface

- Multiplexed address and data bus which is compatible with the 80C188 microprocessor
- Supports a non-multiplexed address bus A[19:0]

I ROM/RAM Controller and Addressing Space

- 1M-byte memory address space
- 64K-byte I/O space

I PSRAM Interface

- PSRAM (Pseudo Static RAM) interface with auto-refresh control

I Compatible UART Channels

- UART speed : maximum baud rate up to 115.2Kbps

I Two Independent DMA Channels

- Supports serial ports with DMA transfers

I Asynchronous Serial Channels

- Supports two asynchronous serial channels with hardware handshaking signals

I Interrupt Controller

- The Interrupt controller with seven maskable external interrupts and one non-maskable external interrupt

I Programmable Chip-select Logic

- Programmable chip-select logic for memory or I/O bus cycle decoder

I Programmable Wait-state Generator

I Counter/Timers

- Three independent 16-bit timers and one independent watchdog timer

I Software Compatible with the 80C186 Microprocessor

I Operating Voltage Range

- Core voltage: 5V $\pm$ 10%
- I/O voltage: 5V $\pm$ 10%

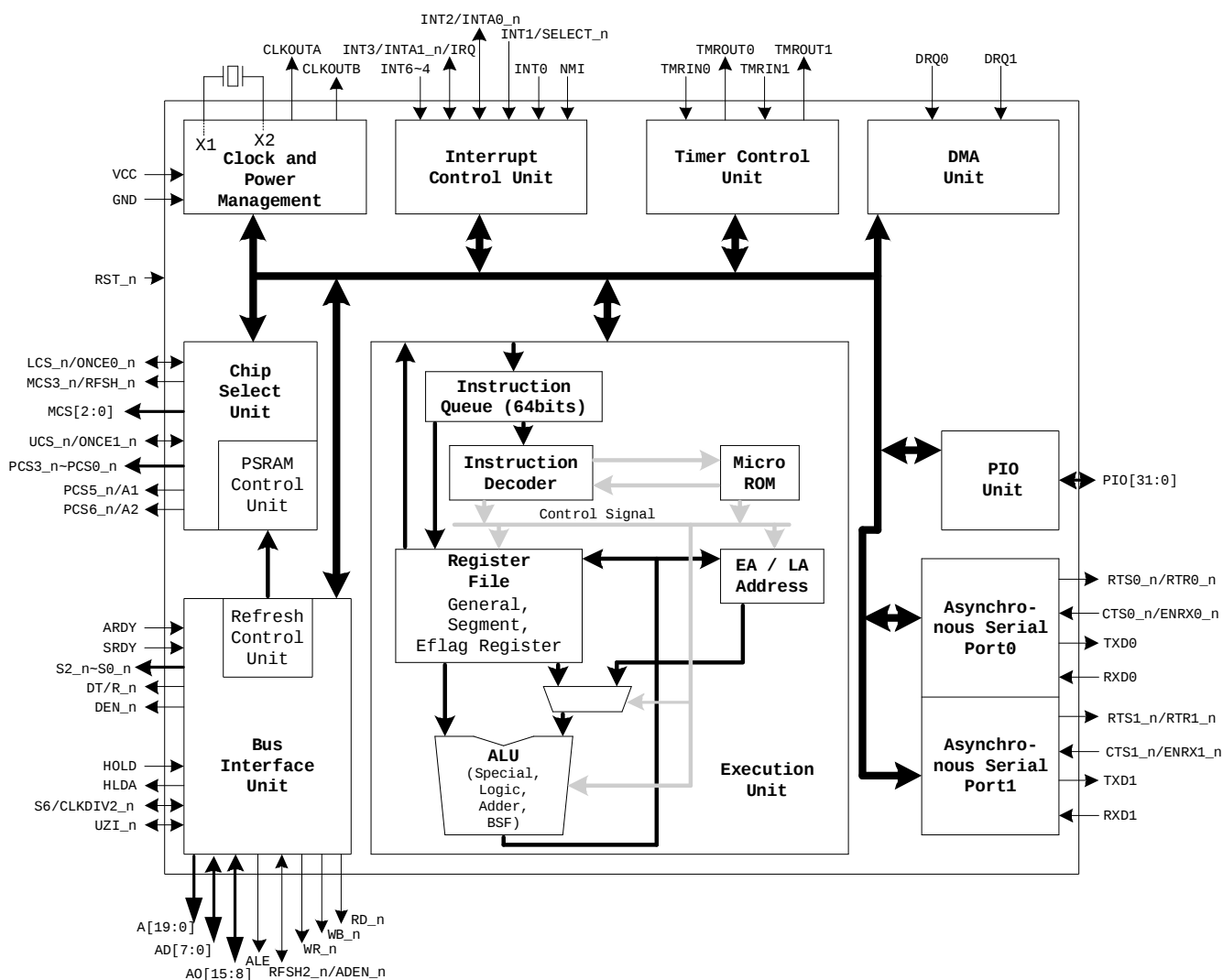
I Ambient temperature: - 40 ~ +85°C

I Power Save and Power Down Mode Support

I Package Type

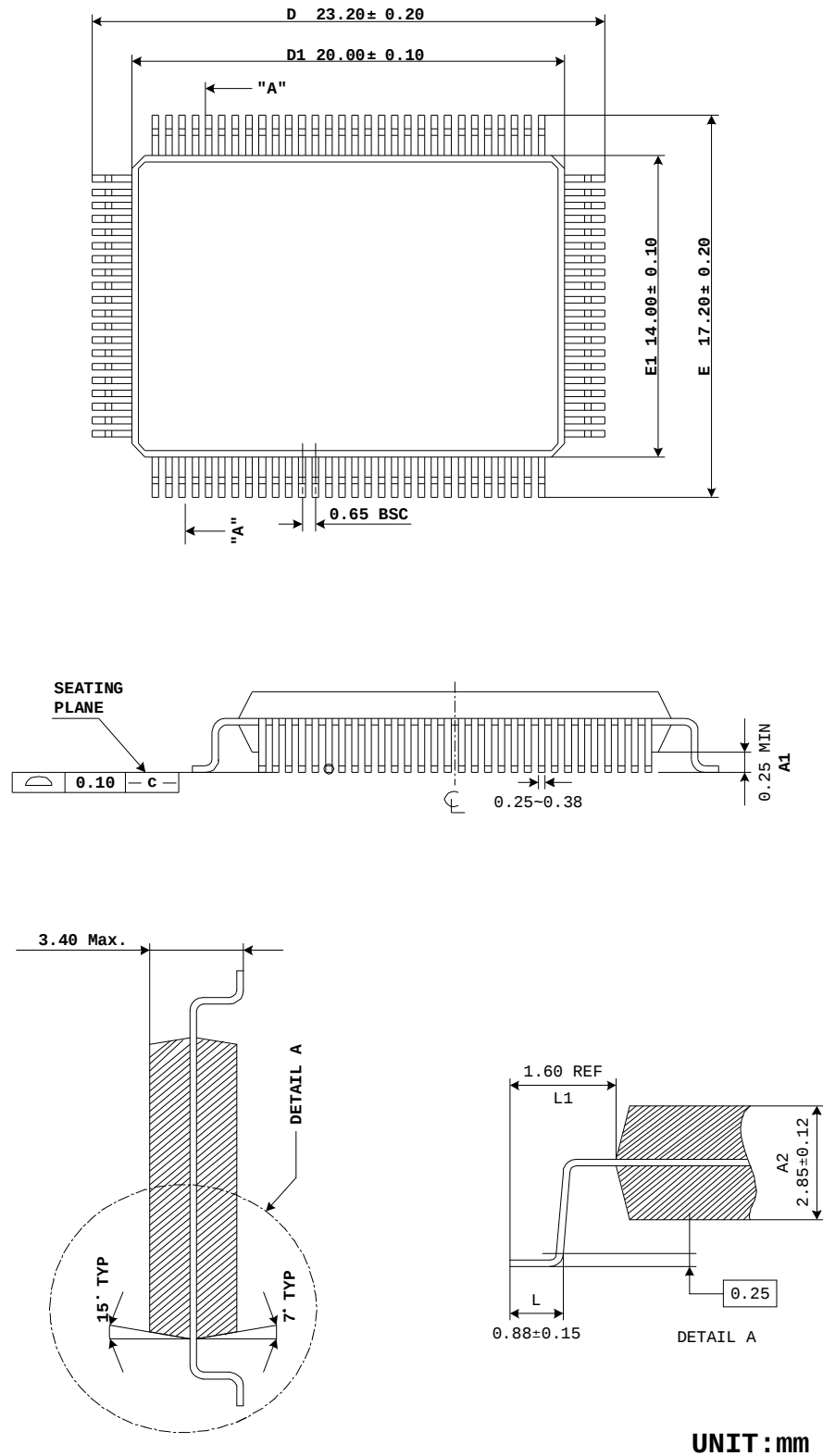
- 100 Pin PQFP & 100 Pin LQFP

2. Block Diagram

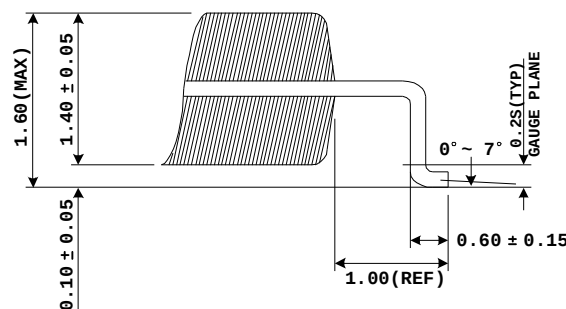
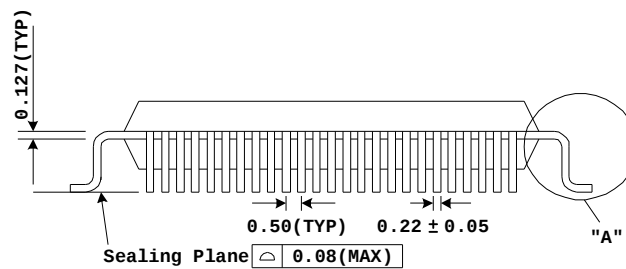
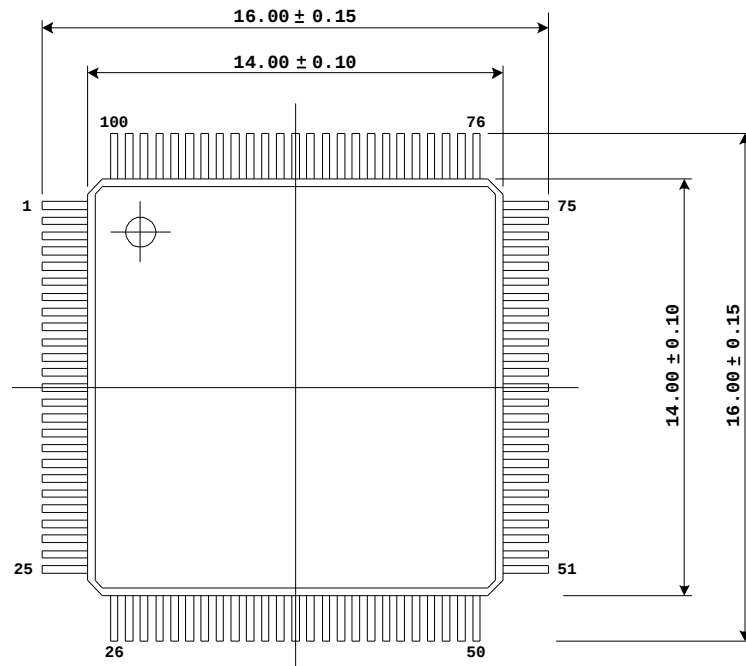


3. Package Information

PQFP 100 pins



LQFP 100 pins



UNIT : mm